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Microelectronics Reliability 44 (2004) 195–205

MICROELECTRONICS RELIABILITY

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Introductory Invited Paper

An introduction to Cu electromigration

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Received 20 October 2003

Abstract

Electromigration is a major reliability concern in today's integrated circuits due to the aggressive scaling of interconnect dimensions and the ever-increasing current densities at operation. In addition, the recent introduction of new materials and processing schemes lead to even more challenges in guaranteeing interconnect robustness against electromigration failure. In this article, we review basic electromigration physics in which the main differences between Al- and Cu-based interconnects relevant to electromigration are covered. We also discuss recent process-related advances in electromigration reliability such as the use of alloys and metal caps. Next, the impact of low-*k* inter-level dielectrics (ILD) on electromigration performance is addressed. Finally, the methodology of electromigration lifetime extrapolation, including reliability assessments of more complex interconnect geometries, is covered.

1. Introduction

Electromigration was first identified as a serious reliability concern on the Al-based integrated circuit (IC) in 1967 [1]. More than thirty years later, electromigration remains a dominant reliability concern for the modern IC due to the aggressive decrease of interconnect dimensions and the comparably aggressive increase of current densities required during operation [2] (Fig. 1). These trends warrant the implementation of new materials and more complex and challenging integration schemes, thereby spawning intense experimental and theoretical study.

A major change for the interconnect system involved the replacement of Al thin-film wiring with less resistive Cu in the late 1990s in order to decrease resistance–capacitance (RC) delay [3,4]. Cu interconnects were also expected to be more robust against electromigration failure, due to the stronger Cu–Cu bonds as indicated by its higher melting temperature relative to that of Al. Unlike Al interconnects which are fabricated through subtractive etching, Cu interconnects and vias are fabricated through a Damascene processing method, which affects the resulting electromigration behavior of the interconnect. In this paper, we will compare the interconnect schemes and electromigration behavior of Al- and Cu-based interconnects.

Since the implementation of Cu wiring, many improvements in electromigration reliability have been achieved by retarding the self-diffusion of Cu through process-related changes. One method is the alloying of the Cu interconnect, and another is the replacement of the dielectric cap on the Cu surface with a metal cap. Both methods will be highlighted in this article.

Simultaneously, the need to lower capacitance in the interconnect system in order to further decrease RC-delay has motivated the implementation of low-*k* inter-level dielectric (ILD) materials in place of the traditional SiO_2-based material [2] (Fig. 2).

Low-*k* materials are usually more compliant than SiO_2-based materials, and also require new processing methodologies. The impact of low-*k* ILD on electromigration will also be discussed.

In addition to understanding the relationship between electromigration and processing, another important aspect of electromigration is the accurate assessment of lifetime extrapolations, in which data taken at experimental conditions are scaled back to use conditions. We will review the use of the well-established Black's

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doi:10.1016/j.microrel.2003.10.020

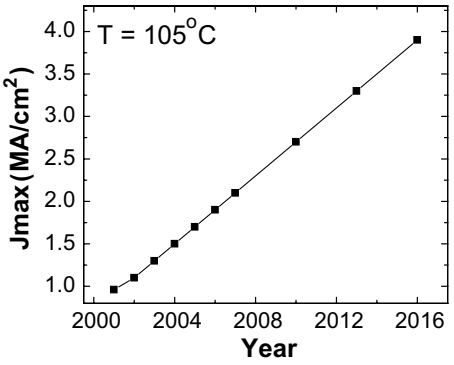

Fig. 1. The required current density at operating conditions continues to rise with time as depicted by the International Technology Roadmap for Semiconductors, 2002 edition [2].

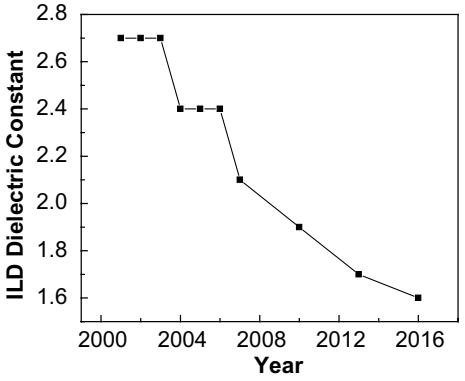

Fig. 2. The minimum effective dielectric constant needed for the continuous decrease in RC-delay, as depicted by International Technology Roadmap for Semiconductors, 2002 edition [2].

Law for lifetime extrapolations as well as reliability assessments of more complex interconnect geometries.

2. Basic electromigration physics

The electric field applied across an interconnect during operation biases the net motion of metallic ions in the direction of electron flow (i.e., from cathode to anode). This net flux of atoms is caused by electromigration, which can be described as the self-diffusion of metallic ions in response to an electric field. The atomic flux is mainly the result of two opposing driving forces: the electron wind force moving the ions in the direction of the electron flow and a back stress that pushes the ions in the opposite direction. The atomic flux (J) can be described by the following equation [5]:

$$J = -\frac{DC}{kT}\left(Z^* eE - \Omega\frac{\partial\sigma}{\partial x}\right), \quad (1)$$

where D is the diffusivity, C is the concentration of atoms, k is Boltzmann's constant, T is temperature, Z^* is the effective charge number, e is the fundamental electronic charge, E is the electric field, Ω is the atomic volume, and $\partial\sigma/\partial x$ is the stress gradient along the line.

Electromigration is a reliability concern because it can lead to interconnect failure, where failures occur at sites of atomic flux divergence, that is, where the net flux of atoms is not zero. At sites where there is a net depletion of atoms, local stresses become increasingly tensile, which can eventually lead to voiding in the interconnect once a critical tensile stress value is reached (σ_{crit}) [6] (Fig. 3), which can subsequently lead to failure by open circuit. In the case of interconnects clad in refractory layers or liners, the electric current can shunt through these layers once a void has formed in the interconnect, which will lead to a resistance increase. This increase can become unacceptably high, at which point the interconnect is considered failed. At sites where there is a net accumulation of atoms, the local stresses become increasingly compressive, which can lead to the formation of metallic extrusions (Fig. 4). A failure by short circuit may result if the extruded metal touches a neighboring interconnect or via.

2.1. The Korhonen model

The stress evolution associated with electromigration in confined metal lines has been described by a model developed by Korhonen et al. [6] In order to find an expression for the stress-evolution in a line during elec-

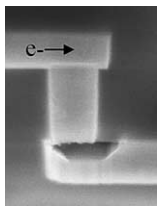

Fig. 3. An example of electromigration-induced voiding, which can lead to interconnect failure by open circuit [7].

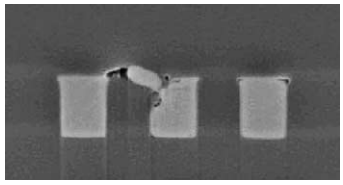

Fig. 4. An example of electromigration-induced extruding, which can lead to interconnect failure by short circuit [8].

tromigration, a relation between the local stress and atomic concentration in the line is needed:

$$\frac{dC}{C} = \frac{-d\sigma}{B}, \tag{2}$$

where B is the effective modulus of the metal–dielectric composite.

By substituting into the continuity equation in the line direction, that is:

$$-\frac{\partial J}{\partial x} = \frac{\partial C}{\partial t} + \left(\frac{C}{B}\right)\frac{\partial \sigma}{\partial t}, \tag{3}$$

where ∂C has been substituted from Eq. (2), we can arrive at a partial differential equation describing the stress evolution along the interconnect line due to electromigration:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{DB\Omega}{kT}\left(\frac{\partial \sigma}{\partial x} + \frac{Z^* eE}{\Omega}\right)\right], \tag{4}$$

where all symbols have been previously defined. A more detailed derivation of the one-dimensional Korhonen model can be found in other references [6,9,10].

Without simplifying assumptions, this model can not be solved analytically. Therefore, numerical simulators have been developed to model the stress evolution due to electromigration using the Korhonen equation (Eq. (4)) [9]. An example of the stress-evolution during electromigration in a simple straight-line interconnect terminating in no-flux vias is shown in Fig. 5.

2.2. Electromigration in Al- vs. Cu-based interconnects

The atomic flux induced by an electromigration driving force is a function of the diffusivity (D) as seen in Eq. (1). This diffusivity is a weighted sum of the atomic diffusivities of all diffusion paths in the interconnect, and is different for the current Al and Cu interconnect technologies due in part to differences in their integration schemes. Al-based interconnects are fabricated through thin film deposition, which often includes a Ti and/or TiN under- and overlayer which sandwich the Al. The underlayer serves as an electrical shunt while the overlayer serves as an electrical shunt and as well as an anti-reflective coating (ARC) layer. After deposition, the stack is etched and passivated with an ILD material such as SiO_2 (Fig. 6a). The resulting primary diffusion paths are: bulk, metal/over- or underlayer interface, metal/sidewall interface, and grain boundary. Because the diffusivities along the two types of interfaces (i.e., metal/over- or underlayer and metal/sidewall interfaces) were found to be about equal [12,13], an expression for the product of Z^* and D for a passivated, subtractively-etched structure can be written as:

$$Z^*D = Z^*_B n_B D_B + 2Z^*_I D_I \delta_l (1/w + 1/h) + Z^*_{GB} \sum_j^n D_{GBj}(\delta_{GBj}/d), \tag{5}$$

where the subscripts B, I, and GB refer to the bulk, interface, and grain boundary, respectively; δ_I and δ_{GB} are the width of the interface and grain boundary, respectively; d is the grain size, w is the line width, h is the line thickness, and n_B, $2\delta_l(1/w + 1/h)$, and (δ_{GB}/d) are

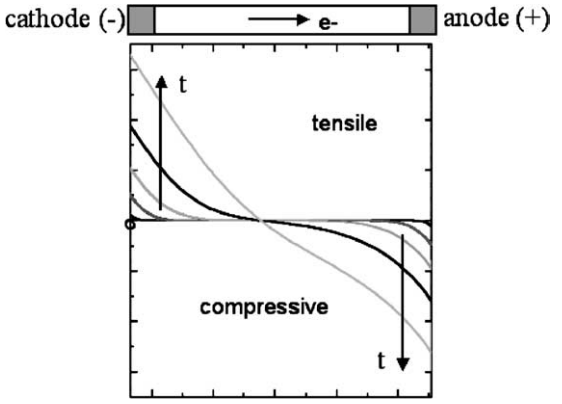

Fig. 5. The stress evolution during electromigration in a straight-line interconnect terminating in no-flux vias [11].

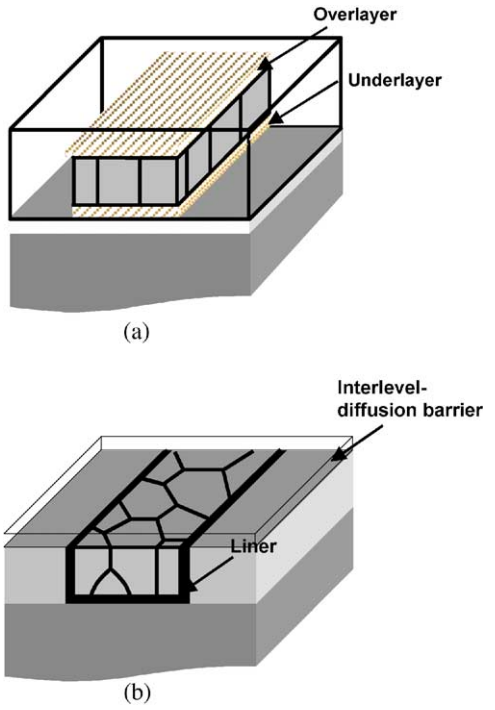

Fig. 6. Schematic cross sections of (a) a subtractively-etched, passivated line with underlayer and overlayer, and (b) a Damascene line with liners on three Cu/trench interfaces and an interlevel-diffusion barrier.

the fractions of atoms diffusing through the bulk, interface, surface, and grain boundary of the line, respectively.

In contrast to Al-based interconnects, Cu-based interconnects are fabricated through a Damascene process. Here, trenches and holes are etched into the ILD and lined with a Ta-based barrier layer and Cu seed. Next, Cu is electroplated into the openings, after which the Cu and barrier over-burden are removed through chemical–mechanical-polishing (CMP). Once the over-burden is cleared from the field, the exposed Cu surface is capped. The typical Cu-cap is a SiN-based dielectric, which serves as an inter-level diffusion barrier (Fig. 6b). This process is referred to as dual Damascene when the trench and via are processed together. The resulting set of primary diffusion paths in this interconnect system is: bulk, metal/liner interface, metal/inter-level diffusion barrier interface, and grain boundary. Analogous to Eq. (5), an expression for the product of Z^* and D for a Damascene structure can be written as a weighted sum of all diffusion paths in this interconnect system [14]:

$$Z^*D = Z^*_{\mathrm{B}} n_{\mathrm{B}} D_{\mathrm{B}} + Z^*_{\mathrm{I}} D_{\mathrm{I}} \delta_{\mathrm{I}} (2/w + 1/h) + Z^*_{\mathrm{S}} D_{\mathrm{S}} \delta_{\mathrm{S}} / h + Z^*_{\mathrm{GB}} \sum_j^n D_{\mathrm{GB}j} (\delta_{\mathrm{GB}j}/\mathrm{d}), \quad (6)$$

where the subscripts B, I, S, and GB refer to the bulk, metal/liner interface, metal/inter-level diffusion barrier surface, and grain boundary, respectively; δ_{I}, δ_{S}, and δ_{GB} are the width of the interface, surface and grain boundary, respectively; d is the grain size, w is the line width, h is the line thickness, and n_{B}, $\delta_{\mathrm{I}}(2/w + 1/h)$, δ_{S}/h, and $(\delta_{\mathrm{GB}}/\mathrm{d})$ are the fractions of atoms diffusing through the bulk, interface, surface, and grain boundary of the line, respectively.

It has been well established that microstructure plays a dominant role in determining the reliability of Al-based interconnects [15–18] due to the dominance of grain boundary diffusion (D_{GB}) over interface (D_{I}) and bulk diffusion (D_{B}) (Eq. (5)). An interconnect with a bamboo microstructure (Fig. 7a) only has grain boundaries whose planes are normal to the direction of current flow, so that electromigration occurs via slower

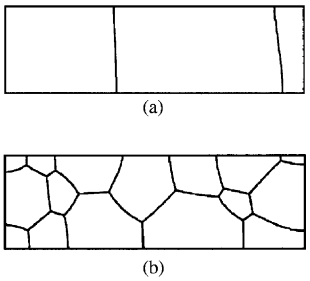

Fig. 7. Interconnect segments with (a) bamboo and (b) polygranular microstructures.

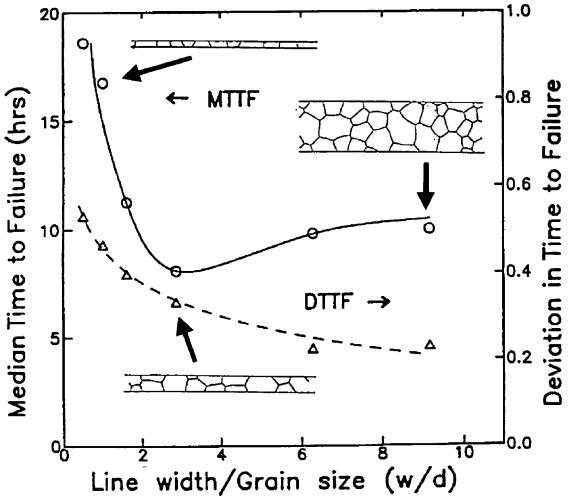

Fig. 8. The dependence of electromigration lifetime on microstructure in Al-based interconnects [15].

surface diffusion, resulting in increased electromigration lifetimes. Interconnects with polygranular microstructures (Fig. 7b), on the other hand, have decreased electromigration lifetimes since many grain boundary planes have a component lying in the direction of the electron flow, so that grain boundaries provide the primary fast diffusion paths for electromigration. Fig. 8 illustrates the effect of microstructure on the electromigration lifetime of Al interconnects.

In contrast to Al-based interconnects, it has been shown that microstructure does *not* play a dominant role in the electromigration of today's Cu-based interconnects [19,20]. Rather, the top surface of the Cu is currently the fastest diffusion path [21–24] (i.e., Ds $\gg$ Dgb.) Specifically, it has been shown that, unlike Al, changing the width of the Cu interconnect while maintaining the same test current density and temperature does not significantly alter the resulting lifetime, thereby indicating that the top surface is the dominant diffusion path (see Eq. (6)). These studies suggest that the reliability of Cu interconnects can be improved through the suppression of surface diffusion, so that the condition of the top interface of the Cu plays a key role on electromigration reliability. Once the Cu diffusion along the top surface is sufficiently slowed, grain structures or interface boundaries should affect the reliability of Cu interconnects.

3. Electromigration and process

Electromigration reliability is highly sensitive to the processing of the interconnect stack. Two approaches for increasing the robustness of Cu electromigration failure through processing will be discussed: alloying the

Cu and replacing the traditional dielectric cap with a metal cap.

3.1. Alloying

More than 30 years ago, it was demonstrated that doping Al interconnects with Cu leads to marked increases in electromigration lifetimes [25] (Fig. 9), which has been attributed to the Cu dopant coating the grain boundaries and triple points, thereby retarding electromigration [26,27]. The alloying of Cu is more recently being studied.

Ideally, the alloy of choice should lead to enhanced electromigration robustness by segregating to the fast diffusion path without significantly increasing the interconnect resistance. Also, the alloy should not be a device killer or hazardous. Other desirable features of an alloy specific to Cu include: formation of a continuous surface layer that bonds well to the dielectric as well as interaction with barrier materials [28,29].

Several methods for doping the Cu interconnect with alloy have been published. One method is based on an alloyed Cu seed in which a thin PVD Cu-seed is deposited on the Cu barrier to provide a conductive surface for subsequent Cu-fill using electroplating, after which an anneal is performed in order to drive the alloy out of the seed and into the trench and vias [29] (Fig. 10). Other methods for alloying the Cu include ion implantation of the Cu surface [30] and co-electrodeposition [31].

Many alloying elements have been investigated on Cu structures, including: Al [32], Cr [33], Mg [34], Pd [35], Sn [29,36,37], and Zr [38]. Of these, CuSn in particular has been shown to lead to marked improvements in electromigration lifetimes in both drift structures [36] (Fig. 11) as well as two-level electromigration structures [29] (Fig. 12). Both studies showed that increased Sn amounts lead to proportionally slower electromigration rates. One potential downfall of doping Cu interconnects with Sn is the significant increase in line resistivity,

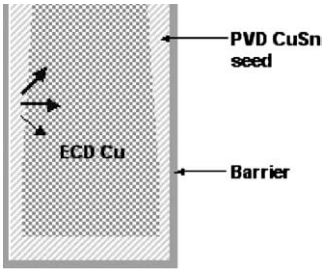

Fig. 10. A method for doping the Cu interconnects has been developed, which involves depositing a doped-Cu seed layer, after which an anneal step drives the dopant into the Cu trench and vias [29].

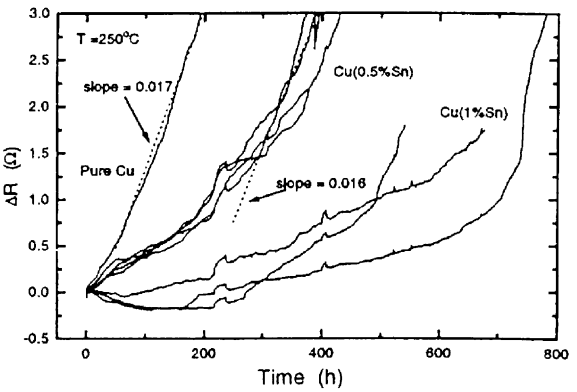

Fig. 11. Significant retardation in resistance increase during electromigration due to the addition of Sn to Cu were observed in drift experiments [36].

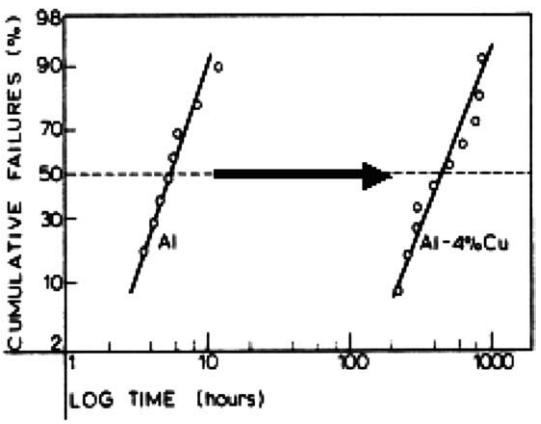

Fig. 9. Two-orders of magnitude increase in electromigration lifetime due to the doping of Al interconnects with Cu has been reported [25].

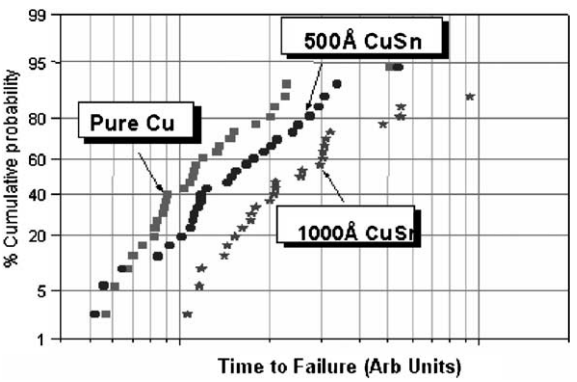

Fig. 12. Lifetime improvements due to the addition of Sn to Cu interconnects were measured in two-level electromigration structures [29].

which would increase RC-delay. To address this, it was shown that the resistivity of CuSn can be controlled not only by the dopant concentration, but also by the subsequent anneal step(s) where resistance decreases with anneal time to a finite value [29].

3.2. Metal cap

Since the top Cu surface of today's interconnects has been shown to be the fastest diffusion path, considerable effort has been made to alter this interface in order to increase electromigration robustness. For example, different refractory materials, such as SiN and SiC [39] have been investigated as the dielectric cap material. Also, different process treatments prior to the deposition of the dielectric cap has been investigated [40]. Both approaches were found to affect the resulting electromigration behavior. Another promising approach to improve electromigration behavior is the implementation of a metal cap. Desirable properties of a new cap material include: protection of Cu from oxidation, suppression of hillock formation during annealing, and improved adhesion. Electroless CoWP is a candidate cap material as it has been shown to have desirable properties such as low thin-film resistivity and excellent conformality [41–43].

Electromigration studies of Cu interconnects with a selective electroless metal coating of CoWP, CoSnP, or Pd on the top surface of Cu Damascene lines have been shown to significantly improve electromigration lifetime [44] (Fig. 13). Here, the time to a given resistance increase of the metal-capped material was about 10× longer than that of SiN_x-capped samples at the test conditions used in this study. While the authors acknowledge that this mechanism is not clearly understood, they do speculate that the electroless metal cap changes the interface bond strength and reduces of

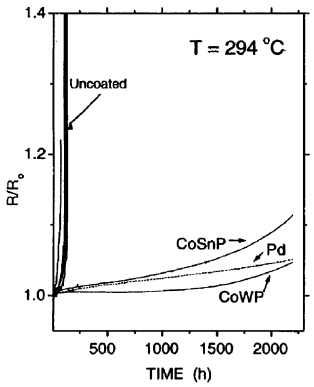

Fig. 13. Tremendous retardation in resistance increase during electromigration testing (or tremendous gains in lifetime) were measured for electroless metal-capped Cu samples relative to SiN_x-capped Cu samples [44].

mobility of Cu atoms by pinning. It has also been shown in a separate study that replacing the traditional hard-mask with a *W* cap reduces interconnect delay due to the lowered effective dielectric constant to as much as 15% where the effect is most pronounced in interconnect systems with low-*k* ILD [45].

4. The effect of ILD on CU electromigration

As dimensions scale beyond the 130 nm technology node, the need to lower capacitance for decreased RC-delay in the interconnect system has motivated another major materials change in the interconnect system: the implementation of low-*k* ILD materials in place of the traditional SiO_2-based material. In addition to a low dielectric constant, ILD materials must also possess high thermal and mechanical stability, good adhesion to other interconnect materials, resistance to processing chemicals, low moisture absorption, and low cost [46]. A general challenge for developing suitable low-*k* materials is obtaining a combination of a low dielectric constant and good thermal and mechanical properties, where the basic difficulty is that the strong chemical bonds that impart structural stability are also the most polarizable, which leads to a high dielectric constant [47].

A key concern relevant to the implementation of low-*k* materials is how it will impact interconnect reliability. To appropriately address this issue with respect to electromigration, we believe that several factors need to be considered. These factors are: the effect that low-*k* ILD will have on drift velocity, the rate at which stresses buildup in the line, and the critical stress change to void nucleation ($\Delta\sigma_{crit}$). It has been reported that surrounding the Cu interconnect with low-*k* materials leads to faster mass transport during electromigration due to degraded thermomechanical properties, such as interfacial adhesion [48], which would shorten electromigration lifetimes. It has also been shown that because the implementation of a low-*k* ILD leads to a lower effective modulus, *B*, of the interconnect system, the stress buildup at vias is slower [6,49], which would lengthen electromigration lifetimes. Thirdly, the critical stress change to void nucleation ($\Delta\sigma_{crit}$), which is the absolute stress difference between the initial stress state of the line and a critical stress that leads to void nucleation, is highly sensitive to processing details. For instance, studies have shown that $\Delta\sigma_{crit}$ varies from process-to-process even when the same materials and integration schemes are used [7,50]. Considering these three factors together, it is difficult to make a general claim about how low-*k* ILD materials affect electromigration behavior since some factors are competing, while another factor is strongly process-dependent. Consistent with this, studies have shown a degradation in lifetime and E_A as the dielectric constant decreases [48], while other studies have shown

that when a process is fully optimized, low-k ILD samples can lead to similar lifetimes as SiO_2-based samples [51]. Therefore, the electromigration robustness of a given ILD material needs to be assessed by explicit measurement.

5. Electromigration lifetime extrapolation

In practice, electromigration reliability assessments are often based on tests conducted at accelerated conditions (i.e., high temperatures and current densities), which are then scaled back to use conditions (Fig. 14). These extrapolations determine whether a technology is reliable enough against electromigration failure for a given specification, or whether further optimization in process and/or design is needed. The extrapolation is commonly based on Black's Law [52], which expresses the median time to failure (MTF), or 50th percentile fail time of a failure population, as:

$$\mathrm{MTF} = A\left(\frac{1}{j}\right)^{n} \exp\left[\frac{E_A}{kT}\right], \tag{7}$$

where A is an empirically-determined constant, j is the current density, n is the current density exponent, E_A is the activation energy to electromigration failure, and k and T have been previously defined.

The figure of merit for electromigration reliability is the use current density, which is commonly denoted as j_{use} or j_{max}, and represents the maximum current density the interconnect system can maintain while still guaranteeing a certain failure rate over a certain amount of operation time at use conditions. To determine this value, a ratio of Black's Law (Eq. (7)) between use and test conditions can be employed for extrapolation:

$$\frac{\mathrm{TTF}_{use}}{\mathrm{MTF}_{test}} = \left(\frac{j_{test}}{j_{use}}\right)^{n} \exp\left[\frac{E_A}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)\right] \exp[-N\sigma], \tag{8}$$

where TTF_{use} is the time to failure at use conditions and represents the required lifetime of the product, MTF_{test} is the median time to failure at accelerated test conditions, j_{test} is the test current density, T_{test} is the test temperature, T_{use} is the use temperature, N is a constant that relates MTF with a time-to-failure at a different fail percent and is determined by product specifications, σ is the deviation in time to failure, and j_{use}, n, E_A and k have been previously defined. Additionally, the expression $\exp[-N\sigma]$ as seen in Eq. (8) relates the median time to failure to a different failure percent. By rearranging Eq. (8), an expression for j_{use} can be written as:

$$j_{use} = j_{test} \cdot \left[\frac{\mathrm{MTF}_{test}}{\mathrm{TTF}_{use}} \cdot \frac{1}{\exp\left[\frac{E_A}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)\right] \exp[-N\sigma]}\right]^{1/n}. \tag{9}$$

The key parameters that affect the extrapolated electromigration reliability as shown in Eq. (9) will be discussed in the following sections.

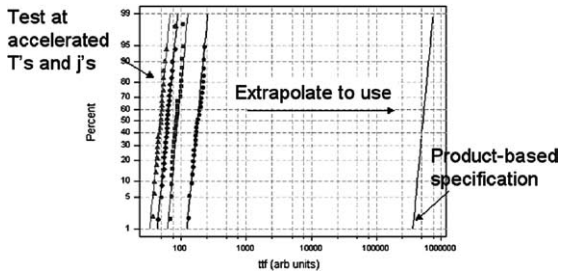

Fig. 14. Lifetime collected from accelerated tests need to be extrapolated to use conditions, which are typically at lower temperatures and current densities [11].

5.1. The effect of N

N specifies the failure percent to which the reliability of the interconnects must be guaranteed for a given use condition, and is determined by product specifications. A higher value of N corresponds to a lower failure percent, and thus a more stringent failure criterion. As examples of relating N to the standard normal cumulative distribution, a "3σ" extrapolation (or $N = 3$) corresponds to a cumulative failure percent of 1e−1%, while a "6σ" extrapolation (or $N = 6$) corresponds to a cumulative failure percent of 1e−7%.

5.2. The effect of sigma

The parameter σ is the inverse slope of a lognormal distribution and describes the spread in failure times. σ plays a strong role on extrapolation where, as seen in Eqs. (8) and (9), a higher σ leads to exponentially lower extrapolated failure times. This relationship can be seen graphically in Fig. 15, which depicts two distributions with similar MTFs, but different σ's, where $\sigma_1 > \sigma_2$. The adverse of effect of a high σ becomes more pronounced at lower failure percents (or higher N).

5.3. The effect of activation energy

The activation energy, or E_A, represents the energy barrier against the diffusive process resulting in electromigration and has an exponential relationship with electromigration lifetime so that increases in E_A are highly desirable. It has been shown that the value of E_A can represent different diffusion paths [53] (Table 1). Values of E_A for today's Cu Damascene interconnects as

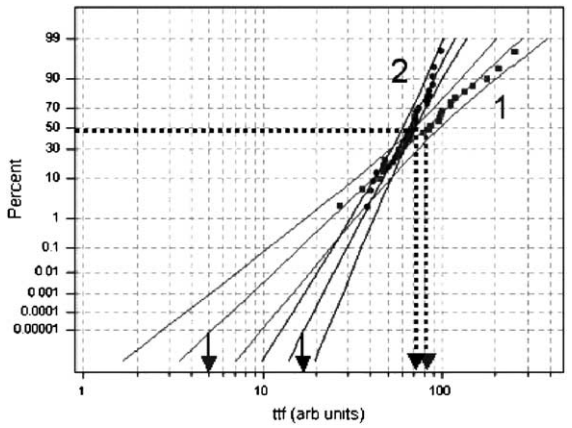

Fig. 15. Larger sigma values lead to lower extrapolated failure times at low fail percents, even when median to failures are comparable [11].

Table 1
Different activation energies are associated with different diffusion paths in Cu-based interconnects [53]

Diffusion path	E_A (eV)
Bulk Cu	2.2
Dislocations	1.2–1.5
Grain Boundaries	0.88–0.95
Surface	0.8–0.9

quoted in literature typically fall in the range of 0.8–1.0 eV [48,50,51,54,55].

5.4. The effect of current density exponent (n)

It has been established through studies on Al interconnects that void-growth-limited failure is represented by a current density exponent of 1 [56], while void-nucleation-limited failure is represented by an exponent of 2 [6,57]. These concepts appear to be consistent in Cu interconnects where correlations were made between n-values and failure analysis [7]. That is, a failure resulting from a void that nucleates directly under the via may be void-nucleation-limited (Fig. 16a), whereas that resulting from a void that nucleates just downstream from the via but does not immediately uncover the via may be void-growth-limited (Fig. 16b).

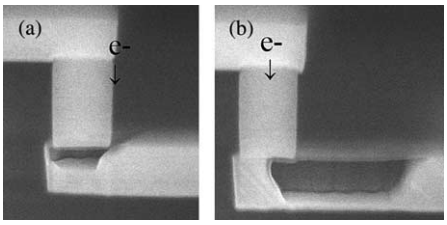

Fig. 16. Two types of void configurations were observed for one population of long-lines. (a) One group indicates void-nucleation-limited failure while (b) the other group indicates void-growth-limited failure [7].

The impact of n on lifetime extrapolation depends on the relative magnitudes of the test and use current densities (j_{test}/j_{use}), as seen by applying a ratio to Black's Law (Eq. (8)). It can be stated, however, that a higher value of n increases the sensitivity of current density on the resulting extrapolated failure time [7].

5.5. The effect of T_{use}

It should also be noted that j_{use} is strongly dependent on the operation temperature, T_{use}. For example, a 5 °C decrease in operation temperature can lead to about 25% increase in j_{use} when assuming typical values of T_{use}, E_A and n (i.e., 105 °C, 0.9 eV and 1.5, respectively). Because of this, careful assessments of the substrate temperature and Joule heating are needed for accurate reliability assessment.

5.6. Bimodality

The lifetime distributions discussed thus far have been monomodal, i.e., all failure times falling on a single lognormal distribution. However, bimodal distributions have also been observed in which the fail times fall on two different lognormal distributions. These distributions require separate analysis for each mode, so that E_A and n can be determined for each mode [58–60]. Previous studies have reported that "early" failure modes were found to have not only smaller failure times but also a lower current density exponent, but similar activation energies [60].

6. EM assessments on complex interconnect systems

Electromigration studies are typically conducted on simple straight-line interconnects terminating in no-flux vias. However, laid-out integrated circuits often have interconnects with much more complex geometries, which include junctions and segments of varying widths and lengths. In carrying out circuit-level reliability assessments, it is important to be able to assess the reliability of these more complex shapes.

6.1. Short-line behavior

It has been well established that the back stress force becomes stronger at lower current densities (j) and line lengths (L). Based on this phenomenon, it has been established that a critical current density and line length product $(jL)_{crit}$ exists for both Al-[5] and Cu-based [48,50,61–63] interconnects below which electromigra-

tion ceases and the interconnect is immortal. The critical current density and line length product is defined as [5]:

$$(jL)_{\text{crit}} = \left(\frac{\Omega \Delta \sigma_{\text{crit}}}{Z^* e \rho}\right), \tag{10}$$

where ρ is the resistivity of the metal, and all other symbols have been previously defined. The stress profile for lines that are immortal to electromigration failure have reached steady state, as depicted in Fig. 17. Because the behavior of short lines can differ from that of long lines, it is important to accurately assess short-line effects when assessing the electromigration reliability, especially from a full-chip perspective.

Recent studies have shown that different regimes of MTF exist as a function of jL [7,51]. That is, at high values of jL when back stress is insignificant ($jL \geqslant 5000$ A/cm), MTF was relatively constant for the range of current densities used in the study. At intermediate values of jL, MTF rapidly increases with decreasing jL due to increasing back stress. Below a critical jL value of about 1500 A/cm, a regime of immortality was observed for all Cu/SiO_2-based interconnects tested in this regime. The critical jL value corresponds to a maximum stress difference in the interconnect necessary for void nucleation ($\Delta\sigma_{\text{crit}}$) to be at least 100 MPa. Failure analysis of these immortal samples revealed that no voids had formed anywhere in the test structure.

Other short-line studies on SiO_2-based ILD have shown a probabilistic characteristic of immortality [50]. That is, a small percentage of lines always failed, even at low jL-conditions so that 100% immortality was never achieved. Failure analysis of these structures revealed that voiding was present in every line tested including those that did not fail. It was further observed that voids that nucleated directly beneath the via would lead to failure, while voids that nucleated somewhat downstream from the via but were tested at low enough jL conditions did not lead to failure. This study reports a $\Delta\sigma_{\text{crit}}$ value of 50 MPa, which is about half of the value mentioned in the previous study, and may explain the consistent presence of voiding. Since both studies were conducted on samples with SiO_2-based ILD, the discrepancy in $\Delta\sigma_{\text{crit}}$ may indicate differences in the quality of the Cu/nitride-cap interface.

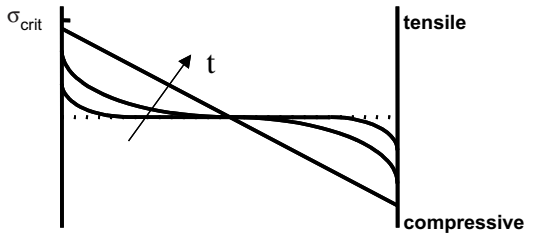

Fig. 17. The stress profile along the interconnect evolves to a straight-line at steady state.

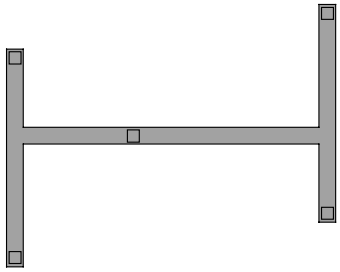

Fig. 18. An example of an interconnect tree, which is defined to be a continuously connected piece of metal within one layer of metallization which is bound by diffusion barriers [65].

6.2. Interconnect trees

Interconnect trees have been defined to be a continuously connected piece of metal within one layer of metallization which is bound by diffusion barriers, and have been proposed to be a fundamental reliability unit [64–67]. An example of an interconnect tree is shown in Fig. 18. Unlike traditional approaches, these studies do not assume that different parts of the trees are independent of each other since material can diffuse freely

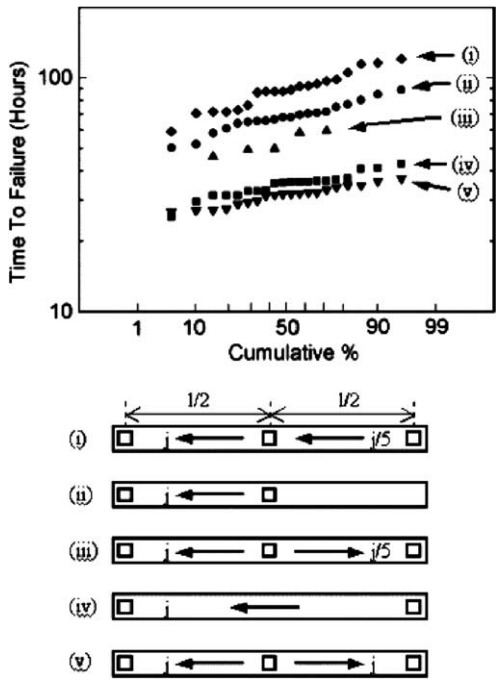

Fig. 19. The lognormal distributions of electromigration lifetimes vary depending on the current direction and magnitude for the same interconnect tree structure [65].

within a tree, thereby coupling the stress evolution in different parts of the tree. This concept has been identified through experimental and modeling studies on both Al- and Cu-based interconnect trees in a "dotted-i" configuration in which the lifetimes of segments within an interconnect tree are strongly affected by the magnitude and direction of current flowing in adjacent limbs or segments [66,67] (Fig. 19). To address this, electromigration models based on nodal reliability analyses have been developed for estimating the reliability of arbitrary interconnect trees, by estimating the times to void nucleation, void growth to failure, and formation of extrusions, using current density information for all segments connecting at the node [65].

7. Conclusions

This article has reviewed key aspects of Cu electromigration, which has proven to be a major reliability concern in today's integrated circuits. We have given a basic review of electromigration physics as well as a comparison between the electromigration behavior of Al and Cu interconnects, in which the difference in processing schemes was emphasized. The close relationship between processing and electromigration reliability has been highlighted in our discussion concerning alloying and metal caps, where promising results leading to significantly enhanced electromigration robustness have been published. We also discussed the implications of low-k ILD materials on Cu electromigration reliability. Next, we reviewed the methodology for electromigration extrapolation and explained the impact of the key statistical parameters. Finally, the reliability assessment of more complex interconnects was discussed.

Acknowledgements

The author would like to thank Stefan Hau-Riege (LLNL) and Amit Marathe (AMD) for their careful readings of this manuscript. The author would also like to thank Connie Wang (AMD) and Todd Ryan (AMD) for useful discussions.

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