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Microstructural impact on electromigration reliability of gold interconnects ☆

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ABSTRACT

Interconnect segments of gold metallization used for GaAs devices are susceptible to significant electromigration degradation and have a microstructure with thousands of grains. In this work, a complete physics-based analysis of electromigration in gold is presented. A novel approach for the numerically efficient simulation of an interconnect containing a large number of grains is introduced. By building grain compounds containing hundreds of grains and equipping them with appropriate models, the dependence of statistical failure features on the variation of geometric properties is investigated. The experimentally observed dependence of the mean failure time and the associated standard deviation of the failure times on the interconnect geometry is well reproduced by our simulations.

1. Introduction

Simulating the influence of microstructure on the electromigration (EM) reliability of a metallic interconnect is a challenging task for two main reasons: firstly, because of the complexity of the vacancy behavior within and near grain boundaries; and secondly, because of the large number of grain boundaries. In some applications the nano-scale of the interconnect width causes the emergence of larger grains extending through the whole interconnect width. The presence of large grains significantly simplifies modeling of the microstructural impact. However, in the case of gold interconnects used for GaAs [1,2] technology we have to deal with a significant number of small grains (~10) through the whole depth of the interconnect. Gold is the metal of choice for interconnects implemented on GaAs, because it forms an contact with very low resistance, has a high melting temperature, and a low parasitic resistivity [3].

2. Motivation and objective

In the recent study on EM reliability of interconnects made of gold by Hau-Riege and Yau [4] the relevant segments of metallization contained several thousands of grains. The current density of 10 mA/μm^2 and the temperature of 361 °C [4] are used as test conditions in a modular integrated reliability analyzer (MIRA) EM test system [2]. The gold interconnect, consisting of two metallization levels, M1 and M2, and the via was fully embedded in a dielectric (silicon nitride, SiN). Several types of test structures have been used, cf. Fig. 1. Two failure modes were observed: (a) voiding at the M1/Via interface and (b) voiding through the thickness of M2 at the Via/M2 interface. The resistance variability and time-to-failure distribution are determined by specific features of the gold microstructure. The study documented, how the MTTF and the standard deviation behave as a function of via size. The objective of this work is to investigate the physical mechanism behind the failure development and the influence of the gold microstructure and the geometric features of the interconnect.

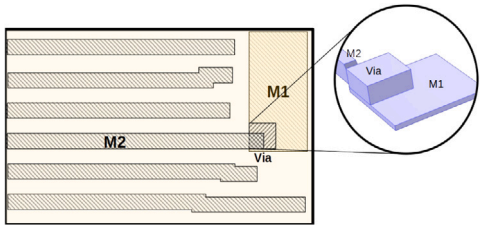

Fig. 1. Layout of the line-end of the investigated test structures.

3. Modeling and simulation

In COMSOL [5], the EM model can be assigned to each grain or to groups of grains fully taking in account the local material properties, like diffusivity, elasticity parameters, and crystal orientations, cf. Fig. 2. Each of the entities consisting of a single, or of a multitude of grains is separately meshed, cf. Fig. 3. We introduce in this work a

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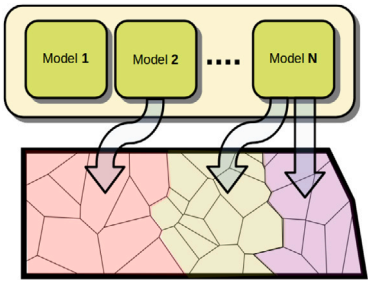

Fig. 2. Schematic picture of the overall modeling approach. From the model library of N configured models two models are chosen and assigned to the three different grain compounds.

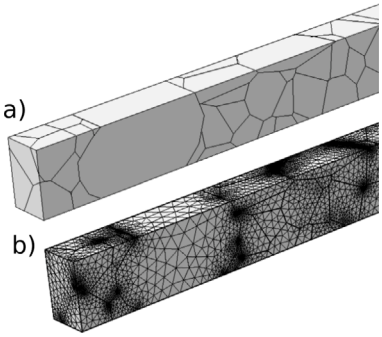

Fig. 3. Example of a multigrain domain (a) without and (b) with a finite element mesh.

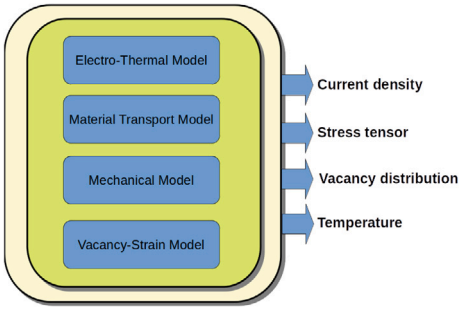

Fig. 4. Schematic representation of the model used for simulation.

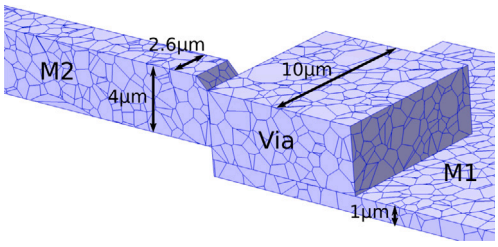

Fig. 5. An example of microstructure used for simulation. M2, via, and M1 are filled with a grain boundary network.

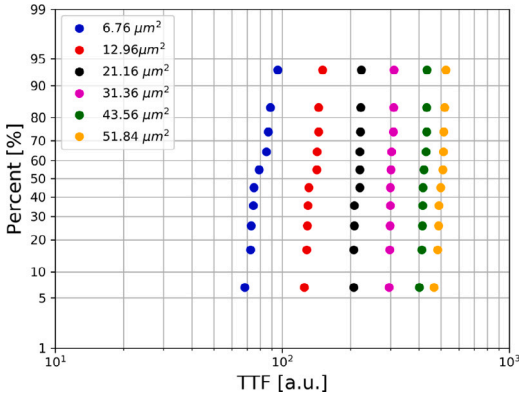

Fig. 6. Lifetime distribution for different via sizes.

novel approach for the numerically efficient simulation of an interconnect containing thousands of grains. A number of grains are grouped into larger grain compounds and at the boundaries of these domains a detailed grain boundary model is applied [6]. The boundaries of the large grain compounds are chosen to comprise characteristic segments of the interconnect geometry, e.g. vias. Alternatively, these segments can also be divided into several grain compounds. The size statistics of the grain compounds are set according to the experimentally obtained statistics of the grain size distribution. Inside the compounds the effective diffusivity (D_{eff}) is calculated as a weighted sum of contributions from the grain bulk (D_{bulk}) and from the grain boundaries (D_{gb}).

$$D_{\text{eff}} = D_{\text{bulk}} + \delta \frac{\sum_i S_i}{\sum_j V_j} D_{\text{gb}} \tag{1}$$

δ is the grain boundary width and S_i and V_i are the grain boundary surfaces and volumes, respectively. The summation is performed along all the grains contained in a compound. The vacancy fluxes driven by the concentration gradient ($\vec{J}_v^c$), by the EM ($\vec{J}_v^e$), by the pressure gradient ($\vec{J}_v^s$), and by the temperature gradient ($\vec{J}_v^T$) are proportional to the effective diffusivity, and the vacancy concentration (C_v) obeys the balance equation [6].

$$\vec{J}_v = \vec{J}_v^c + \vec{J}_v^e + \vec{J}_v^s + \vec{J}_v^T, \quad \frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J}_v + G_{\text{eff}}(C_v) \tag{2}$$

The simulation based on the model Eqs. (2) provides as output, for an arbitrary multilayer interconnect geometry and for given initial and boundary conditions, cf. Fig. 4, the temperature distribution, the current density distribution, the tensorial mechanical stress field, and the point defect (vacancy) distribution. These values enable the determination of the interconnect lifetime. The model used for simulation is implemented in COMSOL Multiphysics utilizing the concepts of *physics interfaces* and *PDE interfaces* [5] which both consist of nodes and settings that set up the equations and variables for specific areas of physics. The COMSOL physic interfaces used for the realization of electro-thermal model (cf. Fig. 4) are *electric currents* and *heat transfer in solids*. For the material transport and vacancy-strain model the PDE interface *coefficient form PDE* is configured and applied, and for the mechanical model the *solid mechanics* physics interface is utilized. Further details on the applied EM model are provided in previous publication [7].

4. Simulation results

Our simulation approach is utilized to study the results published by Hau-Riege and Yau [4]. The polycrystalline background microstructure is generated with the NEPER [8]. All three segments of the interconnect, M1, Via, and M2 are filled with a numerically generated network of grain boundaries, cf. Fig. 5. The microstructural characterization measurements carried out in [2] have revealed that the gold microstructure has a median grain size of 0.95 µm and a standard deviation of 0.3 µm. In Fig. 6 the simulated lifetime distributions for six different via sizes are presented. As one can see, all distributions are lognormal and monomodal in agreement with the experiments [4]. Additionally, the experimentally observed dependence of the mean failure time, cf. Fig. 7, and the associated standard deviation, cf. Fig. 8, of the failure times on the interconnect geometry is also well reproduced

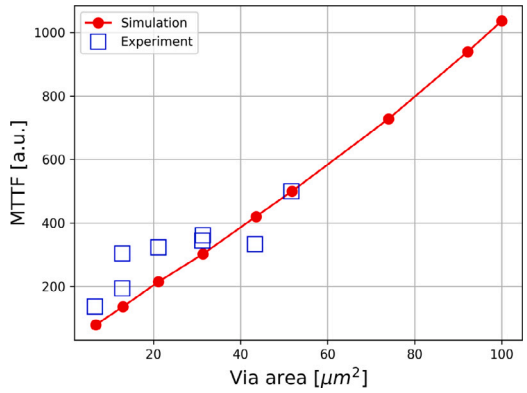

Fig. 7. MTTF for different via sizes The maximal value of the MTTF is adjusted to the experimental value from [4].

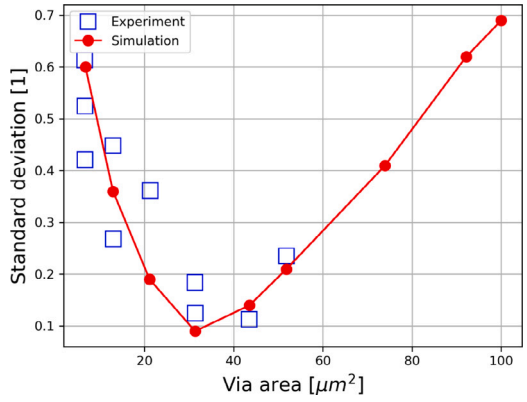

Fig. 8. Standard deviation for different via sizes. The maximal value of the standard deviation is adjusted to the experimental value from [4].

by our simulations. In order to further investigate the model behavior, we have performed simulations for three more via surfaces up to the 100 μm^2. An explanation for an increased MTTF for larger via sizes is that due to a larger reservoir of atoms and wider via surface the stress build up is slower. The corresponding standard deviation, displayed in Fig. 8, however, reduces up to a via surface of 31.36 μm^2, and then increases towards the via surface of 51.84 μm^2. The reduction in the standard deviation is expected as a consequence of the lesser influence of the microstructure for larger vias and its subsequent increase is a phenomenon which originates in the accumulation of the standard deviation [9].

5. Conclusion

We applied state-of-the-art electromigration modeling to study the evolution of electromigration degradation of gold interconnects. The model accounts for previously experimentally determined statistical properties of gold. As observed in the experimental reliability study, the MTTF increases with an increasing surface of the via, while simultaneously, the standard deviation exhibits both, a decreasing as well as an increasing phase. This behavior is consistently reproduced by our simulations results.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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