Pergamon

PII: S0026-2714(96)00268-5

Microelectron. Reliab., Vol. 37, No. 7, pp. 1053–1072, 1997

0026-2714/97 $17.00 + 0.00

ELECTROMIGRATION: A REVIEW

D. G. PIERCE†
Sandia National Laboratories, MS 1081, Albuquerque, NM 87185, U.S.A.

and

P. G. BRUSIUS‡
Honeywell SSEC, 12001 Hwy 55, Plymouth, MN 55441, U.S.A.

(*Received* 2 *November* 1995)

Abstract—The aggressive scaling planned for integrated circuits is placing more demands on the materials, processes and designs. The circuits must be reliable and electromigration is a key reliability issue. Because many of the factors that contribute to electromigration are not completely understood, manufacturers must proceed cautiously. In this article electromigration is reviewed from the prospective of the reliability engineer, focusing on those areas of greatest applicability to the manufacturing environment. First, the fundamental physics of electromigration are examined to provide a basis for understanding the factors that affect the lifetimes under the various test conditions. Then, empirical data concerning the impact on reliability of metal stripe geometry, structure and composition are reviewed. The care necessary to make fast, wafer-level tests an important process control tool is discussed. It is shown that pulsed-dc and ac waveforms can provide longer lifetimes than predicted previously, providing some relaxation of current density requirements for higher circuit densities. An understanding of these phenomena is necessary for the reliability engineer to assess today's and tomorrow's integrated circuits. © 1997 Elsevier Science Ltd.

1. INTRODUCTION

Electromigration in thin films has been the subject of intense study, both theoretical and experimental, over the past 30 years. The reason for this interest is that electromigration can cause opens or shorts in integrated circuit interconnects under conditions of normal use, resulting in circuit failure. Thus, electromigration is of great practical interest to manufacturers and users of microcircuits.

In spite of this exhausting study, many aspects of electromigration are not well understood. This is due in part to the many factors (grain structure, grain texture, interface structure, stresses, film composition, physics of void nucleation and growth, thermal and current density dependencies, etc.) that influence electromigration and to the inability to isolate the effect of these factors experimentally. Indeed, in an example given in Section 2, we will see that it is not possible to differentiate between two models of gross electromigration behavior given exceedingly well behaved data, due to the dominance of the exponential terms in the atomic diffusivity. The inadequate theoretical understanding leads to the unsatisfactory result that design for metal reliability during process development is largely a trial and error process governed by an incomplete set of underlying principles.

Electromigration in integrated circuit metallization continues to be a subject of importance with an increasing number of publications on the subject every year. This intense interest is the result of the planned aggressive scaling of integrated circuit dimensions over the next 10 years. E.g. the Semiconductor Industry Association's Technology Roadmap [1] estimates that by 2010 the average interconnects cross section will be reduced by a factor of nine, the total length of interconnect per chip will increase by a factor of 25, the required interconnect reliability will increase by a factor of 32 and the power dissipated by the chip will double. These factors all lead to the need for greatly improved electromigration performance.

In this article we will review what we feel is the state-of-the-art in electromigration from the practical standpoint of those that fabricate integrated circuits. Along with that review, we will take the opportunity to share some unpublished data that are of relevance.

2. BASIC PHYSICS

As a result of the great interest in electromigration expressed above, several exhaustive review articles on the subject have been written in recent years [2, 3]. In this section it is not our intent to replicate the detailed information already available in those articles. Rather, we will set the stage for the sections that follow and place our interpretation on those areas we feel worthy of additional comment.

†Currently at Sandia Technologies, P.O. Box 23338, Albuquerque, NN 87192 U.S.A.
‡Author to whom correspondence should be addressed.

Electromigration is forced atomic diffusion with the driving force due to an electric field and associated electric current in metals. Electromigration is an important failure mechanism in integrated circuit metallization for two reasons. The first is that metal thin films can dissipate enormous power densities without melting and in turn can carry large current densities (>10 MA/cm^2 for aluminum). Thus, the driving force can be quite large. Second, the ratio of grain boundary/interface area to film cross-sectional area is large, leading to fast diffusion paths and high average mobility [4]. Thus, the diffusion process itself is faster in thin films which also enhances the effect.

The electromigration of aluminum requires the self diffusion of aluminum in an aluminum matrix. This is only possible if the diffusing atom can jump into a vacancy in an adjacent lattice site. Thus, mathematical treatments of electromigration in aluminum are usually cast in terms of vacancy diffusion, which yields an equal and opposite flux of host atoms. The vacancy flux (J) due to the electromigration driving force (including the back diffusion term) is

$$J = -D\frac{\partial c}{\partial x} + \frac{Dc}{kT}Z^*eE = -D\frac{\partial c}{\partial x} + \frac{Dc}{kT}Z^*e\rho j \quad (1)$$

where c is the vacancy concentration, D is the diffusivity, k is Boltzmann's constant, T the absolute temperature, e the electronic charge, E the applied electric field, ρ the resistivity and j the current density. The effective charge (Z^*) is a dimensionless material parameter thought to be comprised of two components:

$$Z^* = Z_{wd} + Z_{el} \quad (2)$$

where Z_{wd} is attributed to momentum exchange between the electron current and the moving atom and Z_{el} is related to the direct electrostatic force on the moving atom. There have been many theoretical treatments of the terms in eqn (2) and a good deal of controversy over whether the term Z_{el} even exists [5–8]. In any case, the electron wind term dominates eqn (2). Thus, aluminum atoms drift in the direction of electron drift and Z^* is positive using the sign convention of eqn (1).

There are two boundary value problems where inspection of eqn (1) provides simple solutions to the diffusion equation that have practical impact. First, consider a thin metal stripe connecting two infinite reservoirs of vacancies (integrated circuit bond pads are a close approximation), subjected to an electric current. Then, in the absence of any flux divergences in the line, eqn (1) implies that the metal line will simply transport metal atoms from the cathode to anode reservoirs. This simple example, which does not result in failure, has an important practical application. Modern metal systems, with narrow linewidths and large grain sizes, may not have defect locations which result in significant flux divergence. Indeed, the above situation has been observed where electromigration damage occurs in the wide end segments of the structure, rather than the narrow line of interest [9]. This phenomenon has led to efforts to redesign electromigration test structures to include diffusion barriers at the line ends to eliminate this effect (e.g. the SEMATECH Working Group on Back End of Line Reliability).

The other simple boundary value problem consists of a line terminated with diffusion barriers (zero atomic flux at the ends of the lines). Again, in the absence of flux divergence in the interior of the line, eqn (1) yields a steady state solution where all atomic flux ceases and the vacancy concentration varies exponentially with distance. Blech [10] examined a similar problem where he assumed that stress gradients provide the dominant driving force for back diffusion. The steady state solution occurs when the driving force due to generated stress equals that due to electromigration, or

$$Z^*e\rho j = \Omega\frac{\partial \sigma}{\partial x} \quad (3)$$

where Ω is the atomic volume and σ the stress. If, as Blech did, we assume that failure requires exceeding some critical stress, σ_c, eqn (2) yields the result that failure will not occur unless the following condition is satisfied

$$j_l > (\sigma_c - \sigma_o)\frac{\Omega}{Z^*e\rho}. \quad (4)$$

Thus, for a given current density there is a line length below which failure will not occur, the well-known Blech length. This has important reliability implications as very short lines will not fail due to electromigration. (A more advanced treatment of the problem of stress and electromigration can be found in Ref. [11].)

From the above discussion it is clear that electromigration will not cause failure unless there is a divergence in the vacancy flux somewhere in the line that allows voids or extrusions to form. Some examples of sources of flux divergence are shown in Fig. 1. The top example is very common today with the pervasive use of diffusion barriers in metallization stacks. In the example shown, an electron current

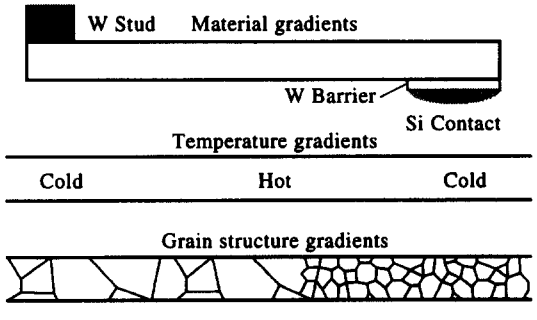

Fig. 1. Sources of flux divergence.

flowing from left to right would cause voiding at the W stud and an accumulation of metal at the silicon contact. For the thermal gradients shown in the middle example, the cold regions act as a diffusion barrier (analogous to the first example) because of the strong temperature dependence of the diffusivity D (and hence mobility)

$$D = D_0 e^{E_a/kT} \tag{5}$$

where E_a is the activation energy for diffusion. In the final example, which often dominates in fine grained metal lines, changes in grain size cause the flux divergence. In the example shown, the material flux in the right side of the figure is greater than the left because there are more grain boundaries to support mass transport. Hence, for an electron current flowing from left to right, a void would form near the middle of the line. The limiting case of the grain structure gradient is when two grain boundaries meet a third, the "triple point" so often cited in electromigration literature. For very narrow lines, with large grains, the "bamboo structure" develops where most grain boundaries are transverse to the line and hence do not aid in the diffusion process. Since there are no "short-circuit" diffusion paths, bamboo lines tend to show the greatest resistance to electromigration induced damage.

While it is necessary to have flux divergence in order for an electromigration failure to occur, it is not sufficient. E.g. in the Blech length discussion above strong flux divergences were at the diffusion barriers at the ends of the line. However, a critical stress had to be exceeded in order for a void or extrusion to form at the flux divergence site. Thus, the mechanics of void (or extrusion) nucleation and growth are critical to electromigration damage.

2.1. *Solutions to the diffusion equation: median time to failure*

The previous section can be broken into three primary topics: transport (electromigration), flux divergence, and void (or extrusion) nucleation and growth. Those topics define the problem to be solved in order to extract the parameter of most interest from a reliability standpoint, the time to fail a metal line at a given stress condition. The transport phenomena define the form of the diffusion equation that needs to be solved. The flux divergence locations define the endpoints of the region over which the diffusion equation needs to be solved and defines part of the boundary conditions (blocking or permeable barrier). The void (or extrusion) nucleation and growth mechanism defines the rest of the boundary condition (vacancies or atoms are removed from the system over time) and gives the criterion for failure. There are many theories for the physical mechanisms behind each of these elements and many solutions, both analytical and numerical, for the diffusion systems which arise. Before examining a few of those approaches, it is instructive to ponder the most widely used relation for the analysis of electromigration data, Black's equation.

Black [12] developed an empirical model relating the median time to failure (t_{50}) of a metal line to the temperature (T) and current density (j) of the following form,

$$t_{50} = \frac{A}{j^n} e^{E_a/kT} \tag{6}$$

where A is a material and process-dependent constant and E_a is the activation energy for the diffusion processes that dominate over the temperature range of interest. Black assumed that the current density exponent was two, which fit his data quite well. That result is somewhat surprising since eqn (1) shows that the driving force has an inverse current density dependence. Measurements reported in the literature have yielded current density exponents ranging from slightly greater than one to values of six or more, with the bulk of the values clustered around two. Values of n above two seem to be due to improper treatment of self-heating effects (more will be said on that in Section 6). Due to variation in reported values of n, some workers treat n as a free parameter. Lloyd [13] has argued that this approach is physically unsatisfactory because the units of A would depend on the value of n measured. From a purely empirical standpoint it is difficult to make a judgment on the correct value of n from data reported in the literature because of typically small sample sizes, limited range in the independent variable (j) and the puzzling tendency for electromigration researchers not to place confidence bounds about their experimental results.

Shatzkes and Lloyd [14] derived a solution to eqn (1) for the case of a semi-infinite line with a perfectly blocking barrier at one end. They assumed that failure would occur when the vacancy concentration at the barrier end of the line reached a critical value needed to nucleate a void. From that model, they obtained the following expression for the time to failure

$$t_f = B\frac{T^2}{j^2} e^{E_a/kT} \tag{7}$$

where B is a constant. This expression is very similar to Black's [eqn (6)], with the exception of the temperature squared term in the pre-exponential factor. Lloyd and Kitchin [15] treated a finite line numerically and found that the current density exponent is also two. Other treatments also find an inverse current density squared dependence [16, 17].

The derivation of eqn (7) was based on the assumption that void nucleation dominated electromigration induced failures and void growth, and resultant failure happens soon after nucleation. Lloyd also considered the case where growth of a void to dimensions needed to cause failure was the rate limiting process [18]. In that instance, the flux of vacancies to the void site dominates and Lloyd found

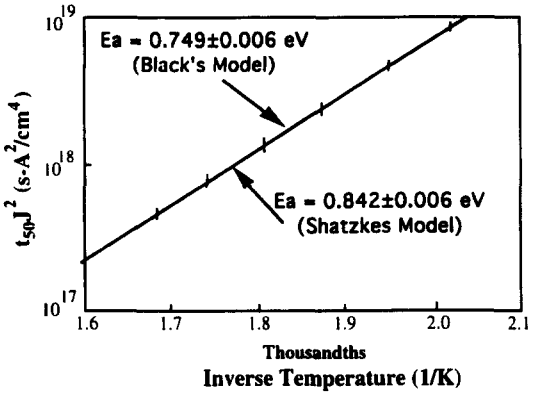

Fig. 2. Curve fits of the Black and Shatzkes–Lloyd models to t_{50} data show both models fit equally well.

that an inverse current density dependence should hold, as would be expected from eqn (1).

Oates recently reported experiments on two Al/Cu/Si metallizations of width 0.6 and 1.2 μm, sandwiched between Ti and TiN layers [19]. Oates found that the current density exponent was 1.9 ± 0.4 for the 1.2 μm lines and 1.2 ± 0.2 for the 0.6 μm wide lines. The 0.6 μm wide lines exhibited few voids which were very large upon failure. This is consistent with Lloyd's observation that an inverse current density dependence is expected when void growth is the rate limiting step in electromigration failures. Other theoretical treatments predict this result [11, 20].

We have seen a variety of models describing the dependence of the median time to failure on stress conditions. The critical question is "which of these models should be used to analyze data and extrapolate results to use conditions?" It is very difficult to answer that question experimentally because of the exponential dependence of the median time to failure on temperature. E.g. electromigration data (taken at the Sandia laboratory), normalized by the square of the current density, are presented in Fig. 2 for a very well behaved layered metallization with a near bamboo grain structure. A sample size of 20 was used to estimate each median time to failure, shown by the circles in the figures. The solid vertical lines are 90% confidence bounds on the estimate of t_{50}. The confidence bounds are small, reflecting the low standard deviations of the failure distributions.

The solid lines (indistinguishable on the scale of Fig. 2) are fits to the data using Black's model [eqn (6)] and the Shatzkes–Lloyd model, eqn (7). Both models fit equally well from a visual and statistical standpoint. Also, because of the small amount of curvature in the Shatzkes–Lloyd model, both fits yield equivalent results when extrapolated to low temperatures. However, the models yield quite different activation energies, as shown in the figure. While of small significance from a reliability engineering standpoint, a proper activation energy is critical in ascertaining the physical processes underlying electromigration. Unfortunately, the models cannot be distinguished from electromigration data and the experimenter is left to use his best judgment as to which analysis technique to choose.

2.2. *Statistics*

Electromigration failure results are statistical in nature, with the statistics driven by the grain structure and defectivity of the metal line under stress. The most common approach to analyzing electromigration data is to assume that the failures are log-normally distributed. This approach is used because of tractability and because the log-normal distributions fit electromigration data quite well. By assuming that the bulk of diffusion at low temperatures is dominated by grain boundary diffusion and that the activation energy for grain boundary diffusion varies normally due to orientation of adjacent grains. Lloyd and Kitchin found those assumptions lead to log-normally distributed times to failure for a stripe with a single potential failure site (or given a constant density of failure sites, a stripe of fixed length) [21]. Though the time to failure for stripes containing a single site might be log-normal, the distribution of times to failure for stripes of arbitrary lengths (arbitrary numbers of potential failure sites) are not. Based on the consideration that the weakest link in a flux divergence chain will fail first, Lloyd and Kitchin derived a multi-log-normal distribution from their single element model. They observed that extrapolation of the log-normal distribution to the number of line segments on an integrated circuit would cause the time to first failure to be overestimated by a factor of 10 depending on the sigma of the fitted distribution. (Of course, extrapolating small sample data to large sample sizes is fraught with peril in any case.) Thus, for conservative estimates for time to first failure (and developing metal design rules), a multi-log-normal distribution is the soundest approach, with some loss of convenience. Other workers have also explored the weakest link approach to electromigration statistics [22].

With the pervasive use of barrier layers, which provide a built-in flux divergence site and the processing of robust metallizations with bamboo structure, the lack of scaling of the log-normal distribution with line length may cease to be a problem [23]. That is, the weak site on the line may always be the cathode diffusion barrier and hence each line segment on an integrated circuit has one potential failure site, regardless of length (ignoring the Blech effect). In that instance, metal lines might exhibit true log-normal behavior, with multi-log-normal behavior characteristic of ensembles of integrated circuits.

2.3. *Physics summary*

Our brief review of electromigration physics shows the difficulty that the experimenter has in choosing a framework in which to analyze one's electromigration data and apply it to the reliability of a

fabrication line's product. The differing approaches also make it difficult to interpret data in the literature. E.g. was an activation energy reported in the literature obtained using Black's model, Shatzkes and Lloyd's model, or yet some other model? All give different results for identical data. Perhaps the most important difference among the approaches is the choice for the current density exponent, since physical reasoning and data indicates that it can lie in the range of 1–2, with important implications in extrapolating results to use conditions. Perhaps the watchwords in electromigration work are to be ever vigilant and never complacent in applying assumptions or using models.

3. STRIPE TESTING

While experiments to support various electromigration transport theories may be conducted in many ways, tests to compare processes, materials, or techniques are generally performed on straight lines with Kelvin connections where a failure criteria is defined and statistics are gathered. Because real life electromigration generally takes years to occur at normal conditions, electromigration tests are almost always highly accelerated. Temperature and current density are the most common means of acceleration. There are many nuances with such test procedures that often lead to widely varying results. The length and width of the test vehicle and the measurement technique are important for obtaining consistent results. Proper consideration of these factors is necessary for the design engineer to assure a reliable chip design. The following section will address the effects of the processing and film design alternatives.

A number of researchers have noticed different results due to the length of the test line. Agarwala *et al.* [24] found that the median lifetime decreased rapidly with increasing length until a critical length was reached where the lifetime became independent of length. Below the critical length the median lifetime exhibited the following behavior

$$t_{50} = Aw \exp(a/l), \tag{8}$$

where A is a constant, w is the width, a is a constant dependent on width and l is the length of the conductor. In that study, a was found to be equal to 63.5 and 83.8 μm for 10 and 15 μm wide stripes, respectively. The rationalization for this behavior was that the probability of encountering more severe defects increases with longer lines. The saturation of the lifetimes at longer length is due to a maximum severity of the defect distribution. A line longer than the critical length always contains the critical defect distribution. This model also suggests a decreased s would come with longer lines and this has been observed [25]. Learn and Shepherd [26] reported that the median lifetime decreased by a factor of 3.5 when a 3300 μm line was compared to a 250 μm line. Kakar [27] found a similar effect. Researchers [28, 29] have suggested that very long test lines should be used for electromigration tests. Schafft *et al.* [30] performed an interlaboratory experiment with 11 laboratories using lines 400, 800 and 1200 μm long, and concluded that 800 μm would make the best standard. While longer lines may give more consistent results, they would have more resistance which requires more voltage making the test more difficult to perform. This standard has been adopted by many and formalized as an ASTM standard.

The effect of line width on electromigration lifetime is more important than length because new technologies are constantly being scaled down and different current density limits may be required for the next generation's smaller devices. Black [31] found that the film lifetime was a direct function of the cross-sectional area for large grained films on lines from 11 to 50 μm wide and thickness from 2000 to 12,000 Å. Since the failure of a line results from a series of voids that eventually string across a line, it should take longer for those voids to line up on a wider line. The idea that smaller lines require smaller current density limits for the same lifetime has a profound effect when scaling a process. Process shrinks would be more limited by metal line width requirements than they now are. Black [32] showed that small conductors should be restricted to carrying a current density less than 0.1 MA/cm^2.

The application of scaling theory [33] to electromigration suggested that at constant voltage, the lifetimes would scale as $1/S^7$, where $S > 1$ is the scaling parameter. This result includes some device assumptions, a more complete discussion of which is given elsewhere [34]. One would hope that near-zero linewidths would support more than a near-zero current density.

There are other factors which affect the linewidth phenomena. Vaidya *et al.* [35] found an unusually large lifetime improvement for fine lines (< 2 μm) due to the film microstructure. These results are shown in Fig. 3. Because the sigmas also tend to increase with decreasing linewidth, the failure rate of the line is more difficult to predict.

This improvement was attributed to the fact that the narrow lines consisted of a "bamboo structure"—a chain of relatively large Al grains with a preferred [111] orientation. The lifetimes correlated to a single parameter containing the grain size, its sigma and the texture. Thus, when lines are narrower than the average grain size, higher current densities can be reliable if the microstructure is properly controlled. Since grain sizes > 2 μm can be produced and controlled, near-micron and submicron lines can tolerate higher current densities than those proposed by Black. This effect has been verified by others [36].

Accurate measurement of the stripe temperature at the accelerated test conditions is also important. In most instances the temperature of the test stripe is found by measuring its resistance at a low current at room temperature, making a similar low current

measurement at the test ambient temperature to allow the calculation of the stripe TCR, and finally making a third resistance measurement at the test current and test temperature ambient. This last measurement allows a simple calculation of the temperature rise.

In an interlaboratory experiment [30] it was found that the testing results of the 11 laboratories on identical samples were within approximately 15% for a modest current density, but varied by 50% for a higher current density. The major cause for the variability was said to be the estimation of the temperature rise of the test metallization due to Joule heating. In this study, the stripes with the lower current density were measured to have a temperature rise of between 4 and 5°C, while the higher current density samples had a rise of between 26 and 36°C. Errors in the calculation of this temperature rise can have significant impact on the lifetime measured. E.g. an error of 9.4°C in the temperature estimate can lead to an error of 30% in the time to failure for an activation energy of 0.55 eV. This error may result from not accounting for the cooler end contact segments between the voltage contact and the test line. Schafft [37] has modeled the test line temperature and recommended that the line should be at least 400 μm long to minimize thermal interactions, that the end contact segment should be twice as wide as the test line, that the length of the end contact segment should be longer than 100 μm, and that the voltage taps should contact the end segment at least 4 times the test line width from the test line. For very fast electromigration tests the Joule heating is even more important, and is discussed further in Section 6.

More tests on simple aluminum lines are performed by monitoring the line resistance and terminating the test when the failure criterion is reached. Typical failure criteria range from a 5 to 20% increase in line resistance. It has been suggested [38] that a 50% resistance increase would be a reasonable failure criteria because the process becomes more thermomigration dominated stressed to this degree. Researchers [39] were able to predict stripe reliability by the early resistance and TCR changes during stress tests. Such tests would take a shorter time and be required for stripes with barrier metals or made of refractory metals which may never reach the failure criterion. Because of resistance oscillations during electromigration tests with barrier metals, a smaller percent failure criteria, 10–30%, will probably give a more consistent estimate of the stripe lifetime [40]. Others have reported that the magnitude of the percent change failure criteria can significantly affect the value of t_{50}, and the calculations of E_a and n [41]. As the pitches of advanced VLSI devices get smaller and the number of levels of metal increases, hillocks and extrusions of stressed metal can lead to short circuits [42]. The use of a TiW barrier metal makes stripes last long enough that short circuits could be the dominant failure mode [43], depending on the thickness of the TiW (thicker TiW = more shorts) and the dielectric thickness (thicker dielectric = longer short circuit lifetime). Thus, more complex test structures and set ups must be employed. New testing problems may also arise because at extremely high temperatures there may be conduction due to thermally generated carriers between the test stripe and its extrusion monitors.

In order to really shorten the testing time, researchers have set up models to perform virtual testing. An early probabilistic model [24] was based on the distribution of structural defects of varying severity along the conductor line. These defects were assumed to be randomly distributed with a constant density. The distribution of the times to failure reflects the distribution of the defects. The model was made to match the observed linewidth and length dependences. A statistical metallurgical model [44] was later derived based on the various divergences due to grain size, grain-boundary mobility and grain-boundary orientation with respect to the electrical field vector in the conductor. This model was found useful from a quality control viewpoint to determine the effect on electromigration lifetime of different grain sizes (longer lifetimes with larger grain size if the grain size variance was constant) and grain size distribution (shorter lifetimes with increased grain sized variance). Building on this model Schoen

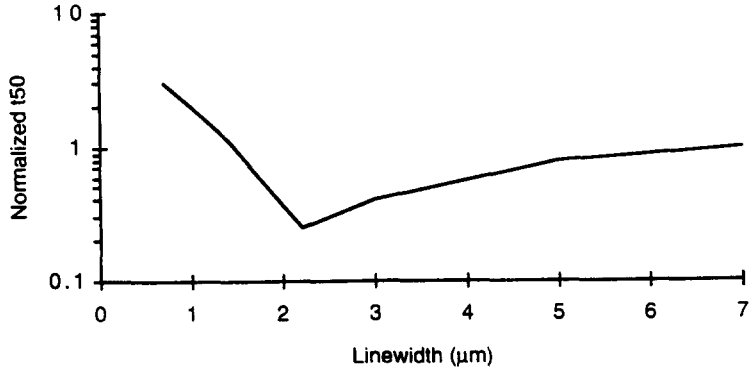

Fig. 3. Effect of linewidth on electromigration lifetimes [35].

[45] set up a computer program to perform Monte Carlo calculations. Again the results were made to fit the noted linewidth, length and grain size effects. Going a step further, Nikawa [46] used an iterative approach in which the growth of a crack increased the local current density which increased the local Joule heating which quickened the crack process. This model predicted lifetimes consistent with a number of previous studies, including the sharp increase in median lifetime as the linewidth decreased to less than the median grain size. Such models were effective at matching past performances, but require more work for predicting new characteristics.

Perhaps of more interest are simulators which predict circuit wearout effects. The Berkeley reliability simulator, BERT [47], utilizes SPICE models and actual layouts to predict currents and their associated wearout effects, such as hot carriers and electromigration. This simulator is based on the length and width dependencies described above, and is said to provide caution when lines need to be widened or vias added, and provides an electromigration failure rate estimate as a function of time, temperature, voltage, frequency and previous stress [48]. Another simulator [49], which utilized Monte Carlo analyses to predict a time-to-failure distribution of an entire VLSI chip, provided feedback for the effect of dimension reduction on a custom designed microprocessor chip. Such programs require huge data bases, and require a lot of time and set up on large computers. More limited, but yet important, schemes allow the computation of average current densities in the power and ground bases for electromigration estimations [50, 51].

In brief, if a design/reliability engineer knows the size of his lines and has characterized the electromigration properties of the process, he can estimate the lifetime of those lines. In the next section, the factors affecting the options of the process/reliability engineer will be discussed.

4. MATERIALS AND THEIR EFFECTS

Most metallurgical systems for integrated circuits are based on aluminum because of its low resistivity and compatibility with silicon processing. It can be deposited by either evaporation or sputtering and has good adherence to silicon dioxide. Aluminum does not, however, have a great electromigration resistance. There are a number of ways to improve the limitation, including changing the microstructure, alloying and the use of another metal either on top, beneath, or in the middle of the aluminum film. The various approaches may have greater electromigration qualities, but are limited in their ease of processing or electrical characteristics. These approaches to enhanced electromigration performance will be discussed here.

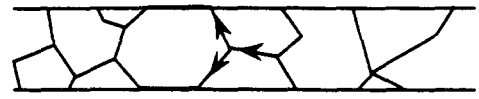

Fig. 4. Triple point.

4.1. *Microstructure effects*

The electromigration resistance of aluminum has been shown to be dependent on the film's microstructure. It was noted in the previous section that longer lifetimes can result from larger grain sizes. One experiment [52] showed that single crystal aluminum was practically impervious to conditions of high current and temperature that caused rapid failures in polycrystalline aluminum. Unfortunately, the high temperature ($>400°C$) conditions required for such processing cause other problems. A line conducted for more than three years at 5 MA/cm^2 and 175°C without failing. Unfortunately, it is not possible to make a single aluminum grain the size of an integrated circuit in a reasonable period of time. Baerg and Wu [53] showed that for two specific metallization systems, the median lifetime was directly proportional to the grain size and the lifetime sigma was directly proportional to the grain size distribution; with the proper characterization, the grain information could be a useful tool for production monitoring. Others [54] have described a similar dependence of failure time on grain size. Part of these observed improvements are due to the reduction in triple points [55]. Triple points are places (Fig. 4) where the boundaries of three grains meet and the electron wind carries ions away on two boundaries and replenishes from one boundary; this process leaves a net loss of material at the triple point, i.e. a void. If the current is flowing in the opposite direction, the triple point may cause a hillock.

In some instances, electromigration lifetime gains are due to more than just larger grains. One study [56] found longer median lifetimes with larger grains, but noted that this increase was probably due to the change in film orientation. A [111] orientation [57] seems to increase electromigration resistance but does not reduce the grain boundary diffusion. A similar relationship between the electromigration behavior and [111] orientation was observed on bamboo structures [58]. Apparently, grain boundary atomic mobility is smaller in films with [111] orientation [56].

Purer aluminum films, as measured by their lower resistivity, will generally have longer lifetimes [59]. In another instance the median lifetime experienced a nine-fold improvement in a high vacuum PVD system [60].

The electromigration resistance of aluminum has also been improved by anodization [61]. A seven–14 times lifetime increase was observed and attributed to a reduced vacancy supply and/or reduced density of void-nucleating sites. Similarly, an oxygen plasma treatment, applied after patterning, was found to

reduce electromigration [62]. The lifetime increased as a function of plasma treatment time.

4.2. *Alloys*

Probably the most common alloying element that is added to aluminum for electromigration purposes is copper. In 1971 d'Heurle [63] found that the lifetimes of films containing copper increased with increasing copper concentration, even beyond the solid solubility limit of copper in aluminum (0.05 wt %). The longest lifetimes were observed with 16% copper, although there may have been other microstructure factors at work with some of the higher copper concentration films. This enhancement is attributed to a two step process: the first and longest step occurs while the copper is depleted from certain areas of the conductor (the grain boundaries); in the second step void formation begins in the areas without copper. In one model of this process the activation energy of Al–Cu films is 0.2–0.3 eV greater than that for the pure aluminum films because of this incremental process [64]. Other studies [65] seemed to show that the addition of *ca.* 4% copper to the aluminum provided about as much lifetime improvement as could be expected, and still allowed for reasonable processing (etchable without corrosion) and silicon performance (non-poisoning of silicon at contacts). A key factor in the lifetime improvements is the heat treatment. Low temperature (250°C) aging for as long as 10 h has been found to increase lifetimes as much as 10 times [66].

Other materials have been alloyed with aluminum for electromigration purposes with differing amounts of success. Magnesium (3 wt %) and chromium (2 wt %) have been found to improve electromigration resistance, while nickel (2 wt %), gold (2 wt %) and silver (2 wt %) provided little gain [67]. These alloys tend to have high resistivities. A ternary alloy—AlCuMg—would be better, and the quaternary alloy containing 4 wt % Cu, 2 wt % Si and 1.5 wt % Mg might be preferable [68]. Magnesium offers the additional challenge in that it tends to react with the oxide at high temperature. More recently Al–Si–V–Pd with 0.1 at. % of both V and Pd has been touted as having improved electromigration resistance for submicron lines with acceptable process integration possibilities [69].

Another scheme to improve the electromigration resistance of aluminum involves adding another metal layer, usually a refractory metal. This metal layer may be added underneath as a barrier metal, on top as a capping layer or in the metal as a sandwich. TiW (generally 10:90 wt %) has been used for many years as a barrier metal to prevent aluminum junction spiking, most often over PtSi ohmic contacts on bipolar devices [70]. The parallel films combine the low resistance of aluminum with the high electromigration resistance of the high melting point tungsten. The electromigration performance of aluminum or aluminum copper with a TiW barrier metal is generally twice as superior as that of the same film without a barrier [71], but can be much as 10 times as [72] with careful control of the vacuum. This improvement is due to the fact that the TiW will continue to conduct current in the presence of aluminum voiding and even when the aluminum may be completely open circuited. Similar improvements have been observed with TiN barrier metals [73]. Capping layers of refractory metals and silicides, such as Ti, W, WSi_2 and $MoSi_2$ have also been seen to increase electromigration lifetimes between four and 10 times [74].

Another means of improving the electromigration performance of aluminum-based films uses a layer of intermetallic compounds of aluminum and transition metals [75]. Lifetime improvements of 100 times are reported. The scheme involved depositing a 200–600 Å layer of the desired transition metal (Cr, Ti, Hf or Ta) between two half normal thickness layers of aluminum, aluminum copper or aluminum copper silicon. The improvement was attributed to the aluminum transition metal compound which effectively blocks crack growth through the film—there are two parallel wires and the probability of voids aligning across each wire at the same place is small. A similar approach using gold and at least one transition metal have shown significantly improved electromigration performance without significantly increasing resistance [76].

Pure copper is one of the most promising films to replace aluminum based conductors because of its low resistivity. The use of copper requires a diffusion barrier to prohibit junction poisoning. In one instance [77] its lifetime was reported to be an order of magnitude longer than that of Al—4% Cu/TiW. Small amounts of palladium added to the copper further improve the electromigration resistance [78].

For more electromigration resistance, refractory metals, such as tungsten or molybdenum, could be utilized. Sputtered tungsten films have demonstrated a median life of 1200 h at 4 MA/cm^2 at 415°C, conditions at which a comparable AlSiCu film would be expected to last 1.7 h [79]. Molybdenum has been tested for 1 week at 300°C and 2 MA/cm^2 with no failures [80]. A Mo/TiW film showed no failures (50% increase in resistance) after 24,000 h at 150°C and 3.6 MA/cm^2 [81]. Some of the longest lasting films in electromigration tests are summarized in Table 1. Note that the non-aluminum films will have activation energies larger than the 0.7 eV assumed in Table 1. Thus, the lifetimes at use condition are greatly overestimated for those films.

4.3. *The role of glassivation*

Since the electromigration process is related to flux divergences and stress, the glassivation would be expected to have an important role. Not all studies have observed the same results. Black's early work [31] and that of others [82] have found that the glassivation increased the activation energy and

correspondingly increased the lifetimes. Others [56] found no change in activation energy. Such differences may be due to the different films, different glassivation, the glassivation process or any combination of these. It is important to understand this effect because nearly every current-carrying conductor is glassivated.

It would appear as though a coating would impede the growth of hillocks and whiskers which must occur with the void formations. Such a process should increase electromigration lifetimes. Ainslie *et al.* [83] showed that there is no glass strong enough to stop the electromigration induced pressure gradient. It is argued that the coating can only reduce the rate of electromigration if the glassivation is extremely strong and conformal to the metallization. Lloyd and Smith [84] observed an increase in lifetime with glassivation and also longer lifetimes with thicker glassivation. Interestingly, the devices with thicker glassivation tended to have more short circuits (the stressed lines were meanders), because the thinner passivation allowed the aluminum to relieve its stress by cracking through vertically, whereas the thicker passivation forced the aluminum between the passivation and underlying oxide interface to the adjacent line. Schafft *et al.* [85] also found longer median lifetimes for passivated samples. He attributed the difference to the mechanical rigidity—the stiffer nitride passivation gave longer lifetimes than phosphorous doped glass. Consistent with these results, polyimide passivation was found to give better electromigration lifetimes than quartz because the quartz tended to have more defects and thus more defect induced flux divergences [86].

All this work tends to show that, if the objective is to determine the reliability of interconnections of the integrated circuits, it is essential to carry out the electromigration testing on samples processed in the same manner as the product. All thermal treatments which could affect the microstructure and the real passivation must be present.

5. CONTACTS AND VIAS

Another electromigration failure mode observed by Black [87] was the shorted or spiked junction. In an aluminum–silicon contact under conditions of high current and temperature, the dissolution of silicon into the aluminum occurs; pits in the silicon are filled with aluminum; as the process continues, the aluminum will eventually short the junction. This process has a relatively high activation energy, 0.95 eV, but is slowed by saturating the aluminum film with a few percent silicon—at 235°C only. 0.003 wt % silicon can stay in solid solution with aluminum. The use of an AlSi alloy can, however, decrease the electromigration resistance of the stripes and degrade the ohmic properties of the contact. This problem has been solved by applying another film between the aluminum and the silicon.

The incidence of spiked junctions can be decreased by applying a CVD layer of doped polysilicon under the aluminum [88]. In this configuration, the polysilicon acts as a barrier material, as well as improving the step coverage. The electromigration process still proceeds, and the lifetime has an activation energy of 0.9 eV, a current density dependence of J^{-10} and a junction depth dependence of x_j^2. It is argued that such a metallization system will be limited by the stripes, not the contacts. However, AlSi stripes do not have particularly long electromigration lifetimes.

Gargini *et al.* [89] showed that scaling devices by a factor k ($k > 1$) with a constant voltage (i.e. 5 V) will increase the current density at the contacts by a factor of k^3. While verifying the same concerns and acceleration factors as above, a different solution was proposed—the use of a refractory barrier metal, such as tungsten. This approach is valuable for shallow junction devices because it eliminates spiking failures, such that the major failure mode would be open circuits at the contacts. This occurs when the electrons flow from the silicon to the aluminum through the barrier metal; the aluminum moves away from the contact but cannot be replenished because of the barrier.

Another common barrier material is TiW, usually with a weight % ratio of 10:90. This material was originally developed as a barrier between gold thin films and PtSi contacts in the 1970s, but has been applied to aluminum films extensively [90]. The ohmic natures of such contacts have been studied thoroughly [91]. Electromigration tests on via chains with and without TiW have shown an order of magnitude improvement with the barrier metal [92]. TiN is sometimes considered a better barrier film than TiW, but has shorter electromigration lifetimes [93]. Silicides cannot be used as a diffusion barrier in aluminum contact systems because they break down at annealing temperatures around 400°C [94]. For

Table 1. Summary of the longest lasting films in electromigration tests

Metal	Tested conditions ($mA/\mu m^2$—°C)	Tested lifetime (h)	Projected lifetime at 25 $mA/\mu m^2$—150°C with $N = 2$, $E_0 = 0.7$ eV	Ref.
MoTiW	36–150	>24,000	>50,000	[81]
W	40–415	1200	5,436,000	[79]
Al–4%Cu/Cr/Al–4%Cu	10–250	11,000	75,000	[75]
NbAuNb	20–300	>10,000	>1,055,000	[76]

Table 2. Combinations of metals used to form vias

Top metal/plug	Electron flow from M1 to M2— failure locations	Electron flow from M2 to M1— failure locations
No barrier/no plug	Interconnects	Interconnects
Barrier/no plug	Interconnects and vias	Interconnects and vias
No barrier/plug	Vias	Interconnects and vias
Barrier/plug	Interconnects	Vias

planarization, smaller contacts may require the use of plugs where the opening in the dielectric is filled by a different metal (often tungsten). Some improvement in the electromigration lifetime has been observed for plug contacts, but this improvement has been attributed to the lower sheet resistivities of the barrier metal in the stack, not the plug or the improved step coverage [95]. Thus, for plugged contacts, electromigration failure times can be lengthened by decreasing the sheet resistance of the refractory metal.

Electromigration of vias, the connections between a first metal conductor and a second metal conductor, is more complex because of the use of multiple metals and structures (plugs/non-plugs). For vias, the electromigration process is dominated more by the interfaces between dissimilar metals and less by the conductor microstructure [96].

The traditional concern for via reliability is the step coverage. Standards, such as MIL-STD-883D, TM 2018, have required step coverages of at least 30%. However, it has been shown that for metallizations with good barrier metals, step coverage is not a factor in the electromigration failures [97]. To be sure, care must be taken when determining what has failed in a via. In one test of vias between TiW/AlCu conductors, the via resistance was monitored separately and found to be stable with resistance increases $<20\%$, while the metal conductor resistance, which included the via resistance, increased as much as 270% [98].

The use of plugs and barrier metals has been thoroughly studied. In one evaluation [99], different combinations of metals were used to form vias, as indicated in Table 2. In this instance the conductor was AlCu, the barrier was TiW and the plug was W. For this high stress condition there were always failures at the vias when the plug was present and the median lifetimes of all plug via failures were shorter than those of the non-plug via failures. With plugs, the vias are the limiting factor; without plugs, the interconnects are the limiting factor. This effect has been confirmed by others, although improvements in plug via lifetimes have been observed due to titanium layering around the plug [100].

Care must be taken when evaluating the electromigration lifetimes of contact and via chains, because if the successive contacts and vias are too close together, no void formation will take place due to the Blech effect discussed earlier. For 1 μm diameter contacts/vias the conductors between the contacts/vias must be at least 10 μm, and probably closer to 30 μm, in order to have the electromigration process reach the critical current [95].

Again, these results explain why tests must be sure to duplicate actual process and layout conditions to meaningfully explain behavior on integrated circuits. In addition, careful analysis of the failure modes and testing details is essential to a true understanding of the circuit reliability.

6. FAST (WAFER-LEVEL) ELECTROMIGRATION TESTS

An electromigration test conducted at moderate test conditions ($T < 250°C$, $j < 2$ MA/cm^2) can take weeks or even months to complete. This test time is much too slow to provide feedback to a manufacturing line for statistical process control or to evaluate (qualify) process changes rapidly. As a result, very fast electromigration tests that can be conducted at the wafer level without need for packaging are becoming very popular in manufacturing and some research environments. In order to achieve the short test times needed, very large current and temperature stresses are used ($T > 300°C$, $j > 1$ MA/cm^2). Generally, Joule (self) heating is used to attain the stress temperature. These large, stress conditions can add a host of uncertainties and unintended effects to the electromigration test, and can affect the accuracy and even meaning of the data obtained. As a result, wafer-level electromigration tests are often used merely as a qualitative indicator of electromigration strength. However, as will be seen below, if done carefully and properly, wafer-level tests can yield accurate quantitative information, particularly on electromigration transport properties. Rapid electromigration assessments made using noise measurements [101, 102] are not discussed here. This technique is not commonly employed, although significant progress has been made in this area.

6.1. *Test approaches*

Recalling Black's model [eqn (6)], the median time to failure of a metal line undergoing electromigration is a function of two independent variables, T and j. When self-heating is used in wafer-level tests, the test temperature depends on the applied current density. Thus, it is not possible to fix one independent variable while varying the other in a wafer-level test. As a result, the various wafer-level test approaches proposed in the literature are essentially algorithms to control the applied current during the course of the

test, based upon *in situ* feedback on the condition of the line under test. Those approaches are described briefly below.

6.2. *Standard Wafer-Level Electromigration Acceleration Test (SWEAT)*

The Standard Wafer-Level Electromigration Acceleration Test (SWEAT) was proposed in 1985 by Root and Turner [103]. This test approach is somewhat novel in that instead of controlling the independent variables, an attempt is made to control the dependent variable through use of eqn (6). Thus, as the test progresses, T is monitored continuously using the line itself as a thermometer and j adjusted so that the left side of eqn (6) is a constant. This test requires *a priori* knowledge of the parameters A, n and E_a, presumably obtained through classic testing on packaged test structures. The test is used as a qualitative indicator of metal performance by observing the variance between the time to failure selected and that actually obtained. Unfortunately, if a change is noted, it is not possible to ascertain which parameters (A, n, E_a or some combination) were the root cause. There is also a great danger in selecting a target time to failure that is too short which results in excessive temperatures.

6.3. *Breakdown Energy of Metals (BEM)*

The Breakdown Energy of Metals (BEM) approach was introduced by Hong and Crook [104] in 1985. The control algorithm consists of a current ramp (staircase) applied to the line under test, with self-heating used to supply stress temperatures. Because the peak current is essentially unbounded, care must be taken to limit the peak current so that the temperature does not become so large as to reach unreasonable levels, such as the melting point of aluminum. Like the SWEAT technique, the temperature is monitored at each step in the staircase. The most intriguing aspect of this approach is the calculation of the so-called energy to failure, E_f, calculated over the current ramp as

$$E_f = \frac{1}{\ell}\int_0^{t_f} I^2(t)R(t)e^{-E_a/kT(t)}dt \qquad (9)$$

where ℓ is the stripe length, t_f is the time to failure, R is the stripe resistance, I is the applied current and all other symbols have their usual meaning. The intriguing aspect is that if Black's model is correct, and $n = 2$ and E_a is known, then the energy to failure should be path independent. That is, it should not depend upon the ramp rate or end temperature, provided the diffusion mechanism does not change. This is due to the normalization of the integrand by the exponential term. Unfortunately, most users of BEM assume the value of E_a and that advantage is lost. Like the SWEAT approach, should a change be observed it is impossible to ascertain which parameter gave rise to the change. Also, because a current ramp is used, much of the test does not apply any meaningful stress to the line because of the strong dependence of temperature on applied current discussed below.

6.4. *Constant* j *and* T *approaches*

Two other approaches that might be used are to control one of the independent variables, current density or temperature, and let the other vary as it will between test structures and over the course of the test. Of the two approaches, it is advantageous to keep the test temperature constant rather than the current density constant. That is illustrated in Fig. 5, where stripe temperature is plotted vs current density for a typical wafer level test. As is evident from the figure, the current density varies by roughly 30% over the range typically used to conduct wafer level tests while the absolute temperature varies by more than 50%. If we apply this variation to eqn (6), and assume an activation energy of 0.7 eV, the variation in current density results in a 60% variation in the median time to failure while the variation in temperature results in a variation of almost three orders of magnitude. Thus, of the two independent variables, controlling the stripe temperature is preferable as errors induced by changing current density will be small. Figure 5 also illustrates why extracting the current density exponent n is very difficult using wafer-level techniques. Only a small range of current densities is attainable, and uncertainties in E_a and T can swamp out the lifetime dependence on current density. Another obvious advantage of this test approach is that the temperature can be varied and an activation energy extracted for the process.

Maintaining constant temperature is the approach used in the Wafer-Level Isothermal Joule-heated Electromigration Test (WIJET) introduced by Jones and Smith [105]. In that test, the stripe resistance is used as the thermometer and the applied current is continuously controlled to keep that resistance constant. Thus, the test might be better termed an isoresistance test. The test is certainly not truly isothermal. As voids start to grow the base resistance of the stripe increases and hot spots develop. Failure

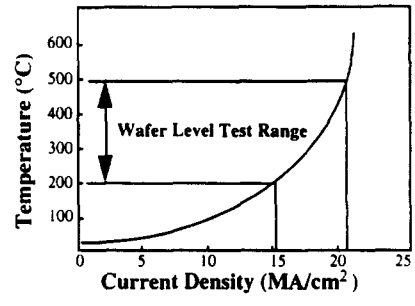

Fig. 5. Temperature as a function of current density for a typical electromigration structure. Wafer chuck temperature set at 29°C.

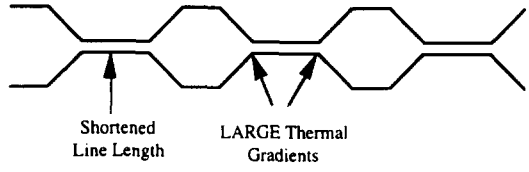

Fig. 6. Schematic of the SWEAT structure.

occurs when the void grows large enough for the resulting hot spot to reach the melting point. Our experience has been that the thermal conductivity of aluminum is high enough that local heating is not a problem until the void is so large that failure would be imminent without Joule heating effects. This test approach has yielded some very good results and will form the basis of the discussions which follow, where we will dispense with the acronym and simply refer to the isothermal test. It is interesting to note that this straightforward approach appeared in the literature two years after the other, more complicated, wafer-level test approaches.

6.5. *Test structure design*

The use of self-heating in wafer-level tests provides one of the advantages from a speed and simplicity standpoint. That is, the current density is very high, resulting in shorter times to failure, and there is no need for thermal chucks or on-chip heaters. The local temperature is very sensitive to cross-sectional area, transverse geometry, material properties and underlying dielectric thickness. Thus it is difficult to extract quantitative information from useful structures such as via chains, serpentines and lines over topography such as steps. Qualitative information can be obtained, but must be interpreted with care.

Given the above, it is surprising that one of the structures most widely used in wafer-level electromigration testing is the SWEAT structure [103], illustrated in Fig. 6. This structure is designed to yield very large thermal gradients to maximize the currents that can be forced through the narrow region. As a result, thermometry is uncertain. Indeed, there have been papers published that are concerned mainly with analytical and numerical solutions to the heat equation to yield the temperature in the center of the narrow portions of the structure as a function of the measured resistance of the structure [106–108]. An added difficulty is that the very short narrow line segments are inefficient at sampling line grain structure, defects and potential nucleation sites. Indeed, one design goal of the structure is to force failure at a pre-determined site, regardless of film microstructure.

Given the above discussion, it would appear that the ideal structure for gathering quantitative information from a wafer-level electromigration test would be a long, constant width stripe over flat topography; such a stripe would provide an adequate sample of grain structures and minimize longitudinal thermal gradients. A long stripe adequately samples grain structure and minimizes longitudinal thermal gradients. That describes the test structure most often used in classic packaged structure tests, the NIST structure standardized by Ref. [109] and shown in Fig. 7. Because the length to width ratio is so large (widths are typically on the order of 1 μm), the temperature is very uniform until the ends of the line are reached. There, the temperature rapidly drops and that gradient acts as a diffusion barrier due to decreased atomic mobility, giving a well controlled boundary condition. That boundary condition simulates the diffusion barrier termination of most metal lines found in modern IC technology. Some concern has been expressed that the large thermal gradients at the ends of the line will induce another diffusion driving force (thermomigration) and hence contaminate the results. A straightforward calculation will show that the added driving force is a third order effect, even with the large thermal gradients that occur in wafer-level tests.

6.6. *Gross defect detection*

It was noted above that wafer-level tests are very sensitive to local geometry and hence the limitation to simple test structures. That sensitivity can allow for the detection and the estimation of the size of gross defects in the sample. Such defects usually manifest themselves as failures that occur "instantaneously", that is, before the stress conditions have been reached. If a well controlled ramp to stress condition is used and the applied current at which failure occurred is captured, then with suitable thermal analysis, it is possible to calculate the size of the void that led to the failure. Such an analysis is shown in Fig. 8 for 1.2 μm wide Al–Cu–Si lines on a W barrier layer tested at Sandia. There the current needed to fuse the stripe under test is plotted as a function of void size. That current was calculated from a two-dimensional (heat flow in the longitudinal and vertical directions) thermal model. The shaded area marks the space over which electromigration tests were conducted. The dotted horizontal lines mark the current needed to fuse the tungsten barrier. The technique is not sensitive to currents below that level because the barrier layer alone can support the

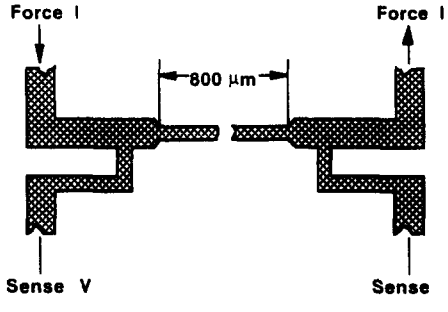

Fig. 7. The ASTM standard (NIST) electromigration test structure.

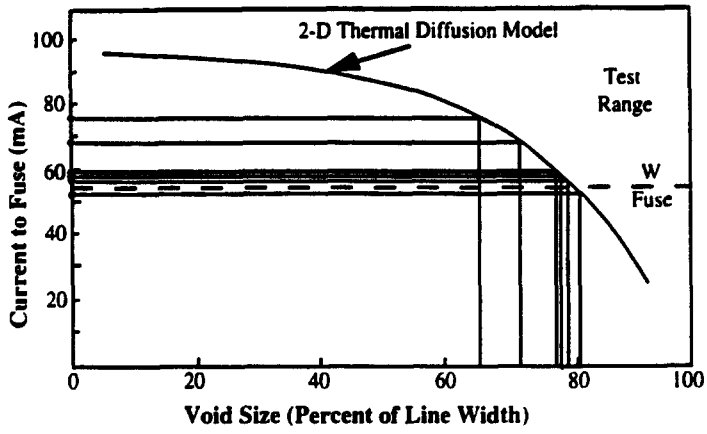

Fig. 8. Thermal analysis of early wafer-level electromigration failures.

current. Data obtained from the experiment shows the presence of voids ranging in size from 65 to 80% of the linewidth. These voids were later confirmed by cross sectioning other metal lines on the wafer. The usefulness of this technique is demonstrated by the fact that the voids could not be imaged by a scanning electron microscope during inspection due to the presence of a high atomic number anti-reflective coating on the top of the metal. Until the wafer-level electromigration test, the presence of such gross voiding was not suspected.

6.7. *Elements of an isothermal test*

We have maintained that if properly done, wafer-level techniques can yield high-quality, quantitative information on electromigration. Before presenting data to that effect, it is useful to review those additional features of the isothermal test that help ensure that high quality.

Thermometry is critical to the conduct of a successful isothermal test. Thus, the temperature coefficient of resistance (β) should be measured for each test lot. This is often the most time consuming part of the process since a probe station hot chuck requires several minutes to settle to the desired temperature. The temperature coefficient of resistance is defined implicitly by the well-known relation

$$R(T) = R(T_o)\{1 + \beta(T_o)[T - T_o]\} \qquad (10)$$

where all symbols have their usual meaning. The temperature coefficient of resistance is extracted by plotting the stripe resistance vs temperature (Fig. 9). In general, metal films are very well behaved with regard to the temperature coefficient of resistance and if expediency dictates, only one sample per lot can be done with small risk of error. The temperature coefficient of resistance can give an indication of metal quality through application of Matthiessen's rule [110]. For identical stoichiometry, β increases as the number of electron scattering sites decreases. Thus, larger values of β indicate a more perfect film.

Another parameter needed for a good wafer-level test is the structure thermal resistance. That parameter, thermal resistance, allows the stress temperature to be reached without overshoot and consequent overstress. It also allows for stripe degradation as reflected in changes in resistance at ambient to be extracted *in situ*, and provides a measure of underlying dielectric thickness if the thermal conductivity of the dielectric is known. The thermal resistance, θ, is defined implicitly by

$$\Delta T = \theta P \qquad (11)$$

where ΔT is the temperature rise above ambient and P is the power input into the stripe. The thermal resistance is extracted from a plot of ΔT vs P (Fig. 10). The thermal resistance can be measured for every structure tested during the ramp to stress conditions with no increase in test time or other experimental burden.

Extraction of the change in room temperature resistance *in situ* during a wafer-level test is important for setting the failure criterion. This prevents the control algorithm from reaching a condition where the current is reduced so much that the stripe never fails. It is also useful in setting uniform failure criteria because robust metal systems will open with very small changes in R_o. This occurs when there are few nucleation sites for voids, such as in near bamboo structures and failure occurs at the thermal diffusion barrier at the cathode. A simple thermal calculation

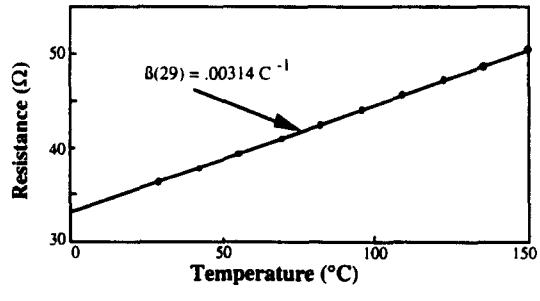

Fig. 9. Extraction of the temperature coefficient of resistance.

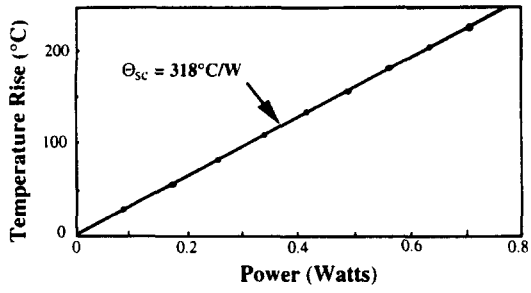

Fig. 10. Extraction of the thermal resistance.

shows that the change in R_o for an isothermal test is given by

$$\Delta R_o(t) = \frac{R_o}{1 + \beta\theta R_o[I^2(t) - I_o]} - R_o \qquad (12)$$

where I is the applied current and I_o is the applied current immediately after the target stress temperature is reached. Other expressions hold for other test techniques. Equation (12) works quite well as shown in Fig. 11 which illustrates previously unpublished Sandia data. There, eqn (12) is plotted vs ΔR_o measured after removal of the stress for metallizations fabricated with a variety of processes. The solid line in the figure denotes perfect agreement between the two.

6.8. *Wafer-level results*

The results of a wafer-level isothermal test using the techniques described above are shown in Fig. 12 [106]. The test conditions span a very large temperature range (180°C–560°C). There the time to failure normalized by the current density squared is plotted vs temperature. Each median times to failure was obtained by fitting a sample size of 20 to a log-normal distribution. The metal tested was 1.2 μm wide Al–Cu lines deposited on a W barrier layer. The lines exhibited a near bamboo grain structure. The median time to failure ranged from 6 s to one week. The vertical lines denote the 90% confidence bounds on the medians and are generally indistinguishable from the data points.

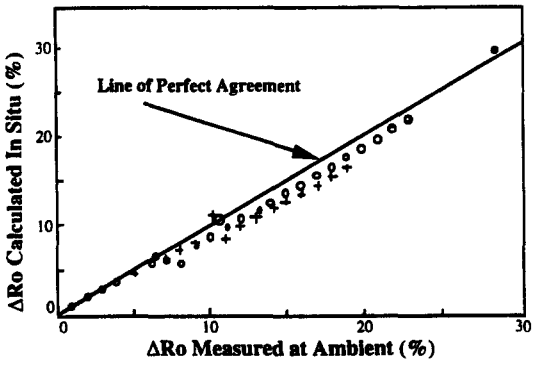

Fig. 11. The change in ambient resistance can be extracted *in situ* during an isothermal test.

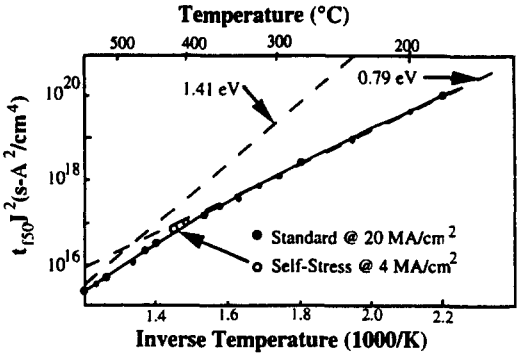

Fig. 12. Wafer-level test results over a very wide temperature range.

Figure 12 clearly illustrates the danger of testing at extreme temperatures because bulk diffusion (with its higher activation energy) starts to come into play above 350°C. Thus, measurements made at temperatures above 350°C and then extrapolated to use conditions will overestimate the time to failure unless a characterization similar to that shown in Fig. 12 is done.

One of the remarkable aspects of Fig. 12 is that simple transport physics tracks over such an extreme range of test conditions. A non-linear multiple regression was used to decompose the activation energies shown in the figure. The bulk value, 1.41 eV, agrees well with values in the literature while the value of 0.79 eV was attributed to interface diffusion due to the near bamboo grain structure of the metal tested. The diffusion coefficients for bulk and interface diffusion were extracted from the data, parameters that are very difficult to measure in aluminum because of the lack of a suitable radio-tracer.

Another significant aspect of Fig. 12 is that the failure distributions were identical across the entire measurement range. This indicates that very fast tests, on the order of seconds, can be related to much lower stress conditions. We would not advocate such an approach unless a characterization similar to that shown in Fig. 12 was conducted first. (Indeed, we rarely conduct tests above 340°C.)

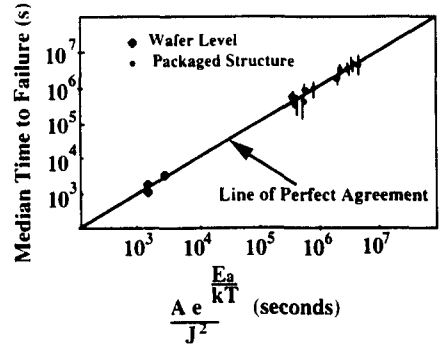

Fig. 13. Correlation experiment between wafer-level and packaged structure tests.

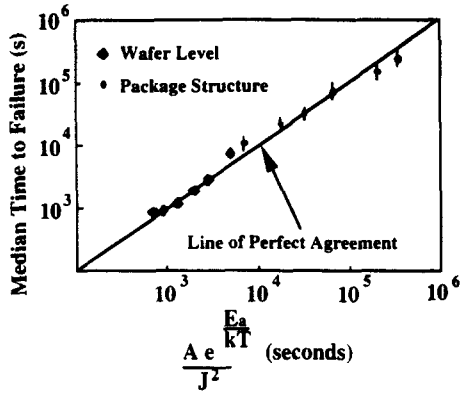

Fig. 14. Correlation experiment between wafer-level and packaged structure tests.

Figure 13 shows the result of an experiment [111] done to determine whether wafer-level tests can be correlated to slower packaged structure tests done at more benign stress conditions. The metal was 1.2 μm wide Al–Cu deposited on a W barrier with an electromigration activation energy of 0.76 eV. The measured time to failure is plotted against a fit to Black's equation. The solid line is the line of perfect agreement between the measurement and model fit. The data agree well with the model, and in this case, there is no difference between the wafer-level results and the packaged structure results.

Another example of correlation is shown in Fig. 14 for a very different metal system. The metal in this case was fine grained Al–Si without a barrier layer and was not passivated. This metal exhibited a very low activation energy (of the order of 0.3 eV) for electromigration. Again, agreement between the two approaches is quite good.

6.9. *Limitations inherent in wafer-level tests*

Thus far we have waxed enthusiastic about wafer-level tests. However, they are not a panacea and should be used in conjunction with classic packaged structure tests. We have already mentioned the inability to extract the current density dependence from wafer-level tests and the need to test only simple structures. Other inherent limitations are given below.

Wafer-level tests are insensitive to the presence of conductive refractory layers in the metal stack. Barrier layers can allow a stripe to show a very large resistance change due to massive voiding without opening. The large current densities used in wafer-level tests will fuse barrier layers as soon as the aluminum opens because those layers are very thin and have high resistivities. Thus, the local temperature can easily reach the melting point of the refractory layer. If a circuit design can tolerate a large resistance change, then a wafer-level test will grossly underestimate the lifetime of the stripe under more benign conditions due to the different failure criteria.

Similarly, the inverse current density dependence observed by Oates [19] is not detectable by wafer-level techniques. Recalling the discussion in Section 2, Oates attributed that dependence on the need to grow large voids in order to attain a failure criterion. Since a wafer-level test will fuse a line as soon as the void approaches the linewidth, the data will always reflect an inverse current density squared dependence. Again, wafer-level tests will underestimate the time to failure at more benign conditions.

If a wafer-level test is allowed to progress to an open (as is often the case) that violent event destroys all evidence of the morphology of the failure site. Thus, wafer-level tests are generally inappropriate for experiments geared towards understanding void nucleation and growth, particularly in robust metal films.

In summary, a wafer-level electromigration test can provide a great deal of useful information on the electromigration process and the quality of the metal. The wafer-level test is indispensable for process control, where speed is paramount. However, the approach should be supported by longer duration (lower stress) tests of packaged test structures to assure that no unwanted effects are being introduced or important effects missed.

7. ELECTROMIGRATION UNDER PULSED AND AC CONDITIONS

Electromigration under pulsed-dc and ac conditions is of great interest to manufacturers and users of integrated circuits. This interest arises because electromigration lifetimes are enhanced as compared to dc lifetimes during bipolar or pulsed operation. Since most metallizations are subjected to time-varying signals under operating conditions, while electromigration characterization is usually done under DC conditions, this enhancement is usually not used advantageously in the formulation of design rules. If time-varying electromigration is well understood, less stringent current density design rules can be used and hence, there can be more aggressive scaling of devices while maintaining adequate reliability design margin.

It has long been known that electromigration-induced damage can recover or anneal upon cessation or reversal of the applied stress current [112]. Relaxation of electromigration damage is not surprising since, from the diffusion equation discussed in Section 2, the driving forces due to vacancy concentration and mechanical stress gradients would cause back diffusion of vacancies and stress relief once the electromigration driving force is removed. Healing of electromigration-induced damage is not complete however because some of the material changes are irreversible [113]. Thus, if the frequency is low enough, even purely symmetric bipolar electromigration stresses will eventually result in failure as the irreversible damage grows for each half cycle.

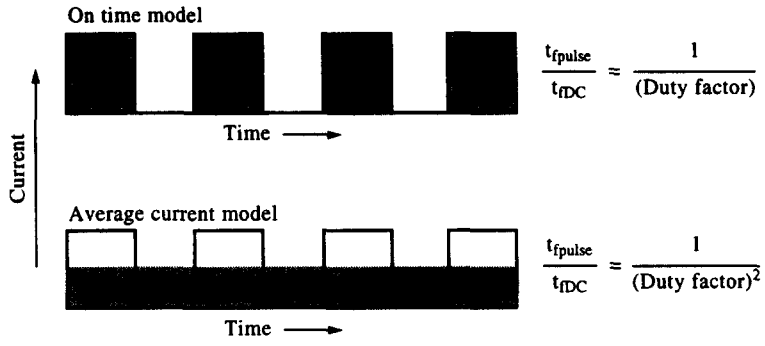

Fig. 15. Principle models for pulsed-dc electromigration.

The relaxation of electromigration damage is the source of lifetime enhancement under pulsed-dc and ac conditions. If we consider a pulsed-dc operation, the additional variables in the stress condition waveform are the frequency and duty factor (on-time as a fraction of period). The effects of frequency and duty factor on pulsed-DC electromigration are conveniently discussed using a modified form of eqn (6)

$$t_{50} = \frac{A}{j^n r^m} e^{E_a/kT} \tag{13}$$

where r is the duty factor and m is a constant. If electromigration depends on frequency, we would expect A to be frequency-dependent, as that term contains factors relating to the void nucleation and growth mechanism [114]. If the electromigration duty factor dependence is simply explained by damage occurring only during the "on" portion of the current pulse with no annealing of damage during the "off" portion, then $m = 1$ in eqn (13); this is sometimes called the "on-time" model. That model is shown schematically in Fig. 15 where the shaded areas represent the effective electromigration driving force. In the low frequency limit, the on-time model is expected to be applicable because the pulse is on long enough to cause severe irreversible damage. In the extreme limit, where the period is twice the electromigration lifetime, the on-time model must hold.

If annealing (or back diffusion) does occur, then m will be greater than 1, and the pulse response is said to be enhanced. If $m = n$, then eqn (1) yields the average current density model where the time average of the current (expectation value) governs the duty factor response. The latter case can be expressed simply as

$$t_{50} = \frac{A}{|j|^n} e^{E_a/kT} \tag{14}$$

for an arbitrary waveform. Note that eqn (14) implies infinite electromigration life under symmetric bipolar current stresses. This is what is expected in the extremely high frequency limit, where the migrating atom is subjected to multiple waveform periods during a diffusion jump and responds to the average.

Electromigration frequency response measurements reported in the literature have yielded results consistent with the above remarks. Most measurements have been limited to moderate frequencies (< 10 MHz) with the exception of Pierce *et al.* [115], who extended the range to 500 MHz using current drive circuitry integrated into the test structure [116]. In general, the lifetime is constant with respect to frequency, providing a 2 times lifetime improvement above dc lifetime for 50% duty factor (on-time model), until a transition frequency (f_o) is reached, where it increases to a higher value [117–120]. It is generally assumed that the increase in lifetime occurs when the "on" pulse width during one period falls below the characteristic time constant for the vacancy concentration to reach equilibrium [119]. That increase usually occurs in the range of 1 Hz to a few kHz. One notable exception was observed by Pierce *et al.* [115], where the transition frequency was roughly 1–10 MHz (Fig. 16). They noted that, since significant Joule heating (*ca.* 20°C) was used in the experiments, the high transition frequency could be due to thermal effects related to the thermal relaxation time of the structure (approximately 1 μs). Those effects would mask a transition occurring below 1 MHz.

The data on duty factor response have shown far more variation. The early work of Miller [121]

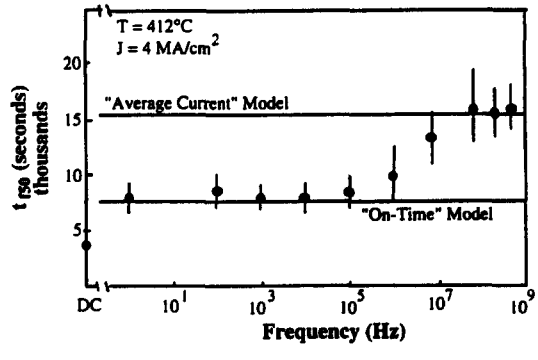

Fig. 16. Electromigration lifetime as a function of frequency [115].

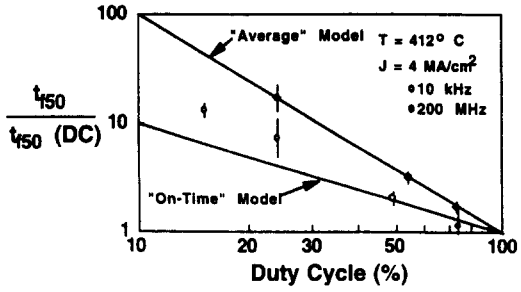

Fig. 17. Electromigration lifetime as a function of duty factor.

generated considerable excitement, as he found an exponential dependence of lifetime with duty factor, with very large enhancements at low duty factors. Experimental work since then [118, 120, 122–128] has not shown such large enhancements, with the value of m usually around two. Larger values of m (from three to five) have also been reported [122, 123, 127]. When m deviates from two, it appears to be strongly correlated to the current density exponent, n. Based on those results, it is generally assumed that the electromigration response under pulsed conditions is a function of the average current density at high frequencies, which results when $m = n$. An example of duty factor data [115] which demonstrate the average current density model at high frequencies is shown in Fig. 17.

The observed duty factor enhancement in electromigration lifetime has led to a variety of models. Most are based upon consideration of the time constant associated with vacancies attaining equilibrium [121, 124, 128, 129]. With one exception [121], all predict $m = 2$ for pulse widths less than the vacancy response time. A different approach was taken by Clement [130], who solved the forced diffusion equation numerically with two simple boundary conditions. He also obtained $m = 2$. Thus, simple transport theory yields the same result as vacancy relaxation methods.

There continues to be a great deal of interest in electromigration response under time varying signals. The added reliability margin due to pulsed-dc or ac operation is crucial in obtaining the design margins needed to maintain reliability for the aggressive scaling of integrated circuit metallization that will occur over the next 10 years. A better understanding, both theoretical and experimental, of lifetime enhancement under time varying signals is needed in developing the design rules needed to maintain those margins with confidence.

8. CONCLUSIONS

We have reviewed the subject of electromigration from the standpoint of the reliability engineer, focusing on those areas of greatest applicability to the manufacturing environment. As a result, emphasis was placed on empirical data concerning metal stripe geometry, structure and composition impacts on electromigration lifetime. Much was said on the subject of fast, wafer-level tests. Those tests, if performed carefully, can provide quantitative information on the electromigration behavior of a metal process in a timely enough fashion to be useful for process control and qualification. The final subject reviewed was the effect of time-varying current waveforms on electromigration lifetimes. That subject is of great importance as lifetimes are greater for pulsed-dc and ac waveforms. A reasonable physical understanding of that behavior allows for relaxation of design rules for a given reliability requirement which in turn allows for higher integrated circuit densities.

The conclusion that can be drawn is that electromigration is a very complex phenomenon where the experimental tools are inadequate to resolve the impact of the many factors governing the process. For the moment, electromigration will continue to be an empirical subject, with theoretical work providing some guidance, but not final solutions. Because of the continuous, aggressive scaling of integrated circuit dimensions, additional work and understanding is essential if the devices are to perform reliably.

REFERENCES

1. *The National Technology Roadmap for Semiconductors*. Semiconductor Industry Association, San Jose, CA, 1994, pp. 94–104.
2. Baldini, G. L., de Munari, I., Scorzoni, A. and Fantini, F., Electromigration in thin-film for microelectronics. *Microelectron. Reliab.*, 1993, **33**(11/12), 1779–1805.
3. Scorzoni, A., Neri, B., Caprile, C. and Fantini, F., Electromigration in thin-film interconnection lines: models, methods and results. *Mat. Sci. Reports*, 1991, **7**, 143–220.
4. Blech, I. A. and Meieran, E. S., Electromigration in thin aluminum films. *J. Appl. Phys.*, 1968, **40**(2), 485–491.
5. Huntington, H. B. and Grone, A. R., Current-induced marker motion in gold wires. *J. Phys. Chem. Solids*, 1961, **20**(1/2), 76–87.
6. Sorbello, R. S., Theory of the direct force in electromigration. *Phys. Rev. B.*, 1985, **31**(9), 798–804.
7. Verbruggen, A. H., Fundamental questions in the theory of electromigration. *IBM Res. Develop.*, 1988, **32**(1), 93–98.
8. Landauer, R., Comment on Lodder's "exact" electromigration theory. *Solid State Commun.*, 1989, **72**(9), 867–868.
9. De Munari, I., Scorzoni, A., Tamarri, F., Govoni, D., Corticelli, F. and Fantini, F., Drawbacks to using NIST electromigration test-structures to test bamboo metal lines. *IEEE Trans. Elect. Dev.*, 1994, **41**(12), 2276–2280.
10. Blech, I. A., Electromigration in thin aluminum films on titanium nitride. *J. Appl. Phys.*, 1975, **47**(4), 1203–1208.
11. Kirchheim, R., Stress and electromigration in Al-lines of integrated circuits. *Acta Metall. Mater.*, 1992, **40**(2), 309–323.
12. Black, J. R., Mass transport of aluminum by momentum exchange with conducting electrons. *Proc. 6th Ann. Int. Rel. Phys. Symp.*, 1967, pp. 148–159.

13. Lloyd, J. R., Reliability modeling for electromigration failure. *Quality and Reliab. Engng Int*, 1994, **10,** 303–308.
14. Shatzkes, M. and Lloyd, J. R., A model for conductor failure considering diffusion concurrently with electromigration in a current exponent of 2. *J. Appl. Phys.*, 1986, **59**(11), 3890.
15. Lloyd, J. R. and Kitchin, J., The finite electromigration boundary value problem. *J. Mater. Res.*, 1994, **9**(3), 563–569.
16. Dwyer, V. M., Wang, F.-S. and Donaldson, P., Electromigration failure in a finite conductor with a single blocking boundary. *J. Appl. Phys.*, 1994, **76**(11), 7305–7310.
17. Trattles, J. T., O'Neill, A. G. and Mecrow, B. C., Computer simulation of electromigration in thin-film metal conductors. *J. Appl. Phys.*, 1994, **75**(12), 7799–7804.
18. Lloyd, J. R., Electromigration physical modeling of failure in thin film structures. *SPIE Vol.* 1596 *Metallization: Performance and Reliability Issues for VLSI and ULSI*, 1991, 106–117.
19. Oates, A. S., Current density dependence of electromigration failure of submicron width, multilayer aluminum alloy conductors. *Appl. Phys. Lett.*, 1995, **66**(12), 1475–1477.
20. Li, C.-Y., Børgesen, P. and Korhonen, M. A., Electromigration-induced failure in passivated aluminum-based metallizations—the dependence on temperature and current density. *Appl. Phys. Lett.*, 1992, **61**(4), 411–413.
21. Lloyd, J. R. and Kitchin, J., The electromigration failure distribution: the fine-line case. *J. Appl. Phys.*, 1991, **69**(4), 2117–2127.
22. Børgesen, P., Korhonen, M. A. and Lin, C.-Y., Statistical distributions of stress and electromigration induced failure. *SPIE Vol.* 1805 *Submicrometer Metallization*, 1992, pp. 130–153.
23. Clement, J. J., Atakov, E. M. and Lloyd, J. R., Electromigration reliability of VLSI interconnect. *Digital Technical J.*, 1992, **4**(2), 114–125.
24. Agarwala, B. N., Attardo, M. J. and Ingraham, A. P., Dependence of electromigration-induced failure time on length and width of aluminum thin-film conductors. *J. Appl. Phys.*, 1970, **41,** 3954–3960.
25. Agarwala, B. N., Attardo, M. J. and Ingraham, A. P., *J. Appl. Phys.*, 1970, **41,** 3954–3960.
26. Learn, A. J. and Shepherd, W. H., Reduction of electromigration-induced failure in aluminum metallization through anodization. *Proc. 9th Ann. Rel. Phys. Symp.*, 1971, pp. 129–134.
27. Kakar, A. K., Electromigration studies on aluminum–copper stripes. *Solid State Tech.*, May 1973, 47–52.
28. LaCombe, D. J. and Parks, E. L., The distribution of electromigration failures. *Proc. of 1986 Int. Rel. Phys. Symp.*, 1986, pp. 1–6.
29. Arzigian, J. S., Aluminum electromigration lifetime variation with linewidth: the effects of changing stress conditions. *Proc. 1983 Int. Reli. Phys. Symp.*, 1983, pp. 32–35.
30. Schafft, H. A., Staton, T. C. and Mandel, J., Reproducibility of electromigration measurements. *IEEE Trans. on Elect. Dev.*, 1987, **ED-34,** 673–681.
31. Black, J. R., Electromigration—a brief survey and some recent results. *IEEE Trans. on Elect. Dev.*, 1969, **ED-16**(4), 338.
32. Black, J. R., Current limitations of thin film conductors. *Proc. 1982 Int. Rel. Phys. Symp.*, 1982, pp. 300–306.
33. Woods, M. H., The implications of scaling on VLSI reliability. *Int. Reli. Phys. Symp. Tutorials*, Apr. 1984, pp. 6–15.
34. Gardner, D. S., Meindl, J. D. and Saraswat, K. C., Interconnection and electromigration scaling theory. *Trans. Elect. Dev.*, 1987, **ED-34**(3), 633–643.
35. Vaidya, S., Fraser, D. B. and Sinha, A. K., Electromigration resistance of fine-line Al for VLSI applications. *Proc. 1980 Int. Rel. Phys. Symp.*, 1980, pp. 165–170.
36. Kinsbron, E., A model for the width dependence of electromigration lifetimes in aluminum thin-film stripes. *Appl. Phys. Lett.*, 1980, **36**(12), 968–970.
37. Schafft, H. A., Thermal analysis of electromigration test structures. *IEEE Trans. Elect. Dev.*, 1987, **ED-34,** 664–672.
38. Rodbell, K. P. and Shatnyski, S. R., A new method for detecting electromigration failure in VLSI metallization. *IEEE J. Solid-State Cir.*, 1984, **SC-19**(1), 98–99.
39. D'Haeger, V., Stulens, H., De Ceuninck, W., De Schepper, L., Tielemands, L., Gallopyn, G., De Pauw, P. and Stals, L., Use of early resistance and early TCR changes to predict reliability of on-chip interconnects. *Quality and Reliab. Engng Int.*, 1994, **10**(4), 309–314.
40. Maiz, J. A. and Sabi, B., Electromigration testing of Ti/Al–Si metallization for integrated circuits. *Proc. 25th Ann. Rel. Phys. Symp.*, 1987, pp. 145–153.
41. Ondrusek, J. C., Nishimura, A., Hoang, H. H., Sugiura, T., Blumenthal, R., Kitagawa, H. and McPherson, I. W., Effective kinetic variations with stress-duration for multilayered metallizations. *Proc. 26th Ann. Rel. Phys. Symp.*, 1988, pp. 179–184.
42. Towner, J. M., Electromigration-induced short circuit failure. *Proc. of 1985 Int. Rel. Phys. Symp.*, 1985, pp. 81–86.
43. Towner, J. M., The importance of the short-circuit failure mode in aluminum electromigration. *J. Vac. Sci. Technol.*, 1987, **85**(6), 1696–1700.
44. Attardo, M. J., Rutledge, R. and Jack, R. C., Statistical metallurgical model for electromigration failure in aluminum thin-film conductors. *J. Appl. Phys.*, 1971, **42**(11), 4343–4349.
45. Schoen, J. M., Monte Carlo calculations of structure-induced electromigration failure. *J. Appl. Phys.*, 1980, **51**(1), 513–521.
46. Nikawa, K., Monte Carlo calculations based on the generalized electromigration failure model. *Proc. of 1981 Int. Rel. Phys. Symp.*, 1981, pp. 175–181.
47. Hu, C., Berkeley Reliability Simulator BERT: An IC reliability simulator. *Microelect. J.*, 1992, **23**(2), 97–102.
48. Liew, B. K., Fang, P., Cheung, N. and Hu, C., Circuit reliability simulator for interconnect, via, and contact electromigration. *IEEE Trans. Elect. Dev.*, 1992, **39**(11), 2472–2479.
49. Choi, G. S. and Ravishankar, K., Wear-out simulation environment for VLSI designs. *Int. Symp. Fault-Tol. Comp.*, 1993, pp. 320–329.
50. Hajj, I. N., Rao, V. B., Iimura, R., Cha, H. and Burch, R., A system for electromigration analysis in VLSI metal patterns. *Proc. Cust. Int. Cir. Conf.*, 1991, pp. 4.4.1–4.4.4.
51. Hwang, J. P., REX—A VLSI parasitic extraction tool for electromigration and signal analysis. *Proc.-Des. Auto. Conf.*, 1991, pp. 717–722.
52. d'Heurle, F. and Ames, I., Electromigration in single-crystal aluminum films. *Appl. Phys. Lett.*, 1970, **16,** 80–81.
53. Baerg, W. and Wu, K., Using metal grain size distributions to predict electromigration performance. *Solid State Tech.*, Mar. 1991, 35–37.
54. Cho, J. and Thompson, C. V., Grain size dependence of electromigration-induced failures in narrow interconnects. *Appl. Phys. Lett.*, 1989, **54**(25), 2577–2579.
55. Wu, K., Baerg, W. and Jupiter, P., Effects of aluminum microstructure on electromigration using a

new reactive ion etching and scanning electron microscopy technique. *Appl. Phys. Lett.*, 1991, **58**(12), 1299–1301.
56. Attardo, M. J. and Rosenberg, R., Electromigration damage in aluminum film conductors. *J. Appl. Phys.*, 1970, **41**, 2381–2386.
57. Howard, J. K. and Ross, R. F., The effect of preferred orientation on the rate of electromigration and its implication to the cracked-stripe failure mode. *IBM Tech. Rep.*, Mar. 1968, **22**, 601.
58. Campbell, A. N., Mikawa, R. E. and Knorr, D. B., Relationship between texture and electromigration lifetime in sputtered Al–1% Si thin films. *J. Elect. Mat.*, 1993, **22**(6), 589–596.
59. d'Heurle, F. M., Electromigration and failure in electronics: an introduction. *Proceedings of the IEEE*, Oct. 1971, Vol. 59, No. 10, pp. 1409–1418.
60. Comello, V., *Semicond. Int.*, June 1990, 30.
61. Learn, A. J. and Shepherd, W. H., Reduction of electromigration-induced failure in aluminum metallization through anodization. *Proc. 9th Ann. Rel. Phys. Symp.*, 1971, pp. 129–134.
62. Wada, T., Higuchi, H. and Ajiki, T., The effect of oxygen (O_2) plasma treatment against electromigration. *Proc. 1985 IEEE Elect. Comp. Conf.*, 1985, pp. 32–36.
63. d'Heurle, F. M., The effect of copper additions on electromigration in aluminum thin films. *Met. Trans.*, 1971, **2**, 683–689.
64. d'Heurle, F. M., Ainslie, N. G., Gangulee, A. and Shine, M. C., Activation energy for electromigration failure in aluminum films containing copper. *J. Vac. Sci. Tech.*, 1971, **9**(1), 289–293.
65. Agarwala, B. N., Patnaik, B. and Schnitzel, R., Effect of microstructure on the electromigration life of thin-film Al–Cu conductors. *J. Appl. Phys.*, 1972, **43**(4), 1487–1493.
66. Nemoto, T. and Nogami, T., Segregation of Cu to grain boundaries by aging treatment and its effect on EM resistance for AlCu/TiN lines. *Proc. 1994 Int. Rel. Phys. Symp.*, 1994, pp. 207–212.
67. Gangulee, A. and d'Heurle, F. M., Effect of alloy additions on electromigration failures in thin aluminum films. *Appl. Phys. Lett.*, 1971, **19**(3), 76–77.
68. d'Heurle, F. M. and Gangulee, A., Effects of complex alloy additions on electromigration in aluminum thin films. *Proc. 1972 Int. Rel. Phys. Symp.*, 1972, pp. 165–170.
69. Dance, B., New alloy for reliable fine-line interconnects. *Semi. Inter.*, Sept. 1995, 66.
70. Ghate, P. B. and Blair, J. C., Electromigration testing of TiW/Al and TiW/AlCu conductors. *Thin Solid Films*, 1978, **55**(113), 113–123.
71. Hoang, H. H. and McDavid, J. M., Electromigration in multilayer metallization systems. *Solid State Tech.*, Oct. 1987, 121–126.
72. Armstrong, N. P., Evaluation of TiW plus Al/Cu electromigration performance. *Quality Reliab. Engng Int.*, 1991, **7**(4), 281–286.
73. Olowwolafe, O. J., Lee, C., Kawasaki, H., Gelator, C., Blumental, R., Theordore, N. D. and Gregory, R. B., Effect in TiN anneal ambient on the microstructure and electromigration performance of Al-based alloys. *Proc. of Mat. Res. Society*, 1993, pp. 95–100.
74. Kikkawa, T., Endo, N., Yamazaki, T. and Watanabe, H., Comparison of refractory metal and silicide capping effects on aluminum metallizations. *Proc. IEEE VMIC Conf.*, 1989, pp. 463–469.
75. Howard, J. K., White, J. F. and Ho, P. S., Intermetallic compounds of Al and transitions metals: effect of electromigration in 1–2 μm wide lines. *J. Appl. Phys.*, 1978, **49**(7), 4083–4093.
76. Gangulee, A., Ho, P. S. and Howard, J. K., Electromigration resistance in gold thin film conductors. *U.S. Patent* N.4,166,279, 1979.
77. Tao, J., Cheung, N. and Hu, C., Electromigration characteristics of copper interconnects. *IEEE Elect. Dev. Lett.*, 1993, **14**(5), 249–251.
78. Park, C. W. and Vook, R. W., Electromigration-resistant Cu–Pd alloy films. *Thin Solid Films*, 1993, **226**(2), 238–247.
79. Merchant, P. P., Electromigration: an overview. *Hew. Pack. J.*, Aug. 1982, 28–30.
80. Engeler, W. E. and Brown, D. M., Performance of refractory metal multilevel interconnection systems. *IEEE Trans. Elect. Dev.*, 1972, **ED-19**, 54–61.
81. Kim, M. J., Skelly, D. W. and Brown, D. M., Electromigration of bias-sputtered Al and comparisons with others. *Proc. 1987 Int. Rel. Phys.*, 1987, 126–129.
82. Spitzer, S. M. and Schwartz, S., The effects of dielectric overcoating on electromigration in aluminum interconnections. *IEEE Trans. Elect. Dev.*, 1969, **ED-16**, 348–350.
83. Ainslie, N. G., d'Heurle, F. M. and Wells, O. C., Coating, mechanical constraints, and pressure effects on electromigration. *Appl. Phys. Lett.*, 1972, **20**(4), 173.
84. Lloyd, J. R. and Smith, P. M., The effect of passivation thickness on the electromigration lifetime of AlCu thin film conductors. *J. Vac. Sci. Tech.*, 1983, **A1**(2), 455–458.
85. Schafft, H. A., Younkins, C. D. and Grant, T. C., Effect of passivation and passivation defects on electromigration failure in aluminum metallization. *Proc. 1984 Int. Rel. Phys. Symp.*, 1984, pp. 250–255.
86. Lloyd, J. R., Electromigration in Al–Cu thin films with polyimide passivation. *Thin Solid Films*, 1982, **91**, 175–182.
87. Black, J. R., Electromigration failure modes in aluminum metallization for semiconductor devices. *Proc. IEEE*, 1969, **57**(9), 1587–1594.
88. Vaidya, S. and Sinha, A. K., Electromigration induced leakage at shallow junction contacts metallized with aluminum/poly-silicon. *Proc. 1982 Int. Rel. Phys. Conf.*, 1982, pp. 50–54.
89. Gargini, P. A., Tseng, C. and Woods, M. H., Elimination of silicon electromigration in contacts by the use of an interposed barrier metal. *Proc. 1982 Int. Rel. Phys. Conf.*, 1982, pp. 66–76.
90. Ghate, P. B., Metallization for very large scale integrated circuits. *Thin Solid Films*, 1982, **93**, 359–383.
91. Babcock, S. E. and Tu, K. N., Titanium–tungsten contacts to Si: the effects of alloying on Schottky contact and on silicide formation. *J. Appl. Phys.*, 1982, **53**(10), 6898–6905.
92. Pramanik, D. and Jain, V., Barrier metals for ULSI: deposition and manufacturing. *Solid State Tech.*, Jan. 1993, 73–82.
93. Pramanik, D. and Jain, V., Barrier metals for ULSI: processing and reliability. *Solid State Tech.*, May 1991, 97–102.
94. Ting, C. Y. and Wittmer, M., Investigation of the Al/$TiSi_2$/Si contact system. *J. Appl. Phys.*, 1983, **54**(2), 937–943.
95. Oates, A., Electromigration failure of contacts and vias in submicron integrated circuit metallizations. *Microelectron. Reliab.*, 1996, **36**(7/8), 925–953.
96. *ibid.*
97. May, J., Electromigration characteristics of vias in Ti:W/Al–Cu(2 wt %) multilayered metallization. *Proc. Int. Rel. Phys. Symp.*, 1991, pp. 91–96.
98. Martin, C. A. and McPherson, J. W., Via electromigration performance of Ti/W/Al–Cu(2%) multilayered metallization. *Proc. 1989 VMIC Conf.*, 1989, pp. 168–175.

99. Tao, J., Young, K. K., Cheung, N. and Hu, C., Electromigration reliability of tungsten and aluminum vias and improvement under AC current stress. *IEEE Trans. Elect. Dev.*, 1993, **40**(8), 1398–1405.
100. Graas, C. D., Le, H. A., McPherson, J. W. and Havemann, R. H., Electromigration reliability improvement of W-plug vias by titanium layering. *Proc. 1994 Int. Rel. Phys. Symp.*, pp. 173–177.
101. Cottle, J. G. and Klonaris, N., Effect of electro- and stress migration forces on the $1/f$ noise of patterned thin metal films. *Thin Solid Films*, 1994, **253**(1–2), 513–517.
102. Diligenti, A., Bagnoli, P E., Neri, B., Beal, S. and Mantellassi, L., Study of electromigration in aluminum and aluminum–silicon thin film resistors using noise techniques. *Solid-State Elect.*, 1989, **32**(1), 11–16.
103. Root, B. J. and Turner, T., Wafer level electromigration tests for production monitoring. *Proc. 1985 Rel. Phys. Symp.*, 1985, pp. 100–107.
104. Hong, C. C. and Crook, D. L., Breakdown energy of metal (BEM)—a new technique for monitoring metallization reliability at wafer level. *Proc. 1985 Rel. Phys. Symp.*, 1985, pp. 108–114.
105. Jones Jr, R. E. and Smith, L. D., A new wafer-level iso-thermal Joule-heated electromigration test for rapid testing of integrated-circuit interconnect. *J. Appl. Phys.*, 1987, **61**(9), 4670–4678.
106. Crowell, C. R., Shih, C. C. and Tyree, V., Simulation and testing of temperature distributions and resistance versus power for SWEAT and related Joule-heated metal-on-insulator structures. *Proc. 1990 Int. Rel. Phys. Symp.*, 1990, pp. 37–43.
107. Dion, M. J., EXTRA-EM: extraction of temperature and resistance for acceleration of electromigration at wafer-level. *Proc. 1991 Int. Rel. Phys. Symp.*, 1991, pp. 287–297.
108. Katto, H., Harada, M. and Higuchi, Y., Wafer-level, JRAMP & J-constant electromigration testing of conventional & SWEAT patterns assisted by a thermal & electrical simulator. *Proc. 1991 Int. Rel. Phys. Symp.*, 1991, pp. 298–305.
109. *Standard Guide for the Design of Flat, Straight-Line Test Structures for Detecting Metallization Open-Circuit or Resistance-Increase Failure Due to Electromigration*. ASTM Standard F1259-89. Annual Book of ASTM Standards, 1990, Vol. 10.04, pp. 669–670.
110. Ascroft, N. W. and Mermin, N. D., *Solid State Physics*. Holt, Rinehart & Winston, N.Y., 1976, pp. 323–324.
111. Pierce, D. G. and Brusius, P.G., Correlation between highly and moderately accelerated electromigration tests. *IEEE Elect. Dev. Lett.*, 1993, **14**(6), 277–279.
112. English, A. T., Tai, K. L. and Turner, P. A., *Appl. Phys. Lett.*, 1972, **21**, 15.
113. Li, Z., Bauer, C. L. and Mahajan, S., Degradation and subsequent healing by electromigration in Al-1 wt % Si thin films. *J. Appl. Phys.*, 1992, **72**(1), 1821–1832.
114. Lloyd, J. R., Electromigration failure. *J. Appl. Phys.*, 1991, **69**(11), 7601–7604.
115. Pierce, D. G., Snyder, E. S., Swanson, S. E. and Irwin, L. W., Wafer-level pulsed-DC electromigration response at very high frequencies. *Proc. 1994 Ann. Rel. Phys. Symp.*, 1994, pp. 198–206.
116. Snyder, E. S., Pierce, D. G., Campbell, D. V. and Swanson, S. E., Self-stressing structures for electromigration to 500 MHz. *1994 IEEE International Test Structure Conference*, March 1994.
117. Tao, J., Cheung, N. W. and Hu, C., Electromigration characteristics of copper interconnects. *IEEE Elect. Dev. Lett.*, 1993, **14**(5), 249–251.
118. Suehle, J. S. and Schafft, H. A., Current density dependence of electromigration t50 enhancement due to pulsed operation. *Proc. 28th Ann. Rel. Phys. Symp.*, 1990, pp. 106–110.
119. Suehle, J. S. and Schafft, H. A., The electromigration damage response time and implications for DC and pulsed characterizations. *Proc. 1989 Int. Rel. Phys. Symp.*, 1989, pp. 229–233.
120. Maiz, J. A., Characterization of electromigration under bidirectional (BC) and pulsed unidirectional (PDC) currents. *Proc. 27th Ann. Rel. Phys. Symp.*, 1989, pp. 220–228.
121. Miller, R. J., Electromigration failure under pulse test conditions. *Proc. 16th Ann. Rel. Phys. Symp.*, 1978, pp. 241–247.
122. Kwok, T., Chan, K. K., Chan, H. and Simko, J., Thermal stress-induced and electromigration-induced void-open failures in Al and Al–Cu fine lines. *J. Vac. Sci. Tech.*, 1991, **A9**(4), 2523–2526.
123. Ting, L. M., May, J. S., Hunter, W. R. and McPherson, J. W., AC electromigration characterization and modeling of multilayered interconnects. *Proc. 1993 Ann. Rel. Phys. Symp.*, 1993, pp. 311–316.
124. Liew, B. K., Cheung, N. W. and Hu, C., Effects of self-heating on integrated circuit metallization lifetimes. *Proc. 1989 IEDM*, 1989, pp. 323–326.
125. Hatanaka, K., Noguchi, T. and Maeguchi, K., A generalized lifetime model for electromigration under pulsed-DC/AC stress conditions. *Proc. Symp. VLSI Tech.*, 1990, pp. 19–20.
126. Towner, J. M. and van der Ven, E. P., Aluminum electromigration under pulsed D.C. conditions. *Proc. 21st Ann. Rel. Phys. Symp.*, 1983, pp. 33–39.
127. Brooke, L., Pulse current electromigration failure model. *Proc. 25th Ann. Rel. Phys. Symp.*, 1987, pp. 136–139.
128. Wu, C. J. and McNutt, M. J., Effects of substrate thermal characteristics on electromigration behavior of Al thin film conductors. *Proc. 21st Ann. Rel. Phys. Symp.*, 1983, pp. 24–31.
129. Liew, B. K., Cheung, N. W. and Hu, C., Electromigration interconnect failure under pulse test conditions. *Proc. 1988 Symposium on VLSI Technology*, 1988, pp. 59–60.
130. Clement, J. J., Vacancy supersaturation model for electromigration failure under DC and pulsed DC stress. *J. Appl. Phys.*, 1992, **71**(9), 4264–4268.