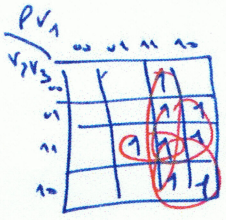
a)

PV_1	V_2	V_3	De
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1
1	1	0	1
1	1	1	1



$De = PV_1 + PV_2 + PV_3 + V_1V_2V_3$

$De = \overline{\overline{PV_1}\ \overline{PV_2}\ \overline{PV_3}\ \overline{V_1V_2V_3}}$ en NANDs de dos entradas

b) $\overline{PV_1} \cdot \overline{PV_2} = \overline{\overline{PV_1 \cdot PV_2}\ \overline{PV_1 \cdot PV_2}}$

$\overline{V_1V_2V_3} = \overline{\overline{V_1V_2}\ \overline{V_1V_2} \cdot V_3}$

$\overline{PV_3} \cdot \overline{V_1V_2V_3} = \overline{PV_3\ \overline{V_1V_2V_1V_2 \cdot V_3} \cdot \overline{PV_3}\ \overline{\overline{V_1V_2}\overline{V_1V_2} \cdot V_3}}$

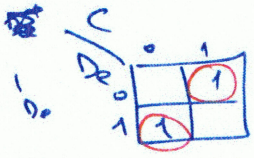
$De = \overline{\overline{PV_1\ PV_2} \cdot \overline{PV_1 \cdot PV_2}} \cdot \overline{PV_3 \cdot \left(\overline{\overline{V_1V_2}\ \overline{V_1V_2}} \cdot V_3\right)} \cdot \overline{PV_3 \cdot \left(\overline{\overline{V_1V_2}\ \overline{V_1V_2}} \cdot V_3\right)}$

Si introducimos un bit con interrupción secreta que puede cambiar la salida a voluntad

C	De	De'
0	0	0
0	1	1
1	0	1
1	1	0

C=0 no cambia De

C=1 si cambia De



$De' = \bar{C}De + \bar{De}C = C \oplus De$

resta "xor"