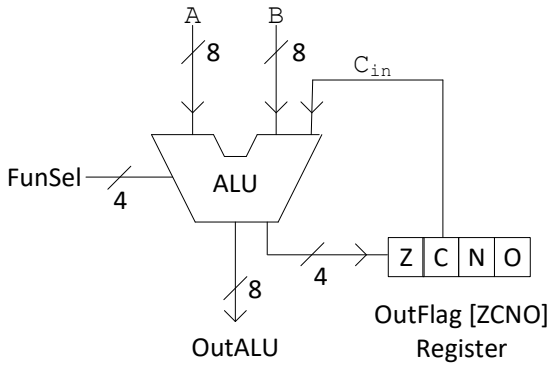
BLG222E Computer Organization

Project 2

Due Date: 30.04.2020, 08:00

(Part-1) Design an Arithmetic Logic Unit (ALU) that has two 8-bit inputs and an 8-bit output. The ALU is shown on the left side of Figure 1. The ALU functions and the flags that will be updated (i.e., **-** means that the flag will not be affected and √ means that the flag changes based on the OutALU) are given on the right side of Figure 1:

- **FunSel** selects the function of the ALU.
- **OutALU** shows the result of the operation that is selected by **FunSel** and applied on A and/or B inputs.
- **Z (zero)** bit is set if **OutALU** is zero (e.g., **NOT B** is zero).
- **C (carry)** bit is set if **OutALU** sets the carry (e.g., **LSL A** produces carry).
- **N (negative)** bit is set if the ALU operation generates a negative result (e.g., **A–B** results in a negative number).
- **O (overflow)** bit is set if an overflow occurs (e.g., **A+B** results in an overflow)**.**
- Note that **Z|C|N|O** flags are stored in a **register!**



FunSel	OutALU	Z	C	N	O
0000	A	√	–	√	–
0001	B	√	–	√	–
0010	NOT A	√	–	√	–
0011	NOT B	√	–	√	–
0100	A + B	√	√	√	√
0101	A + B + Carry	√	√	√	√
0110	A - B	√	√	√	√
0111	A AND B	√	–	√	–
1000	A OR B	√	–	√	–
1001	A XOR B	√	–	√	–
1010	LSL A	√	√	√	–
1011	LSR A	√	–	√	–
1100	ASL A	√	–	√	–
1101	ASR A	√	–	–	√
1110	CSL A	√	√	√	√
1111	CSR A	√	√	√	√

Figure 1: The ALU (Left) and its characteristic table (Right)

(Circular | **A**rithmetic | **L**ogical) **S**hift (**L**eft | **R**ight) operations are depicted in Figure 2, *Figure 3, and Figure 4*.

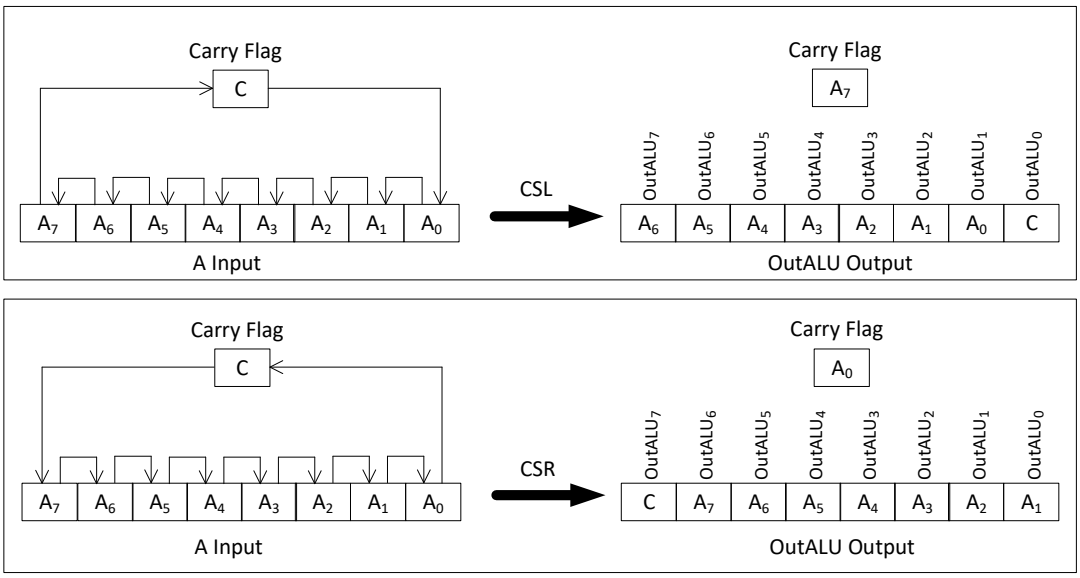


Figure 2: Circular Shift Operations

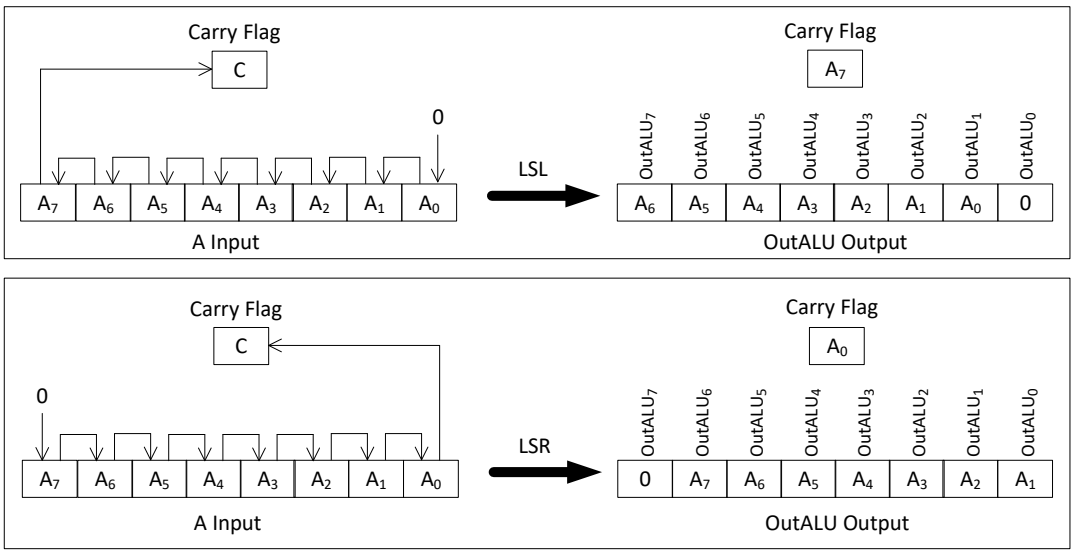


Figure 3: Logical Shift Operations

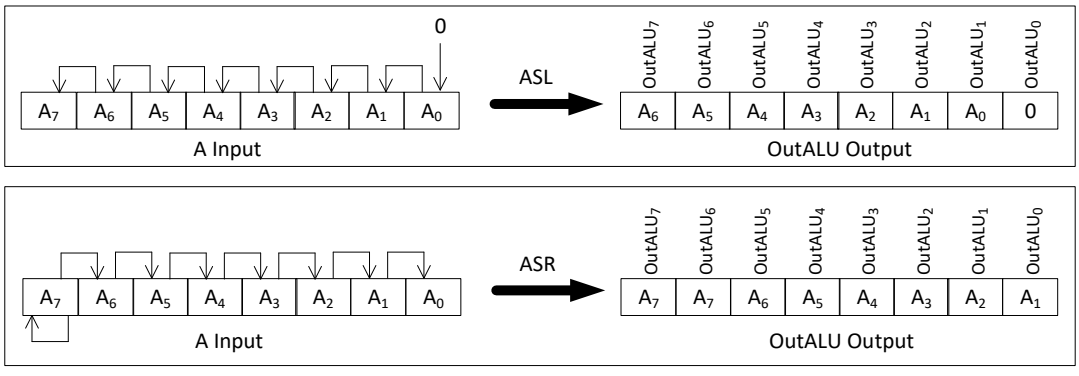
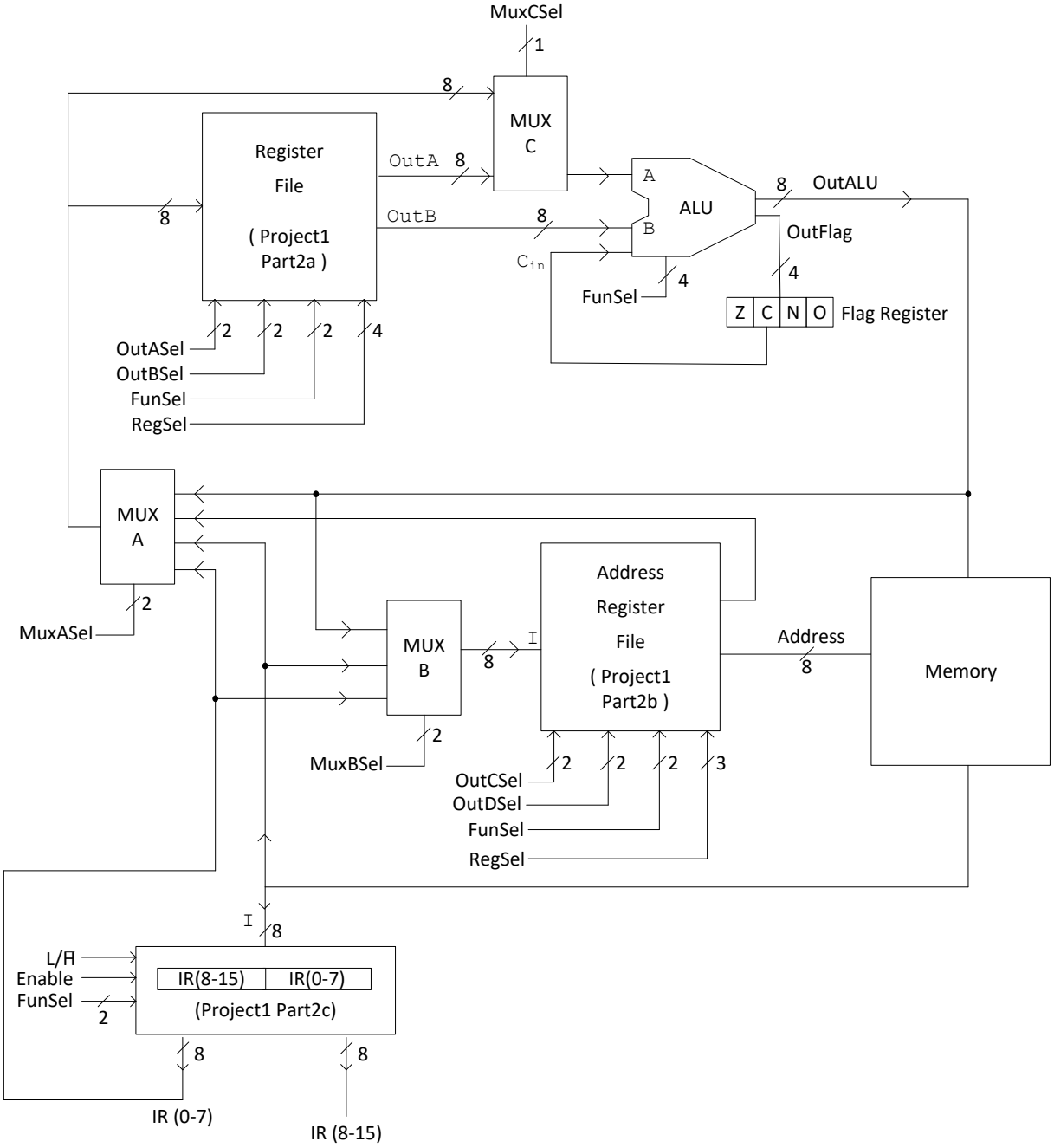


Figure 4: Arithmetic Shift Operations

(Part-2) Implement the organization in Figure 5. Please note that, **the whole system uses the same single clock.**



MuxASel	MuxAOut
00	IROut (0-7)
01	Memory Output
10	Address Register OutC
11	OutALU

MuxBSel	MuxBOut
00	ϕ
01	IROut (0-7)
10	Memory Output
11	OutALU

MuxCSel	MuxCOut
0	MuxAOut
1	OutA

Figure 5: ALU System

Submission:

Implement your design in logisim software, upload a single compressed (zip) file to Ninova before the deadline. **All the students from each group should submit the project file. Therefore, be sure that all of you uploaded the same final file to Ninova.** This compressed file should contain your design files (.circ) and a report that contains:

- the number&names of the students in the group
- list of control inputs and corresponding functions for your design

Group work is expected for this project. All the 4 student members of the group **must** design together. Make sure to connect pins (under Wiring group of logisim) to the inputs and control inputs of your design, so that different inputs and functions can be tested. Similarly connect your inputs and outputs to a “Hex Digit Display" in logisim (under Input/output group of logisim) so that the test outputs can be observed and use proper labelling to improve the clarity of your circuits.