



# **Nemo Project**

## **NemoSim Simulator Tool User Guide**

**Rev. 1.4**  
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## Documentation Control

### History Table

Version	Date	Description
1.0	31 July 2025	Initial release
1.1	7 August 2025	Revised and expanded
1.2	19 August 2025	<ul style="list-style-type: none"><li>● In Section 2.1:<ul style="list-style-type: none"><li>○ Updated and explained the LIF and BIU network XML codes</li><li>○ Added a note about the optional LIF <b>YFlash</b> field</li></ul></li><li>● In Section 2.2, added a note about the optional BIU <b>sup_xml_config_path</b> field</li><li>● In Section 2.4, reformatted the filename syntax</li><li>● In Section 3, added an important note</li></ul>
1.3	18 November 2025	<ul style="list-style-type: none"><li>● In Section 2.1, added optional XML codes for manipulating specific BIU neuron parameters</li><li>● In Table 2-2, added new parameters for configuring the digital-to-spike (DS) converter (bit width, clock, mode)</li><li>● In Section 2.2, added two new configuration file keys (CSV files) for calculating energy (<b>synapses_energy_table_path</b>, <b>neuron_energy_table_path</b>).</li></ul>
1.4	7 January 2026	<ul style="list-style-type: none"><li>● In Table 2-2, added the CPara parameter</li><li>● In Section 2.2, for the BIU network, added the <b>verbosity</b> setting</li><li>● In Section 2.4, updated the definition of the <b>Vin_&lt;x&gt;_&lt;y&gt;.txt</b> file</li></ul>

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# 1. Introduction

## 1.1 Overview

This document describes the NemoSim simulation tool, which is used for spiking neural network architectures, and has been developed as part of the Nemo Project.

It enables researchers and engineers to model, simulate, and analyze the behavior of various neural network types, such as Leaky Integrate-and-Fire (LIF) and Brain-Inspired Unit (BIU) networks.

## 1.2 Purpose

NemoSim is designed to:

- Simulate neural network architectures using user-defined configurations
- Model time-evolving neuron and synapse states in response to input currents
- Support both standard and custom network types (LIF, BIU, and extensible for new models)
- Generate outputs for scientific analysis and visualization, including detailed time-series data for neural state, synapse activity, and spikes
- Facilitate debugging and research, with outputs and tools to identify and analyze network behavior

## 1.3 Key Features

- **Flexible Input:** NemoSim accepts XML-based network descriptions and plain text current input files, supporting both manual and scripted generation.
- **Extensible Design:** The modular codebase allows for easy addition of new neuron/synapse models and architectures.
- **Comprehensive Output:** The tool produces multiple output files (membrane potentials, synaptic inputs, spikes, and so on) for analysis and plotting.
- **Analysis Tools:** NemoSim includes Python scripts and guidelines for visualizing and interpreting simulation results.
- **Robust Error Handling:** The tool detects and reports errors in input files and configuration, aiding reproducibility.

## 1.4 Typical Use Cases

- Computational neuroscience research
- Neuromorphic hardware prototyping and validation
- Algorithm development and prototyping for spiking neural networks

## 2. Using the NemoSim Simulation Tool

To use the NemoSim simulation tool, do the following:

1. Prepare the XML/TXT files, as described in Section 2.1
2. Prepare the JSON file, as described in Section 2.2
3. Run the NemoSim tool, as described in Section 2.3
4. Plot the output, as described in Section 2.4

## 2.1 Step 1: Preparing the XML/TXT Files

Do the following:

1. In an XML configuration file, define your network architecture, neuron parameters, and simulation settings.

- Important:**
- *The XML file must have a <NetworkConfig> root with a type attribute.*
  - *Required child elements depend on the network type (LIF, BIU, and so on).*
  - *All required numeric fields must be present and valid numbers.*

For example:

- For a LIF network:

```
<NetworkConfig type="LIF">
    <LIFNetwork>
        <Cm>1.0</Cm>
        <Cf>0.5</Cf>
        <VDD>2.5</VDD>
        <!-- other LIF parameters -->
    </LIFNetwork>
    <Architecture>
        <Layer size="32"/>
        <YFlash rows="32" cols="32">
            <weights>
                ...
            </weights>
        </YFlash>
        <!-- network connectivity, layers, weights, etc.
-->
    </Architecture>
</NetworkConfig>
```

**Note:** *YFlash* is a matrix of weights, in which each weight holds a value that represents a resistance or diode that will be multiplied by the output of each neuron.

*Each neuron connects to the corresponding row in the YFlash, and each column of the YFlash is connected to the corresponding entrance of each neuron in the next layer.*

Table 2-1 defines the key parameters that are used in this section of the LIF XML configuration file.

These values are based on standard analog neuron circuit modeling practices and can be adapted depending on the simulation context.

**Table 2-1: LIF Network XML Configuration Parameter Definitions**

Parameter	Description	Unit	Example Value	Notes
Cm	Membrane capacitance	Farads (F)	1e-6	Determines the neuron integration time constant
Cf	Feedback capacitance	Farads (F)	1e-9	Affects how quickly the membrane voltage resets or leaks after a spike
VDD	Supply voltage	Volts (V)	5.0	Sets the upper voltage bounds for circuit behavior
VTh	Threshold voltage	Volts (V)	1.0	Defines the spike generation threshold
K	Gain factor	N/A	2	Dimensionless scaling factor (for example, for current mirror)
Rmin/Rmax	Min/Max resistance in synaptic array	Ohms ( $\Omega$ )	145e3/145e6	Used for dynamic range in weight representation
gm	Transconductance	Siemens (S)	6.896e-6	Typically from the input differential pair
CGB*, CGD*, CDB*	Parasitic capacitances (Gate-*, Drain-*, Bulk-*)	Farads (F)	~e-18 values	Derived from transistor model extraction
req	Effective resistance	Ohms ( $\Omega$ )	145e3	Used in equivalent RC modeling

Parameter	Description	Unit	Example Value	Notes
R_da	Driver array resistance	Ohms ( $\Omega$ )	10e3	Series resistance from driver circuitry
dt	Simulation time step	Seconds (s)	0.001	Time increment for each simulation step
IR	Input current scaling factor	Amperes (A)	1e-10	Multiplies the provided input values to obtain actual currents

- For a BIU network:

```
<NetworkConfig type="BIU">
    <BIUNetwork>
        <!-- BIU parameters here -->
    </BIUNetwork>
    <Architecture>
        <Layer size="1">
            <synapses rows="1" cols="1">
                <weights>
                    <row>7.0</row>
                </weights>
            </synapses>
            <NeuronRange start="0" end="2"> // optional
                <VTh>0.5</VTh>
                <RLeak>550e6</RLeak>
                <refractory>10</refractory>
            </NeuronRange>
            <Neuron index="6"> // optional
                <VTh>0.19</VTh>
            </Neuron>
        </Layer>
        <!-- architecture details -->
    </Architecture>
</NetworkConfig>
```

**Note:** The following optional repeated tags are available under each `<Layer>`:

- `<NeuronRange start="S" end="E">` with any of the following parameters: `<VTh>`, `<refractory>`, `<RLeak>`
- `<Neuron index="i">` with any of the following parameters: `<VTh>`, `<refractory>`, `<RLeak>`

Each layer has its own matrix of synapses that connects to the entrance of each neuron in the layer.

Table 2-2 defines the key parameters that are used in this section of the BIU XML configuration file.

These values are based on a switched-capacitor SNN architecture using programmable digital weights, charge sharing, and comparator-based thresholding.

**Table 2-2: BIU Network XML Configuration Parameter Definitions**

Parameter	Description	Unit	Example Value	Notes
Cu	Synapse unit capacitance	Femtofarads (fF)	4	Defines the granularity of weight resolution
Cn	Neuron integration capacitor	Femtofarads (fF)	1000	Large capacitor for temporal integration
VDD	Supply voltage	Volts (V)	1.2	Nominal voltage for digital and analog circuitry
VTh	Comparator threshold voltage	Volts (V)	$\pm 0.4$	Spike generation threshold (programmable)
WS	Weight sign	N/A	+1 or -1	<ul style="list-style-type: none"> <li>● Positive = VDD</li> <li>● Negative = VSS</li> </ul>
W[3:0]	Synaptic weight (4-bit)	Digital	0–15	Multiplies the charge contribution per synapse
Refractory	Refractory period (cycles)	Integer	1–8	Input is blocked for N cycles after spike
Cl	Leakage capacitance (optional)	Femtofarads (fF)	5e-15	Models subthreshold leakage or passive decay
Vm	Neuron potential	Volts (V)	Dynamic	Computed via charge-sharing at each phase
Nu	Number of synaptic inputs	N/A	Varies by layer	Determines the total Cu contribution per neuron
DSBitWidth	Digital-to-spike converter bit width	Integer	4/8	Determines the total Cu contribution per neuron
DSClockMHz	Digital-to-spike converter clock frequency	Integer	10	Determines the total Cu contribution per neuron
DSMode	Activation mode of digital-to-spike converter bit width	String	ThresholdMode   FrequencyMode	Determines the activation mode of the DS
CPara	Parasitic capacitor	Femtofarads (fF)	5.5e-15	Parasitic capacitance

2. In a plain TXT file, define the neuron values.

**Important:** *Each line shall contain values corresponding to the neurons in the first layer (without delimiters), representing the input current for each time step (or input channel).*

For example:

```
1 0 1 0 1 1 1 0
0 0 1 0 1 1 1 0
0 0 1 0 1 1 1 0
0 0 1 0 1 1 1 0
1 0 1 0 1 1 1 0
```

**Tip:** You can use the provided Python **input\_creator.py** script to generate input files; for example:

```
python input_creator.py
> "1e-10 * math.sin(2 * math.pi * t * 5 + 3 *
math.pi/2) + 1e-10"
```

## 2.2 Step 2: Preparing the JSON File

Do the following:

- In a JSON file, define your workspace parameters and input files paths.

For example:

- For a LIF network:

```
{  
    "output_directory":  
        "./Tests/SNN/LIF/sin_current_test/",  
    "xml_config_path":  
        "./Tests/SNN/LIF/sin_current_test/testFull.xml",  
    "data_input_file":  
        "./Tests/SNN/LIF/sin_current_test/input.txt",  
    "progress_interval_seconds": 2  
}
```

- For a BIU network:

```
{  
    "output_directory":  
        "./Tests/SNN/BIU/output_directory",  
    "xml_config_path": "./Tests/SNN/BIU/test.xml",  
    "sup_xml_config_path":  
        "./Tests/SNN/BIU/supervisor.xml",  
    "data_input_file": "./Tests/SNN/BIU/input.txt",  
    "synapses_energy_table_path":  
        "./Tests/SNN/BIU/Spike-in_vs_Not_spike-in.csv",  
    "neuron_energy_table_path":  
        "./Tests/SNN/BIU/Energy_Neuron_CSV_Content.csv",  
    "verbosity":  
        "info/debug",  
    "progress_interval_seconds": 2  
}
```

- Notes:**
- *sup\_xml\_config\_path* is an optional field used only by the BIU network.
  - The following files are read by *parseConfigFromFile* and are copied into **NetworkParameters** (overriding the XML values, if present):
    - *neuron\_energy\_table\_path* is the path to the neuron energy CSV file.
    - *synapses\_energy\_table\_path* is the path to the synapse energy CSV file.
  - **verbosity (Info/Debug)** controls the verbosity of the output files: less for info, more for debug.

## 2.3 Step 3: Running the NemoSim Simulator Tool

Do the following:

- From the root directory, type:

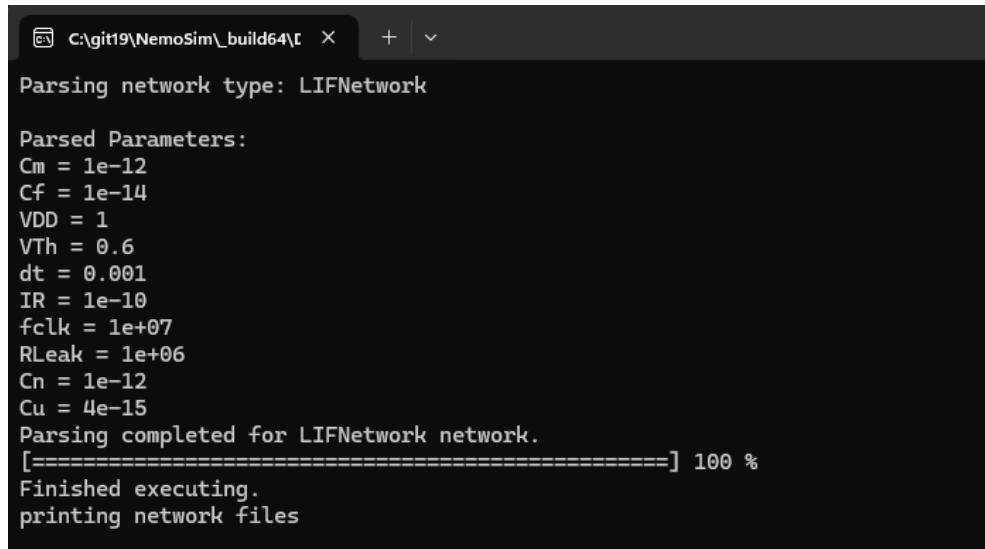
```
NEMOSIM.exe <name of JSON file>
```

For example:

```
NEMOSIM.exe config.json
```

While the NemoSim is running, it will display progress messages on the screen, as demonstrated in Example 2-1. If an error occurs, an error or warning message will be displayed (for details, see Section 3).

*Example 2-1: NemoSim Progress Messages*



The screenshot shows a terminal window with the following output:

```
C:\git19\NemoSim\_build64\l Parsing network type: LIFNetwork  
Parsed Parameters:  
Cm = 1e-12  
Cf = 1e-14  
VDD = 1  
VTh = 0.6  
dt = 0.001  
IR = 1e-10  
fclk = 1e+07  
RLeak = 1e+06  
Cn = 1e-12  
Cu = 4e-15  
Parsing completed for LIFNetwork network.  
[=====] 100 %  
Finished executing.  
printing network files
```

## 2.4 Step 4: Plotting the Outputs

When the NemoSim has finished running, it generates output files and places them in the output directory you specified in the JSON file (as described in Section 2.2).

Output files are plain text, each containing a list of numeric values (one per line). Each output file corresponds to a specific neural variable, where <x> is the number of the layer, and <y> is the number of the neuron:

- LIF Simulation (three files per neuron):
  - **Iins\_<x>\_<y>.txt**: Input currents
  - **Vms\_<x>\_<y>.txt**: Membrane potentials
  - **Vouts\_<x>\_<y>.txt**: Output voltages (spikes)
- BIU Simulation (three files per neuron):
  - **Vin\_<x>\_<y>.txt**: Neuron input values (the output of the synapses that go into the neuron)
  - **Vns\_<x>\_<y>.txt**: Neural state potentials
  - **Spikes\_<x>\_<y>.txt**: Output spikes

After the output files have been generated, you can plot or analyze them to look for neurons with unexpected behaviors (for example, constant potentials or no spikes) for further debugging.

Do one of the following:

- For LIF networks, use the **plot\_vm\_to\_dt.py** script.
- For BIU networks, use the **plot\_vn\_to\_dt.py** script.

For example:

```
python plot_vm_to_dt.py Iins_0_0.txt vms_0_0.txt  
Vouts_0_0.txt
```



## 3. Error Handling

**Important:** All errors are considered to be critical, and will stop the NemoSim Simulator.

### 3.1 Error Message Formats

- Errors (examples):

```
Error loading XML file: <description>
Error: No <NetworkConfig> root element found.
Error: Network type attribute not found in
<NetworkConfig>.
```

### 3.2 Possible Return Codes

The code uses TinyXML2, which defines error codes such as:

- XML\_SUCCESS (0): Success
- XML\_NO\_ATTRIBUTE
- XML\_WRONG\_ATTRIBUTE\_TYPE
- XML\_ERROR\_FILE\_NOT\_FOUND
- XML\_ERROR\_FILE\_COULD\_NOT\_BE\_OPENED
- XML\_ERROR\_FILE\_READ\_ERROR
- XML\_ERROR\_PARSING\_ELEMENT

For the full list, see TinyXML2's **XMLError** enum.



## 4. References

- For details and example files for LIF, see **Tests/SNN/LIF/**.
- For details and example files for BIU, see **Tests/SNN/BIU/**.
- Output file examples: **Vin.txt**, **Vns.txt** (in the test folders).