*Εργασία bonus*

library IEEE;  
use IEEE.STD\_LOGIC\_1164.ALL;  
  
  
entity function\_reg is  
    Port ( clk  : in STD\_LOGIC;  
            x: in std\_logic;  
            y: in std\_logic;  
            z : in std\_logic;  
           reset : in STD\_LOGIC;  
           f : out STD\_LOGIC);  
end function\_reg;  
  
architecture Behavioral of function\_reg is  
  
begin  
       process (clk,reset)  
            begin  
                  if reset > '1' then  
                     f<='0' ;  
                  elsif rising\_edge(clk) then  
                   f<= (x and y and z) or (x and y and not z )or ( not x and not y and not z);  
                  end if ;  
         end process ;    
  
end Behavioral;

--testbench

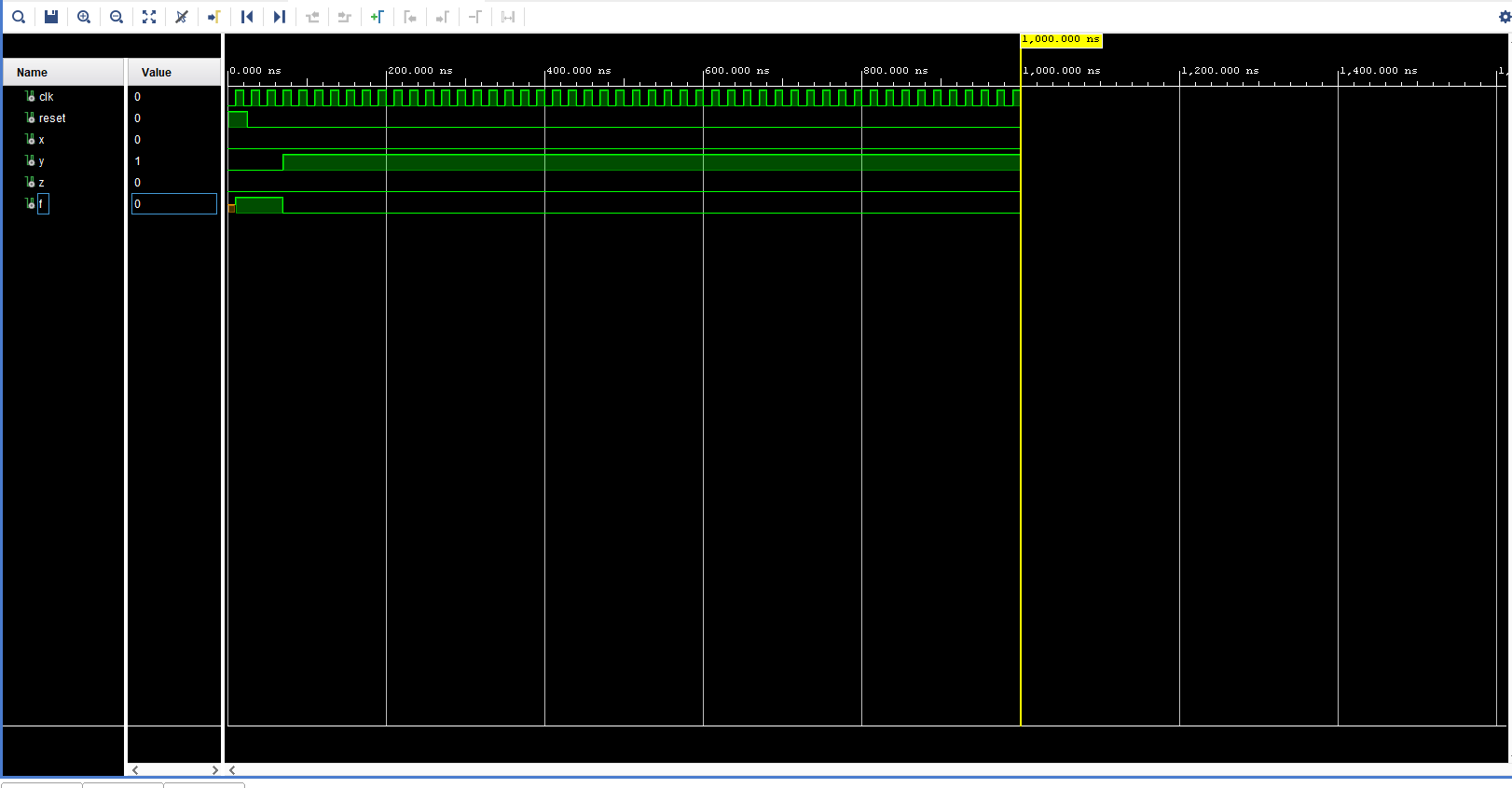
library IEEE;  
use IEEE.STD\_LOGIC\_1164.ALL;  
  
  
entity tb\_function\_reg is  
     
end tb\_function\_reg;  
  
architecture Behavioral of tb\_function\_reg is  
    signal clk ,reset ,x,y,z :std\_logic := '0' ;  
    signal f : std\_logic;  
     
    component function\_reg  
        port (clk  : in STD\_LOGIC;  
            x: in std\_logic;  
            y: in std\_logic;  
            z : in std\_logic;  
           reset : in STD\_LOGIC;  
           f : out STD\_LOGIC);  
     end component;

 begin  
 uut: function\_reg  
    port map (  
    clk => clk,  
    x => x ,  
    y => y ,  
    z => z ,  
    reset => reset ,  
    f => f  
    );  
  
    clk\_porcess: process  
     begin  
           clk<='0';  
           wait for 10 ns;  
           clk<='1';  
           wait for 10 ns;  
     end process;

     stim\_proc: process  
     begin  
        reset <='1';  
        wait for 25 ns;  
        reset <='0';  
        wait for 25 ns;  
         
        x<='0'; y<='0'; x<='0';  
        wait for 20 ns ;  
        x<='0'; y<= '0'; z<='1';  
        x<='0'; y<='1'; z<= '0';  
        wait for 20 ns;

      wait ;

      end process;  
end Behavioral;



ΚΑΡΑΒΙΑ ΜΑΡΙΑ ΣΠΥΡΙΔΟΥΛΑ (ΑΜ:2026202100049)