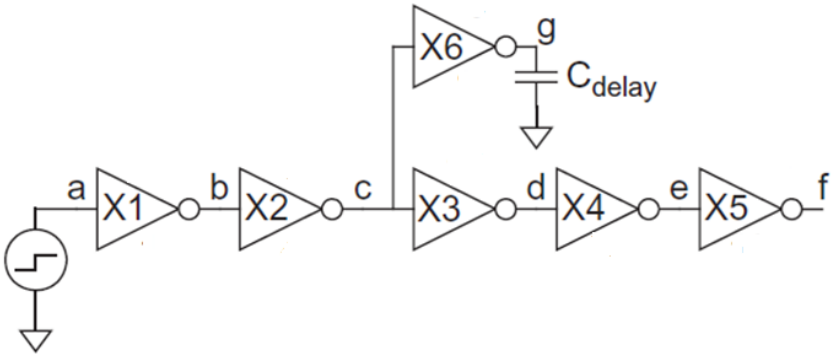
Posted: 11/19/2024 Design Project (ECE 4130/5130) (Timely completion Demonstration is Required)

Due: 12/05/2024

Objectives:

1. To learn the Cadence design environment to perform Transient analysis of schematic of inverter
2. To learn the Cadence design environment to perform Transient analysis of schematic of 2-input NAND gate
3. To perform Transient analysis and comparison between the designs of 2 input NAND and NOR gates
4. Measure the input capacitance of inverter and in the process find out capacitance per unit transistor (5λ/2λ)
5. To obtain the **best circuit choice** in terms of delay by utilizing theory of logical effort



Tasks

Related to Objective 1:

1. Replicate all the tasks performed in the first video (related to Inverter's schematic only).

Related to Objective 2:

2. Replicate the tasks performed in the third video – related to the NAND gate's schematic.

Related to Objective 3:

3. This task is related to NAND gate: Use paper pencil analysis to find out which set of input conditions will lead to propagation delay and which set of input conditions will lead to contamination delay. Next in Vitruoso - include 100fF (simply replace the 1fF with 100fF) capacitor at the output of the NAND gate designed earlier. Perform the transient analysis. Verify using simulations that indeed your paper-pencil analysis is in line with the simulation results (Note. your paper analysis will only give you the trend – the actual values will be off).
4. Do a paper analysis of the required input transitions for propagation delay and contamination delay for 2 input NOR gate. Next implement a 2 input NOR gate, include 100 fF at the output of the NOR gate symbol (as shown in tutorial for NAND gate)- following the techniques you learned in the video tutorials. For 2-input NOR: PMOS size = 12um and NMOS size = 3um – Verify using simulations that indeed your paper-pencil analysis is in line with the simulation results (Note. your paper analysis will only give you the trend – the actual values will be off).
5. Compare the simulation results you obtained for NAND and NOR gates

Related to Objective 4:

6. Using the unit inverter found earlier (by me) using simulation and unit inverter's capacitance-

PMOS= 2.1 micrometer, and NMOS=1.5 micrometer (i.e. PMOS size is: **W/L= 7λ /2λ** and NMOS size is: W/L = 5λ/2λ) (notice that NMOS's W is not 4λ)- find out the input capacitance of X4 inverter using the method taught in the class – this method is also explained on page 308 of your text book – after finding the capacitance of X4 find out the input capacitance of unit inverter (size PMOS:1.4 and NMOS: 1)- Notice that in the following Figure I want you to size X1 = 1 unit inverter, and X2 as 4 unit inverters, and similarly sizes of X3, X4, X5 and X6 are 8, 32, and 128 unit inverters, respectively as shown in the Figure 1.

Notes:

a. Since the new unit inverter has an input capacitance and output capacitance of 2.4 units, so now we need to normalize the values using this new input capacitance value of inverter. (**Hint:** 2input Nand gate has a g =3.4/2.4 and p= 4.8/2.4 =2)
b. For Cdelay – sweep the values between 50f F to 900f F – and then narrow it down to the right value
c. To find out the C for unit inverter you'll need to divide the obtained Cdelay with 32.
d. Try to find out the value for C per micron – this value should be similar to the value given in slide 11 of slide set Chapter4_1….**Hint** unit inverter capacitance will be close to 6 fF.
~~e. Use the value of tau as 60 psec for paper pencil calculations for these tasks.~~

7. Related to Objective 5:

Compound Gate:

a. For each group I will be assigning a unique combination of compound gate's logic equation and H (possible examples are shown towards the end of this document). Show the paper pencil analysis for initial sizing of the compound gate (worst case analysis to obtain each path equal to unit simulated inverter's resistance).
b. Draw its schematic
c. Obtain the g values and p for this compound gate.
d. Obtain the initial estimate on number of stages- mention your design choices (i.e. possible number of stages that you are going to use)
e. Find out the delays for all the chosen cases using paper pencil analysis.
f. Size the transistors (show each NMOS and PMOS's sizing)
g. Make a comparison between your paper pencil analysis and (average case) simulated results, in terms of propagation delay. Discuss on the differences in the result –the trend should be the same.

Non-Compound Gates: Explore other possible circuit options to derive the same load with same logic but without using compound gates:

h. Show the steps you took in order to reach the design choices (I am expecting you to come up with some sort of calculation for number of stages).
i. Show the calculation **for at least two options** .
j. Confirm your delay values against simulation.

Deliverables (Tabulate your data where you feel it is necessary):

Tasks 1 and 2) Please bring your laptop in the class on 11/26/2024 and show me the simulations of schematic of inverter and NAND gate.

Task 3) A pdf file **having a separate section for each of the subsequent tasks** and provide following:

a. Show your paper-pencil analysis of NAND gate

b. Show two waveforms – one for propagation delay and other for contamination delay – verify whether they are in line (i.e. having the same trend) as your paper-pencil analysis or not.

Task 4) In the SAME pdf file make a different section and provide following:

a. Show your paper-pencil analysis of NOR gate
b. Show two waveforms – one for propagation delay and other for contamination delay – verify whether they are in line (i.e. having the same trend) as your paper-pencil analysis or not.

Task 5) Make a table to illustrate the difference between the values obtained ~~in Tasks 2 and 3 and discuss your results~~ NAND and NOR gates

Task 6) ~~Report the modified values of gs and ps of the 2 and 3 input NAND and NOR gates~~ (good presentation will lead to better grades). Show your simulation waveform (from the EDA tool)– show your simulated circuit (transistor level) with width of the MOSFETs visible (from the EDA tool)- report the capacitance value of X4, unit inverter, unit transistor and capacitance per micron.

Task 7) Provide a report on parts a, b, c, d, e, f, g, h, i, j