Design Project

ECE 5130 (Intro to Digital VLSI)

Fall 2024

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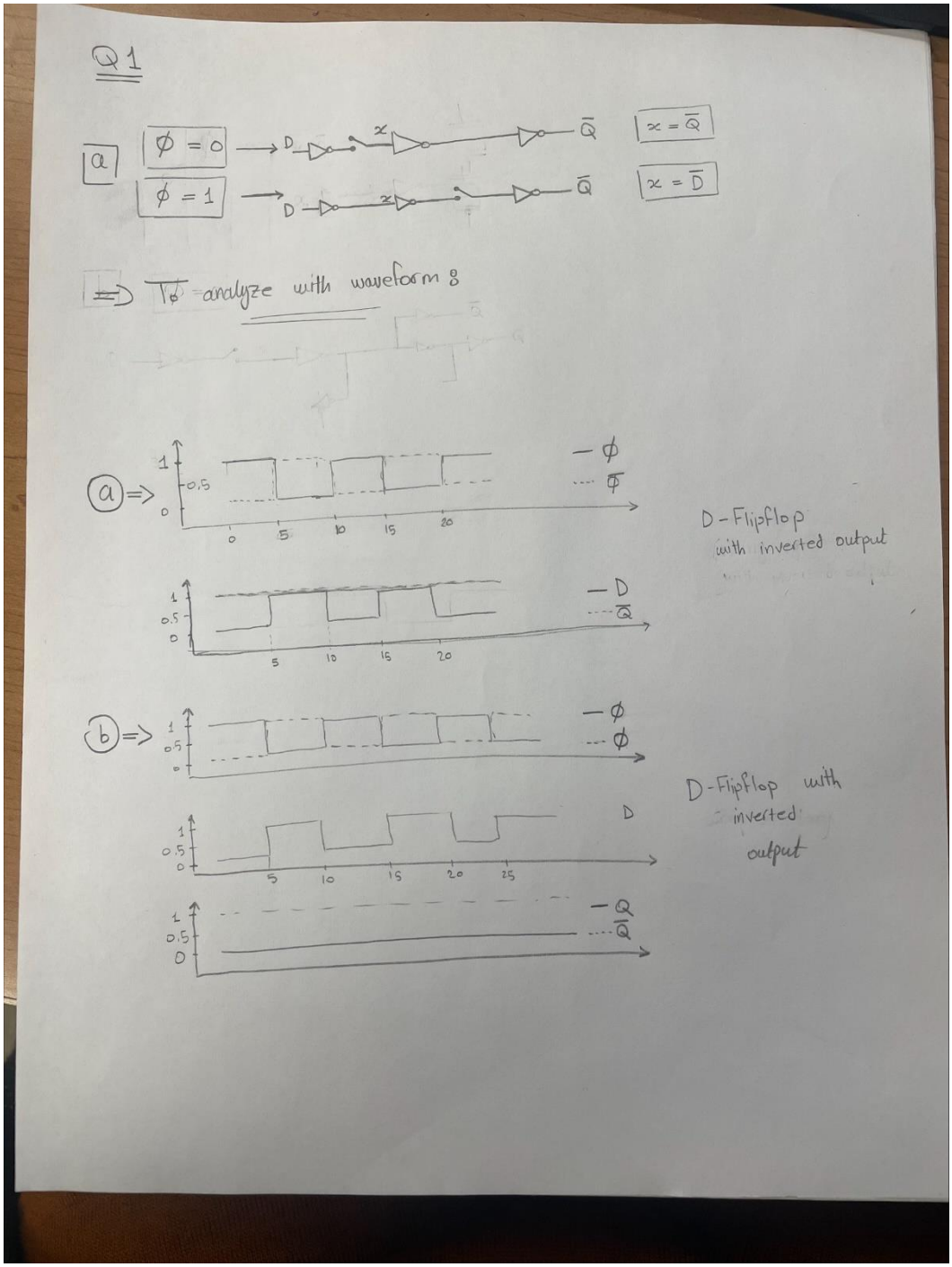
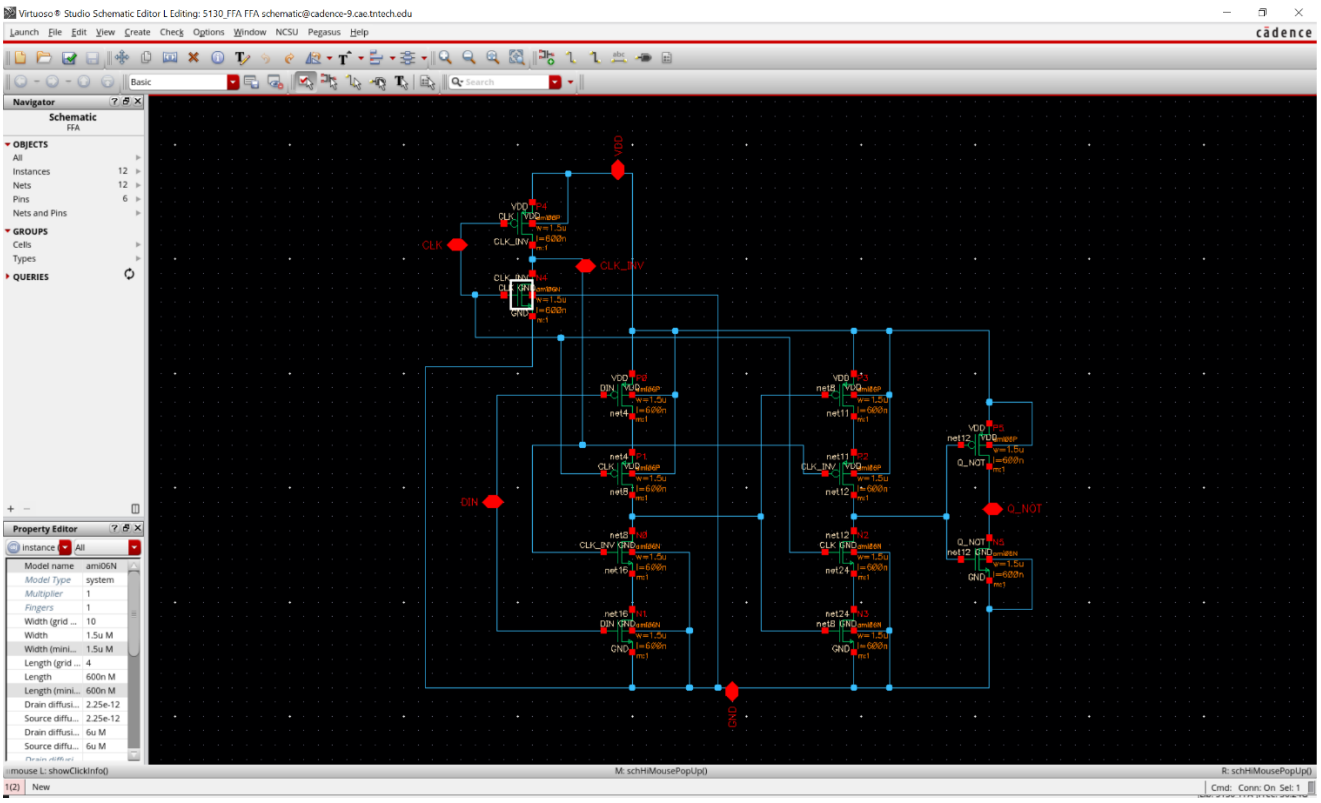
QUESTION 1

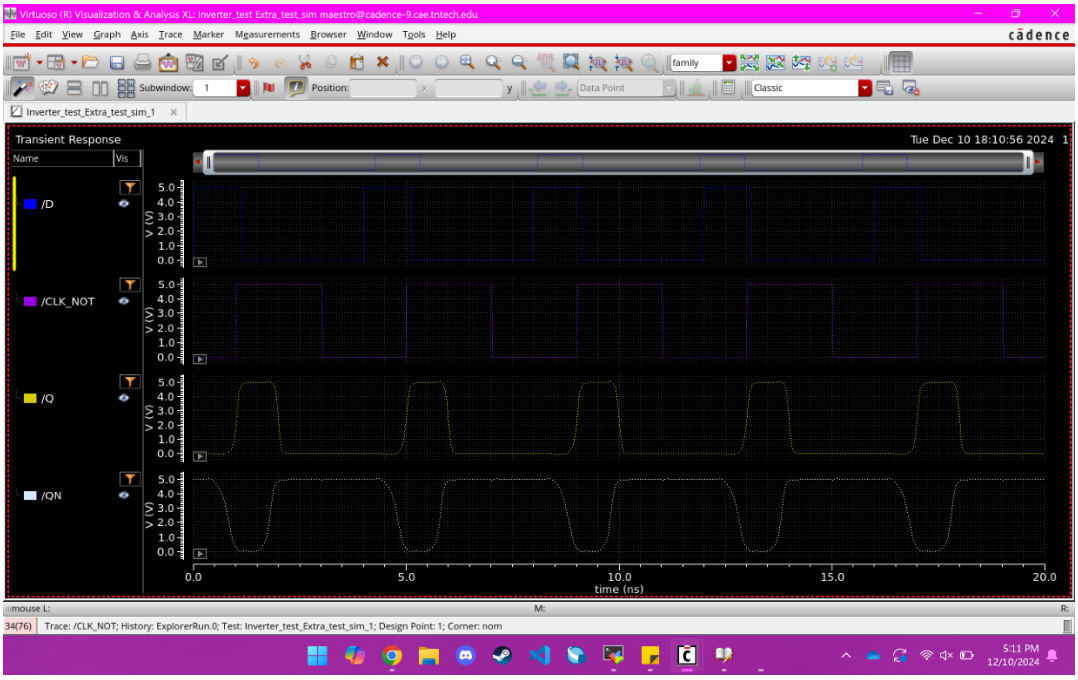

Q1
a
ϕ = 0
D
x
Q̄
x = Q̄
ϕ = 1
D
x
Q̄
x = D
analyze with waveform
a
1
0,5
0
0
5
10
15
20
ϕ
ϕ̄
D - Flipflop with inverted output
1
0,5
0
5
10
15
20
D
Q̄
b
1
0,5
0
ϕ
ϕ
1
0,5
0
5
10
15
20
25
D
1
0,5
0
Q
Q̄
D-Flipflop with inverted output

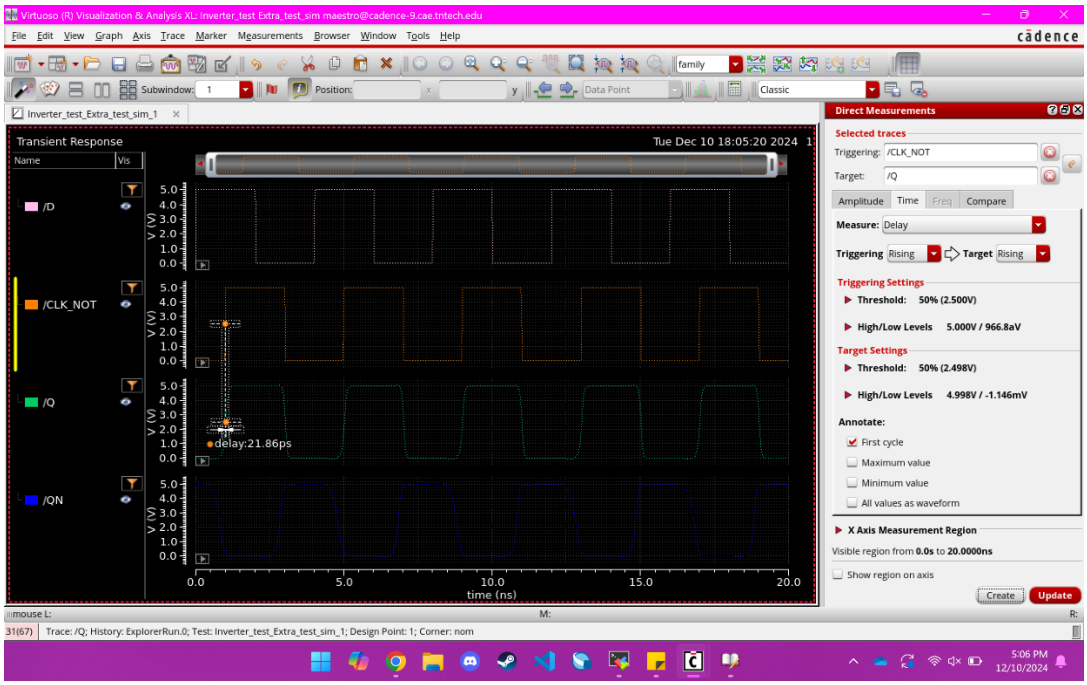
QUESTION 2

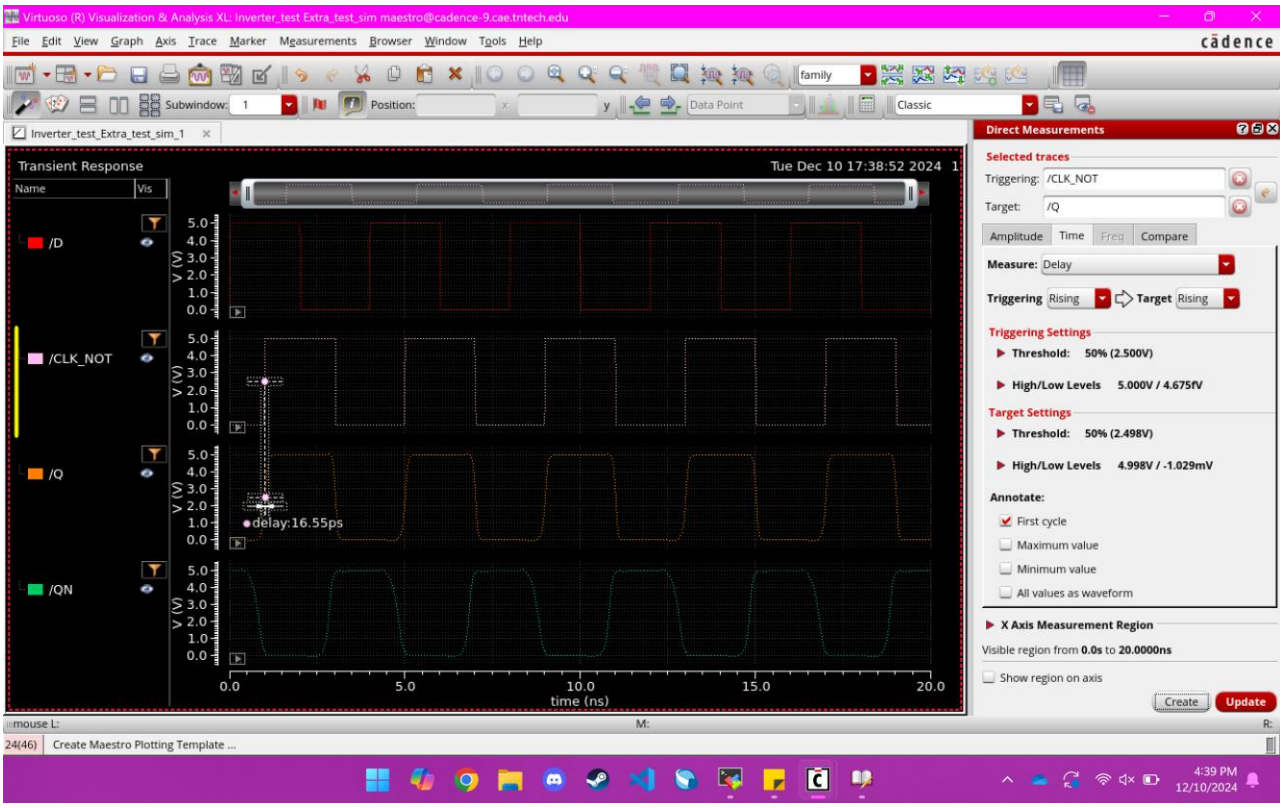

Virtuoso® Studio Schematic Editor L Editing: 5130_FFA FFA schematic@cadence-9.cae.tntech.edu
Launch File Edit View Create Check Options Window NCSU Pegasus Help
cadence
Navigator
Schematic
FFA
OBJECTS
All
Instances 12
Nets 12
Pins 6
Nets and Pins
GROUPS
Cells
Types
QUERIES
Property Editor
Instance All
Model name ami06N
Model Type system
Multiplier 1
Fingers 1
Width (grid ... 10
Width 1.5u M
Width (mini... 1.5u M
Length (grid ... 4
Length 600n M
Length (mini... 600n M
Drain diffusi... 2.25e-12
Source diffu... 2.25e-12
Drain diffusi... 6u M
Source diffu... 6u M
VDD
CLK
CLK_INV
DIN
Q_NOT
GND
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()
New
Cmd: Conn: On Sel: 1

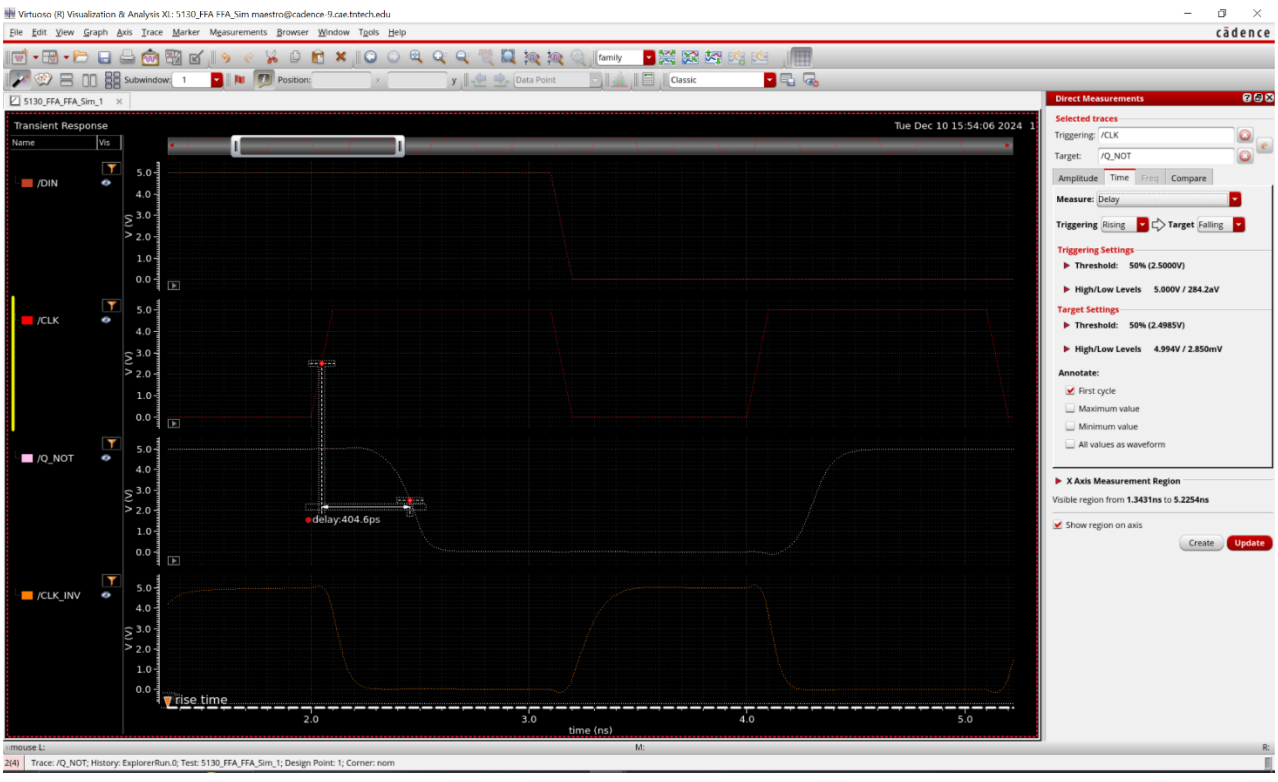
QUESTION 3

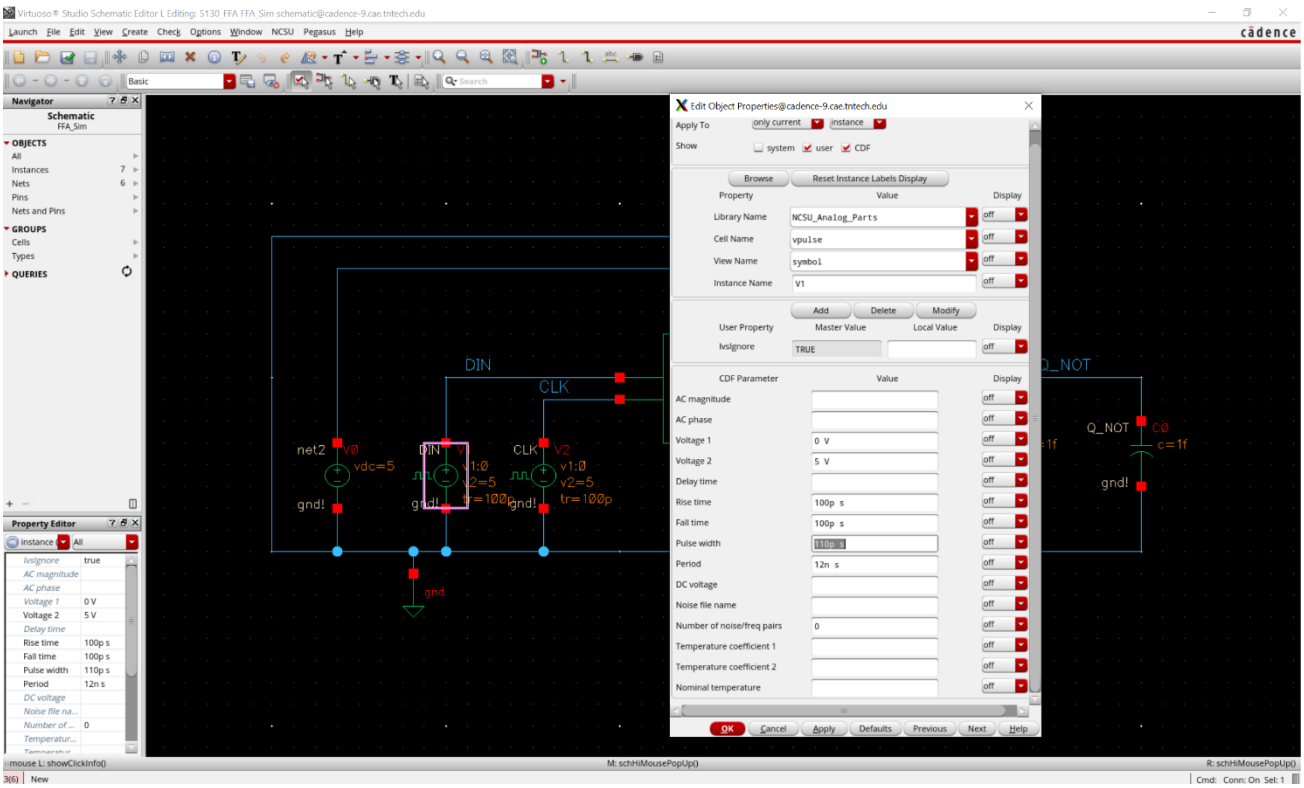
We measured the hold time by decreasing the hold time until the clock to Q delay was 1.5 times the normal value of C2Q.png. I measured the setup time by slowly decreasing the setup time until the Clock to Q delay was 1.5 times the normal C2Q.png time. The hold time was 110p S and the setup time was 200p S.

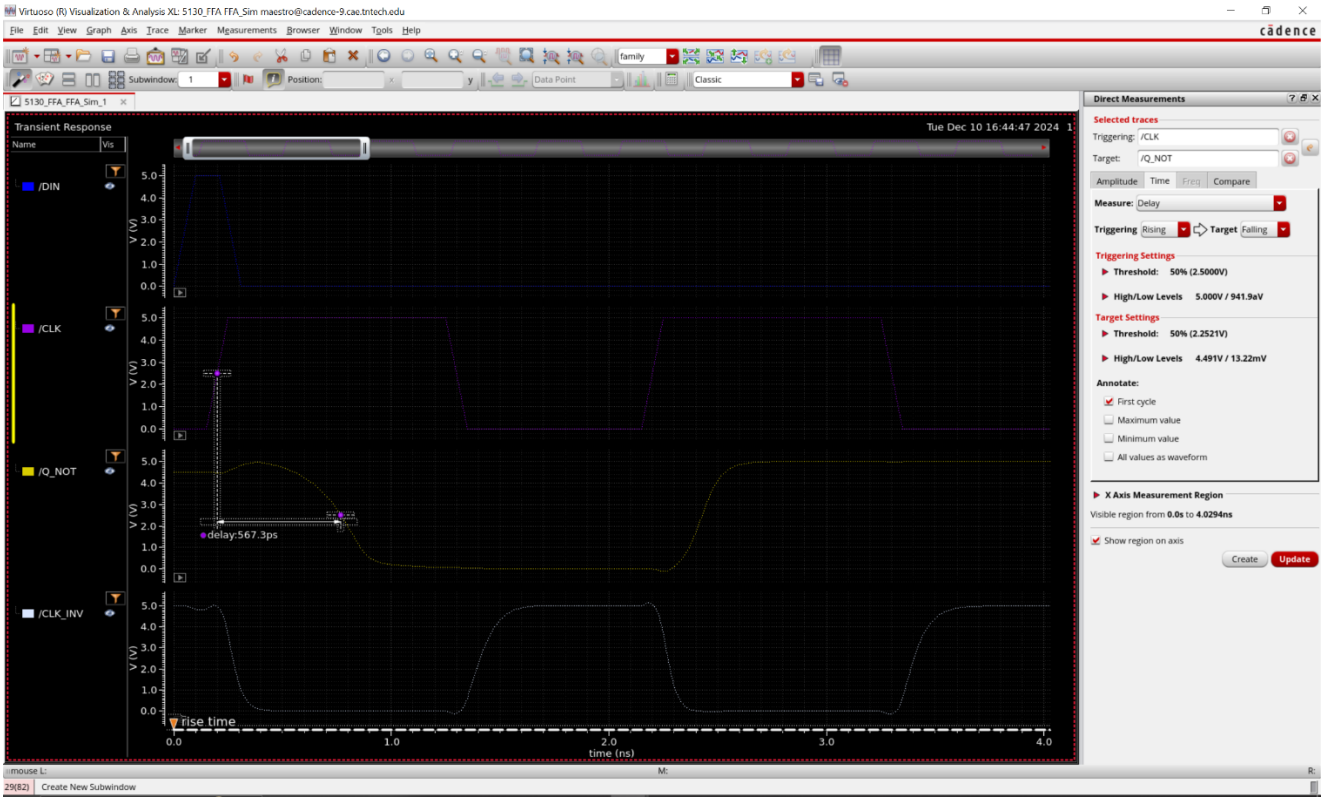


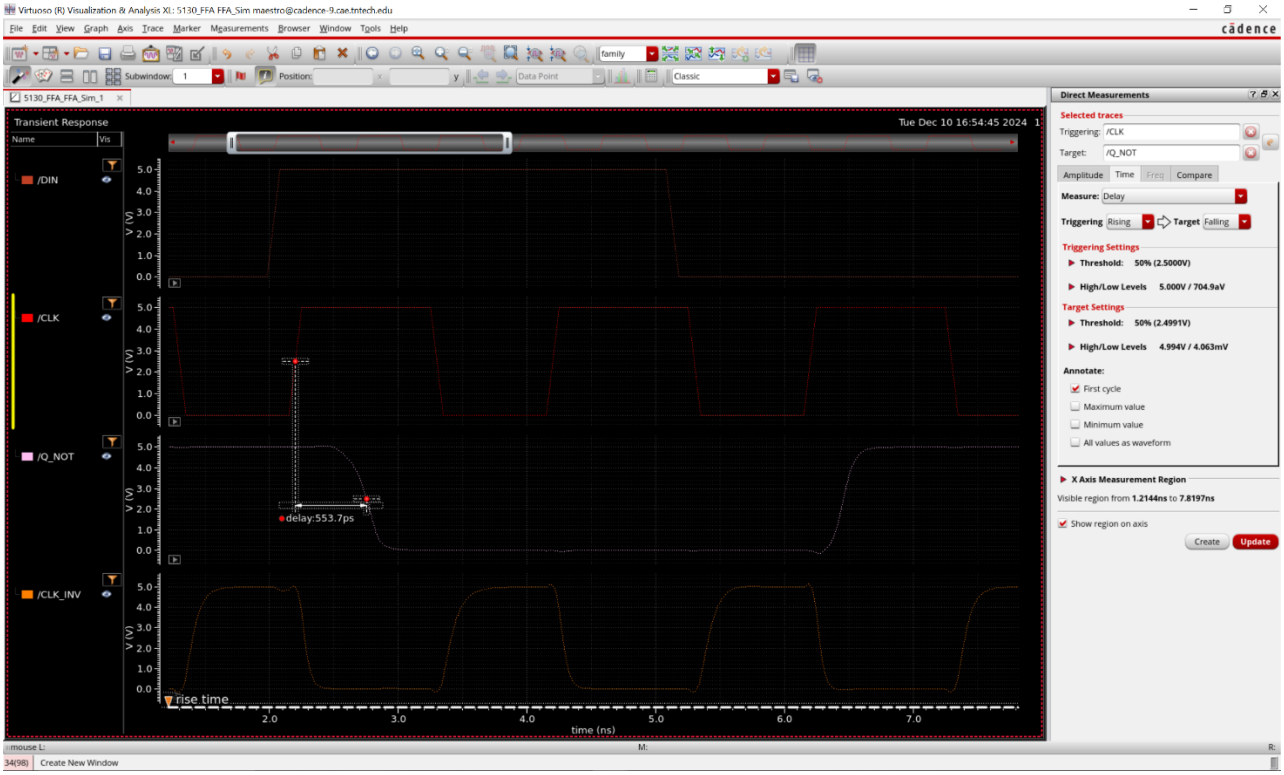


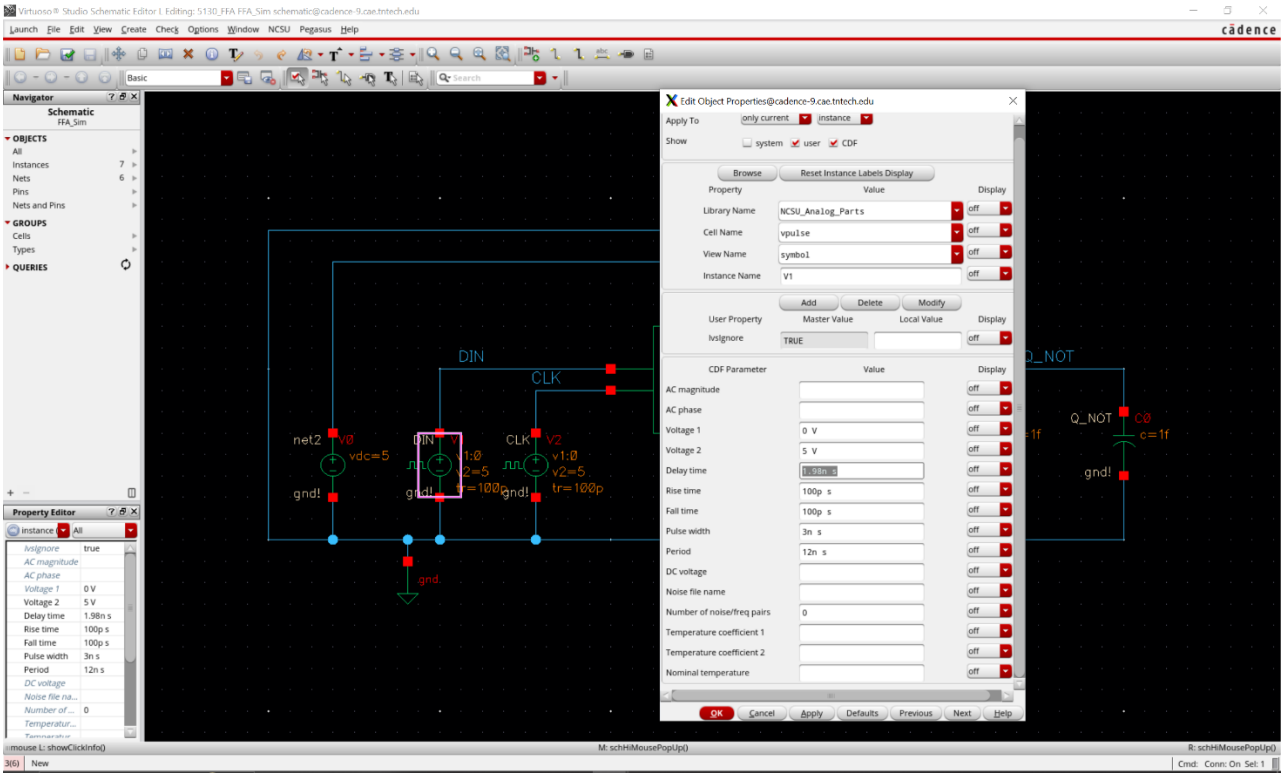

Virtuoso (R) Visualization & Analysis XL: Inverter_test Extra_test_sim maestro@cadence-9.cae.tntech.edu
File Edit View Graph Axis Trace Marker Measurements Browser Window Tools Help
cadence
Inverter_test_Extra_test_sim_1
Transient Response
Tue Dec 10 17:38:52 2024
/D
/CLK_NOT
/Q
/QN
delay:16.55ps
time (ns)
Direct Measurements
Selected traces
Triggering: /CLK_NOT
Target: /Q
Amplitude Time Freq Compare
Measure: Delay
Triggering Rising Target Rising
Triggering Settings
Threshold: 50% (2.500V)
High/Low Levels 5.000V / 4.675fV
Target Settings
Threshold: 50% (2.498V)
High/Low Levels 4.998V / -1.029mV
Annotate:
First cycle
Maximum value
Minimum value
All values as waveform
X Axis Measurement Region
Visible region from 0.0s to 20.0000ns
Show region on axis
Create
Update
Create Maestro Plotting Template ...
4:39 PM
12/10/2024


Virtuoso (R) Visualization & Analysis XL: 5130_FFA FFA_Sim maestro@cadence-9.cae.tntech.edu
cadence
5130_FFA_FFA_Sim_1
Transient Response
Tue Dec 10 15:54:06 2024
/DIN
/CLK
/Q_NOT
/CLK_INV
delay:404.6ps
rise time
time (ns)
Direct Measurements
Selected traces
Triggering: /CLK
Target: /Q_NOT
Measure: Delay
Triggering Rising Target Falling
Triggering Settings
Threshold: 50% (2.5000V)
High/Low Levels 5.000V / 284.2aV
Target Settings
Threshold: 50% (2.4985V)
High/Low Levels 4.994V / 2.850mV
Annotate:
First cycle
Maximum value
Minimum value
All values as waveform
X Axis Measurement Region
Visible region from 1.3431ns to 5.2254ns
Show region on axis
Create
Update


Edit Object Properties@cadence-9.cae.tntech.edu
Library Name
NCSU_Analog_Parts
Cell Name
vpulse
View Name
symbol
Instance Name
V1
Pulse width
110p s
Period
12n s
DIN
CLK
Q_NOT
net2
gnd!


Transient Response
Tue Dec 10 16:44:47 2024
/DIN
/CLK
/Q_NOT
/CLK_INV
delay:567.3ps
rise time
time (ns)
Direct Measurements
Selected traces
Triggering: /CLK
Target: /Q_NOT
Measure: Delay
Triggering Settings
Threshold: 50% (2.5000V)
High/Low Levels 5.000V / 941.9aV
Target Settings
Threshold: 50% (2.2521V)
High/Low Levels 4.491V / 13.22mV
Annotate:
First cycle
Maximum value
Minimum value
All values as waveform
X Axis Measurement Region
Visible region from 0.0s to 4.0294ns
Show region on axis
Create
Update


Transient Response
Tue Dec 10 16:54:45 2024
/DIN
/CLK
/Q_NOT
/CLK_INV
delay:553.7ps
rise time
time (ns)
Direct Measurements
Selected traces
Triggering: /CLK
Target: /Q_NOT
Amplitude
Time
Freq
Compare
Measure: Delay
Triggering Rising
Target Falling
Triggering Settings
Threshold: 50% (2.5000V)
High/Low Levels 5.000V / 704.9aV
Target Settings
Threshold: 50% (2.4991V)
High/Low Levels 4.994V / 4.063mV
Annotate:
First cycle
Maximum value
Minimum value
All values as waveform
X Axis Measurement Region
Visible region from 1.2144ns to 7.8197ns
Show region on axis
Create
Update


Navigator
Schematic
FFA_Sim
OBJECTS
GROUPS
QUERIES
Property Editor
Edit Object Properties@cadence-9.cae.tntech.edu
Library Name NCSU_Analog_Parts
Cell Name vpulse
View Name symbol
Instance Name V1
Delay time 1.98n s
Rise time 100p s
Fall time 100p s
Pulse width 3n s
Period 12n s
DIN
CLK
Q_NOT
net2
gnd!
gnd

QUESTION 4

For question 4, the circuit will fail when the delay for the inverted clock is significantly higher than the clock signal coming in to the circuit. If the NMOS transistors for the inverted clock are 225 um instead of 1.5 um, it will cause the inverted clock to be significantly delayed. This will cause the circuit to malfunction.