Design Project

ECE 5130 (Intro to Digital VLSI)

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OBJECTIVE 3

Comparison between the designs of 2 input NAND and NOR gates

In the following paper-pencil analysis, we investigated the input conditions that would result in propagation delay and contamination delay for both a 2-input NAND gate and a 2-input NOR gate. It is noticeable that the transitions of interest are from 11 to 10 as the worst delay and from – to 00 as the best delay value, while the transition for 11 will be in-between.

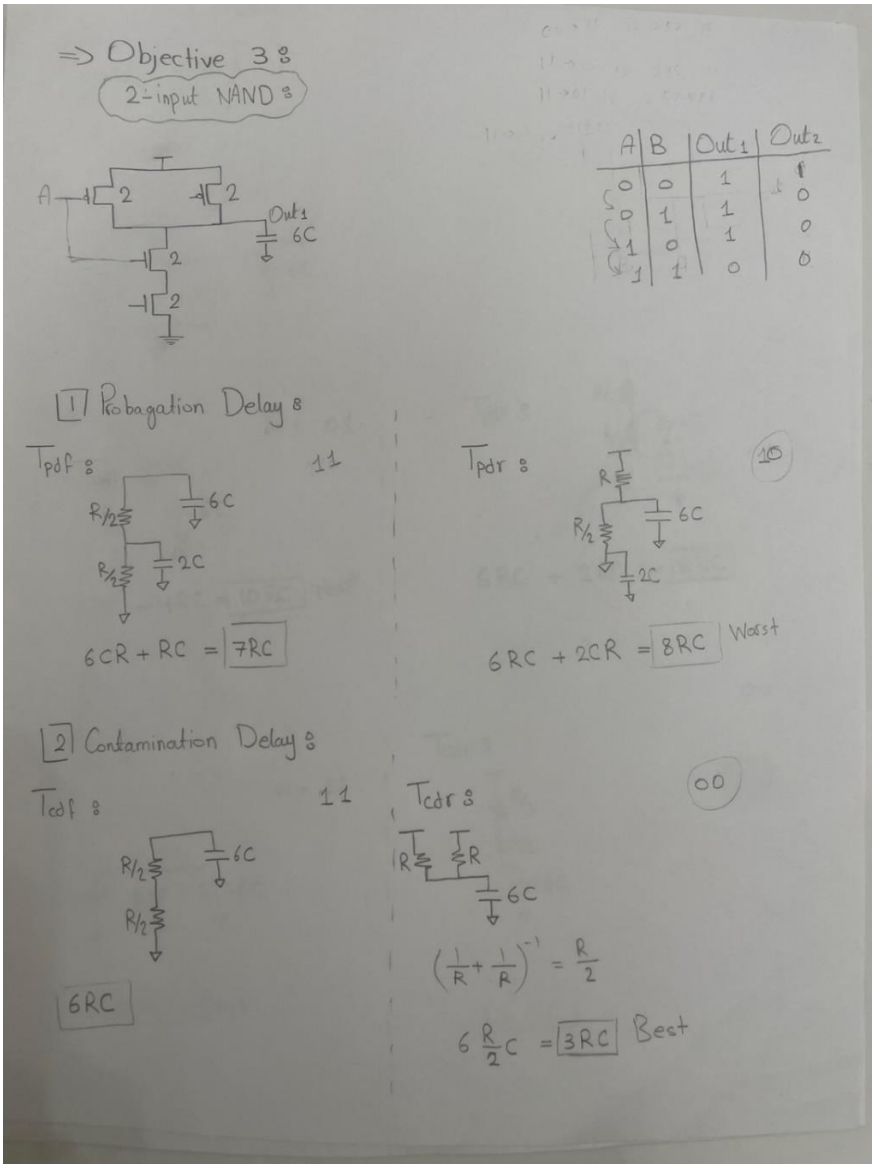

Figure 1: Paper-pencil Calculations for NAND Gate

For the NAND gate, we identified the specific input transitions that lead to propagation and contamination delays. Subsequently, in the Virtuoso tool, we implemented a 100 fF capacitor (replacing the 1 fF capacitor from the original design) at the output of the NAND gate. We then performed simulations to verify whether the results from the paper-pencil analysis align with the simulation outcomes, as shown in the following pictures.

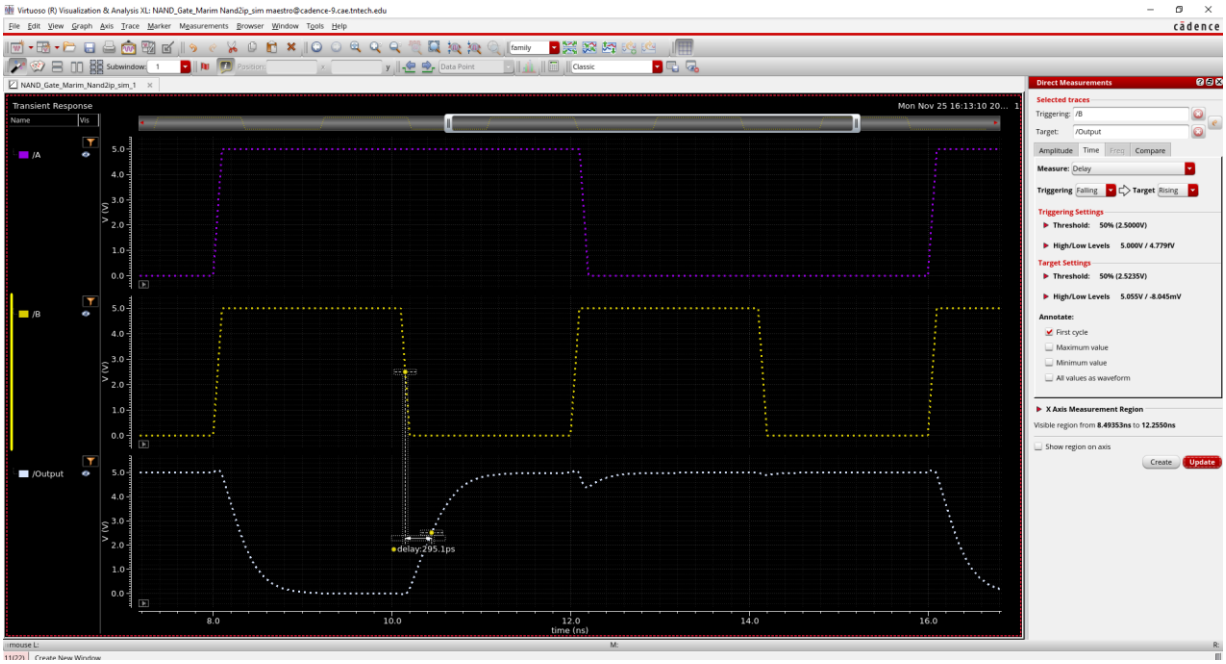

Figure 2: Propagation Delay for 2 Input NAND Gate

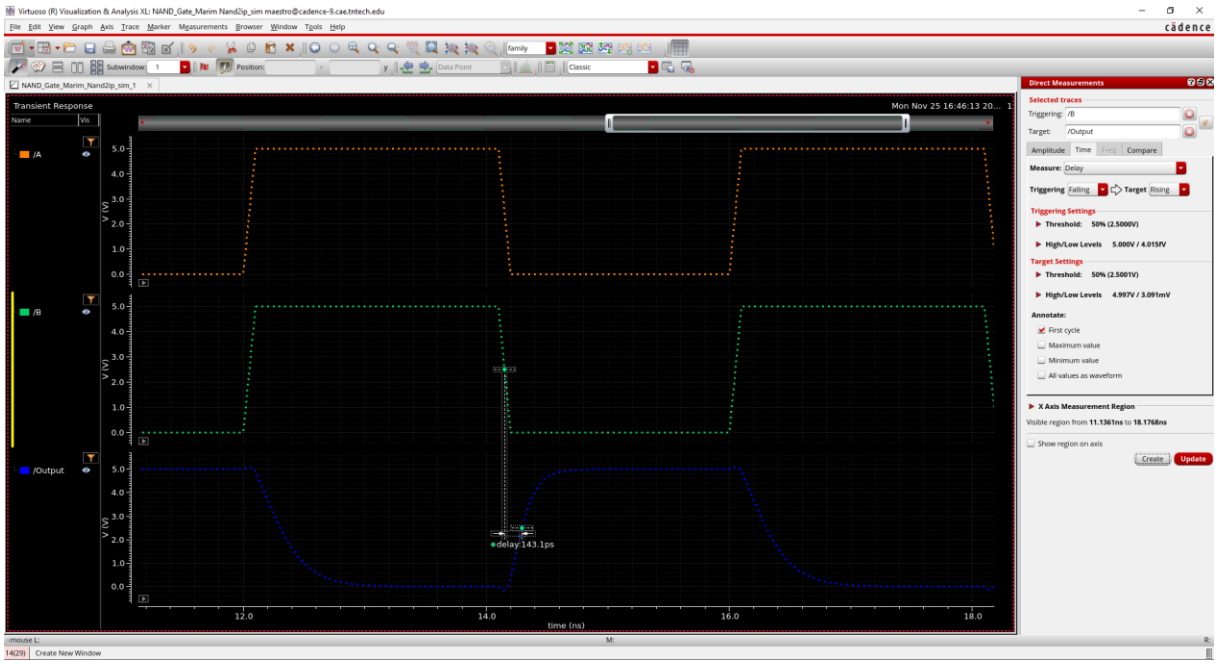

Figure 3: Contamination Delay for 2 Input NAND Gate

Similarly, for the 2-input NOR gate, we performed a similar paper-pencil analysis, shown in the following picture, to determine the required input transitions for both propagation and contamination delays.

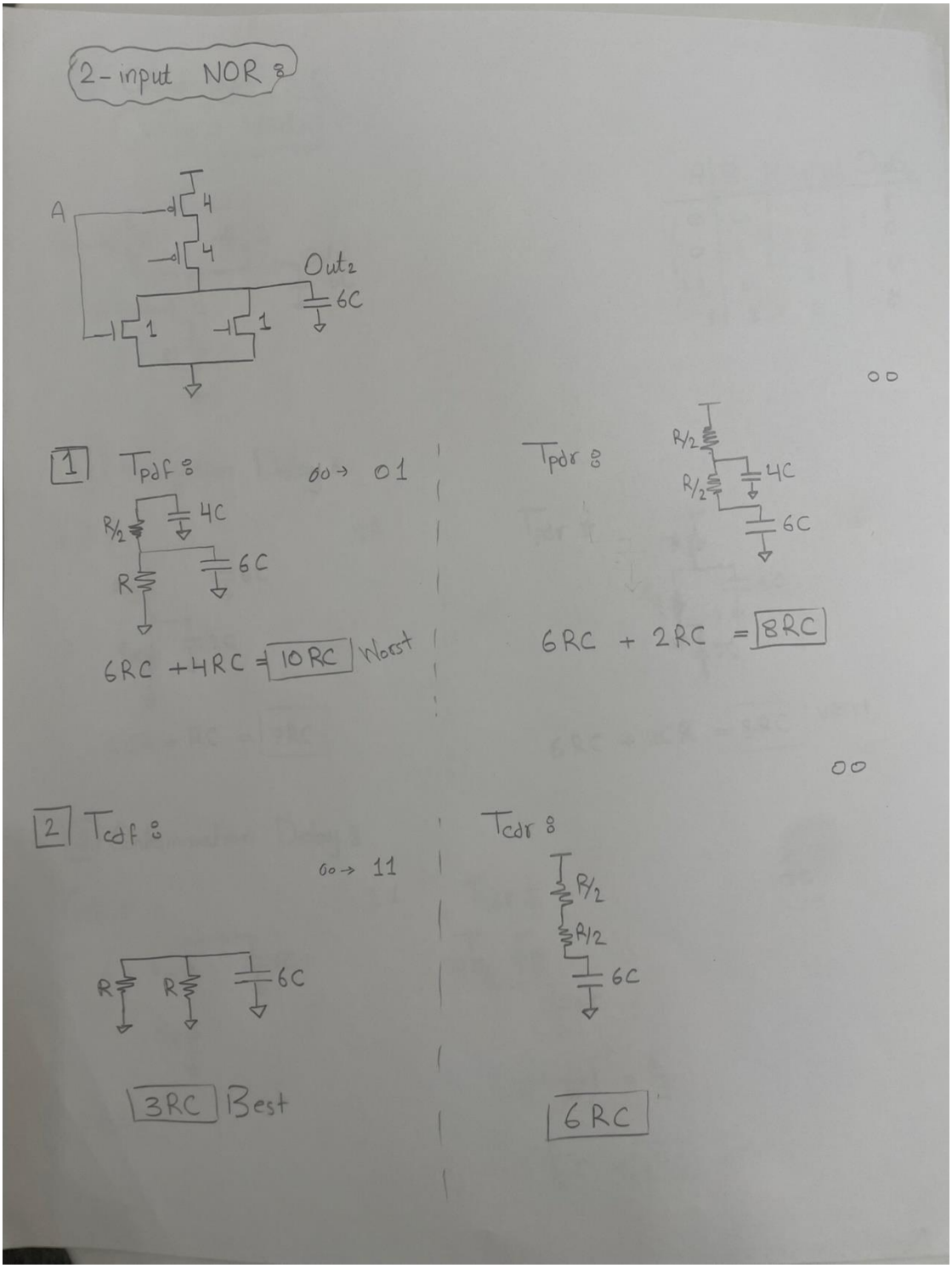

Figure 4: Paper-pencil Calculations for NOR Gate

We then proceeded to implement the 2-input NOR gate in the design with the specified PMOS size of 12 µm and NMOS size of 3 µm. A 100 fF capacitor was included at the output, following the same procedure as for the NAND gate. Afterward, we validated the results using simulations to confirm that the outcomes from our initial analysis were consistent with the simulation data, as shown in the provided picture.

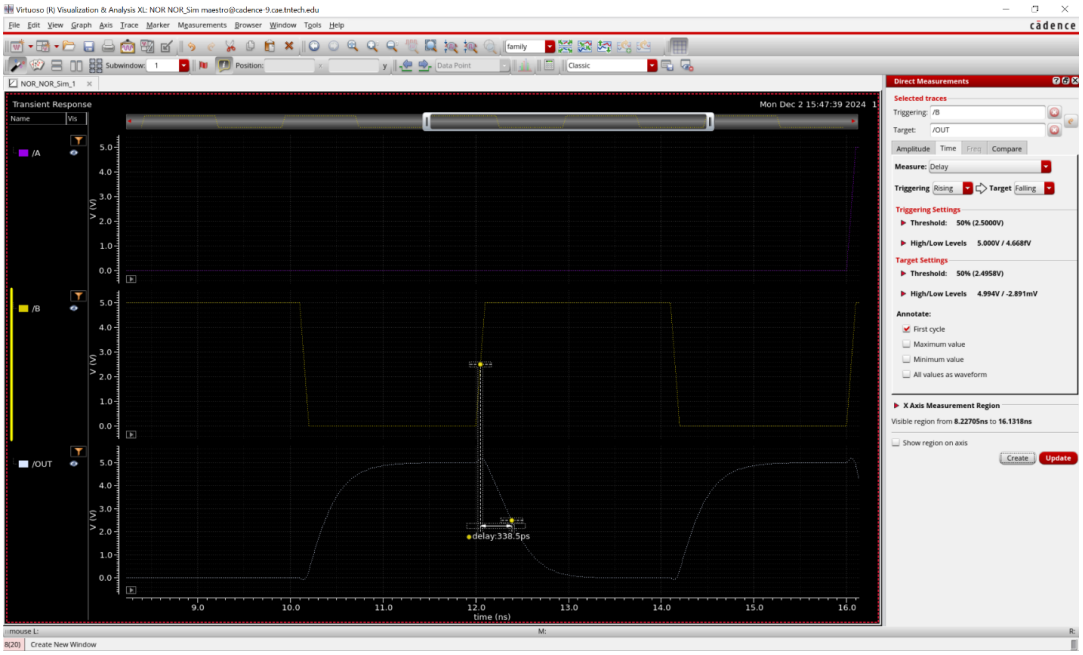

Figure 5: Simulated Propagation Delay for 2 Input NOR Gate

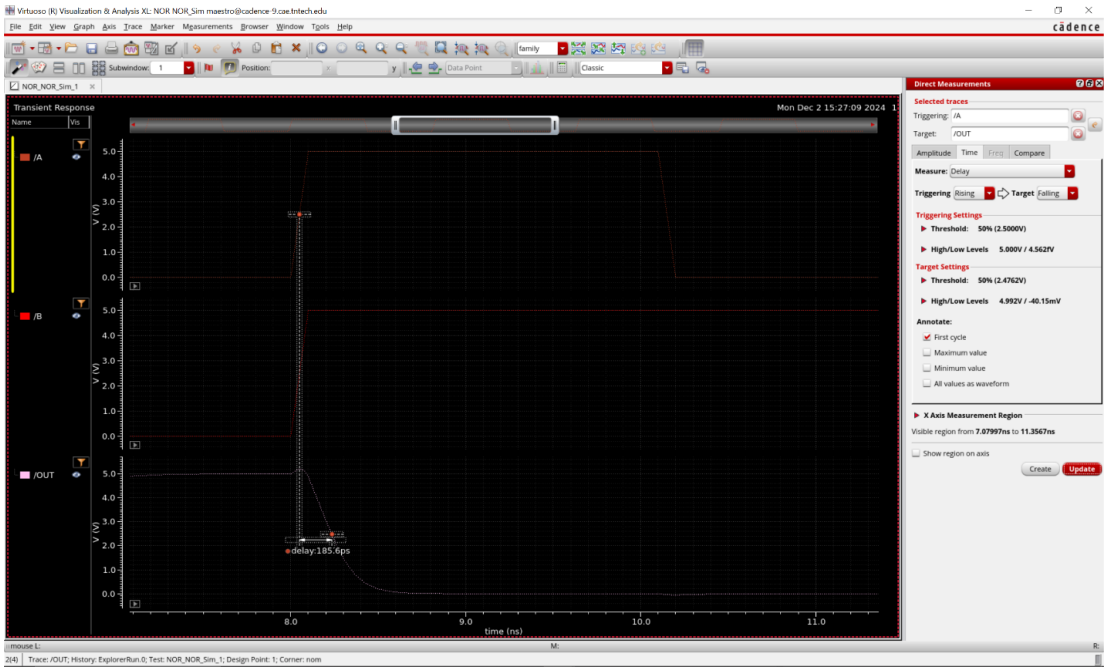

Figure 6: Simulated Contamination Delay of 2 Input NOR Gate

Finally, we compared the simulation results for both the NAND and NOR gates, as summarized in the following table.

	2-NAND	**2-NOR**
T_{pdf}	**7RC**	**10RC**
T_{pdr}	**8RC**	**8RC**
T_{cdf}	**6RC**	**3RC**
T_{cdr}	**3RC**	**6RC**

OBJECTIVE 4

Measure the input capacitance of inverter and in the process find out capacitance per unit transistor (5λ/2λ)

In this task, it is required to find the delay from **c** to **d** and determine the input capacitance of inverter X4 in the following picture. The sizes of the inverters are as follows: X1 is sized as a single unit inverter, X2 is sized as 4 unit inverters, X3 is sized as 8 unit inverters, X4 is sized as 32 unit inverters, and X5 and X6 are sized as 128 unit inverters.

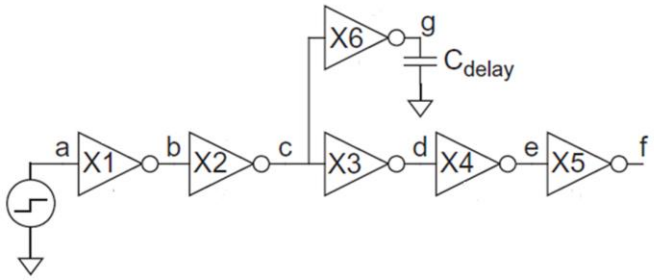

Figure 11: provided circuit

We began by using the unit inverter design that previously done, which had a PMOS size of 2.1 micrometers and an NMOS size of 1.5 micrometers. Specifically, the PMOS had a width-to-length ratio of W/L = 7λ/2λ, and the NMOS had W/L = 5λ/2λ. Using this, we calculated the input capacitance of the X4 inverter, in the design in the following picture. After calculating the capacitance for the X4 inverter, we proceeded to find the input capacitance of a unit inverter with the specified PMOS size of 1.4 micrometers and NMOS size of 1 micrometer. We addressed the following important notes and steps:

- Since the new unit inverter had an input and output capacitance of 2.4 units, we normalized the values using this capacitance. For example, for a 2-input NAND gate, we used the scaling factor $g = \frac{3.4}{2.4}$ and $p = \frac{4.8}{2.4} = 2$.
- For the Cdelay, we swept the capacitance values between 50 fF to 900 fF and then narrowed it down to the appropriate value based on the simulation results.
- To find the capacitance for the unit inverter, we divided the obtained Cdelay by 32, as instructed.
- Additionally, we aimed to determine the capacitance per micron.

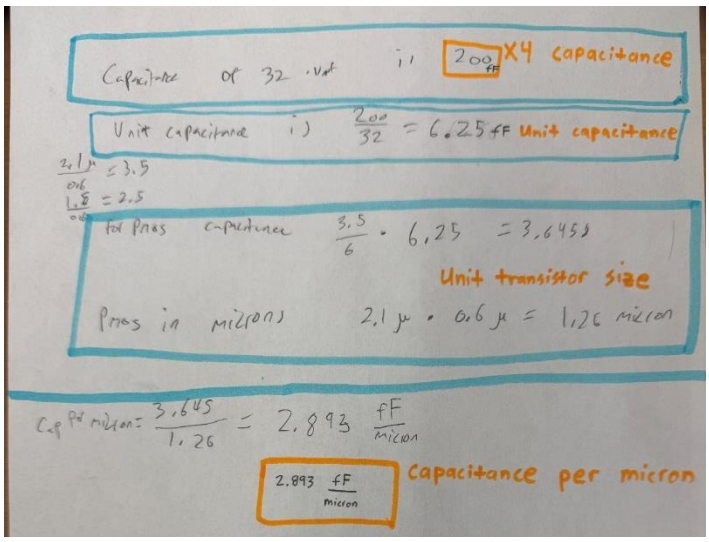

Figure 7: Calculations for Task 6

Finally, we performed simulations and observed the resulting waveforms from the EDA tool. We also verified the transistor-level circuit, ensuring that the MOSFET widths were visible and properly sized. The following pictures include the capacitance values for X4, the unit inverter, the unit transistor, and the capacitance per micron.

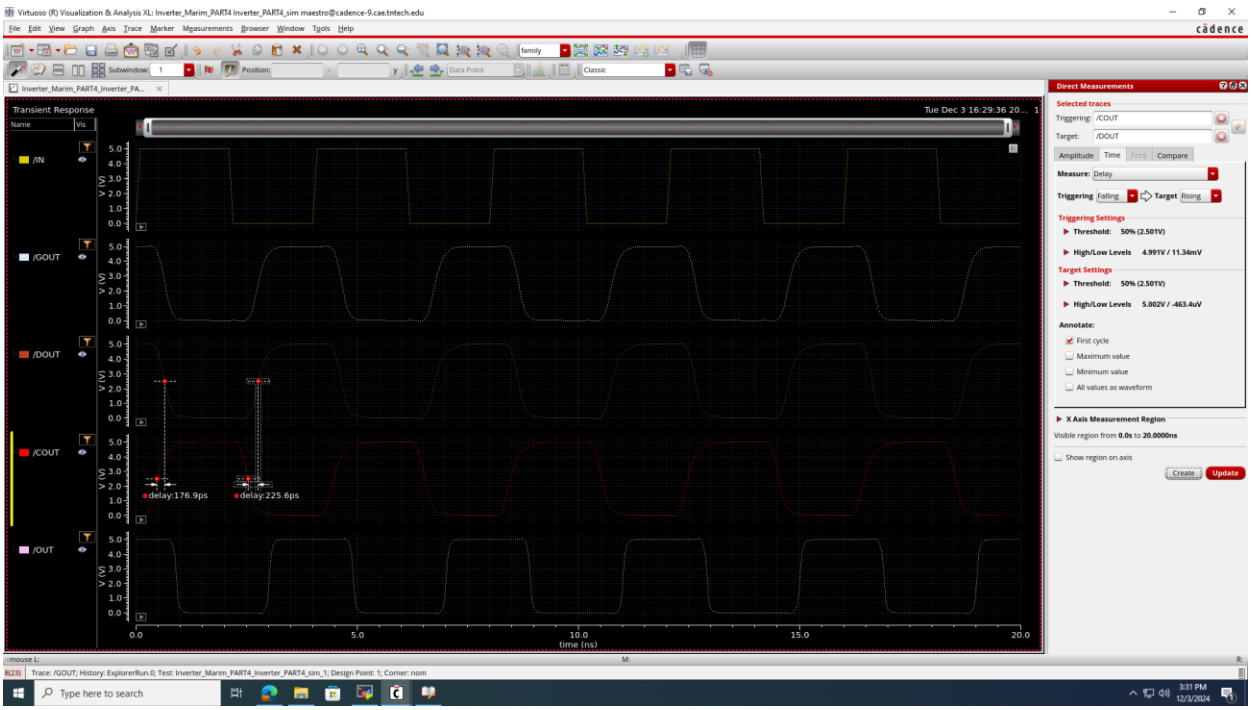

Figure 8: Node C Measured to Node D

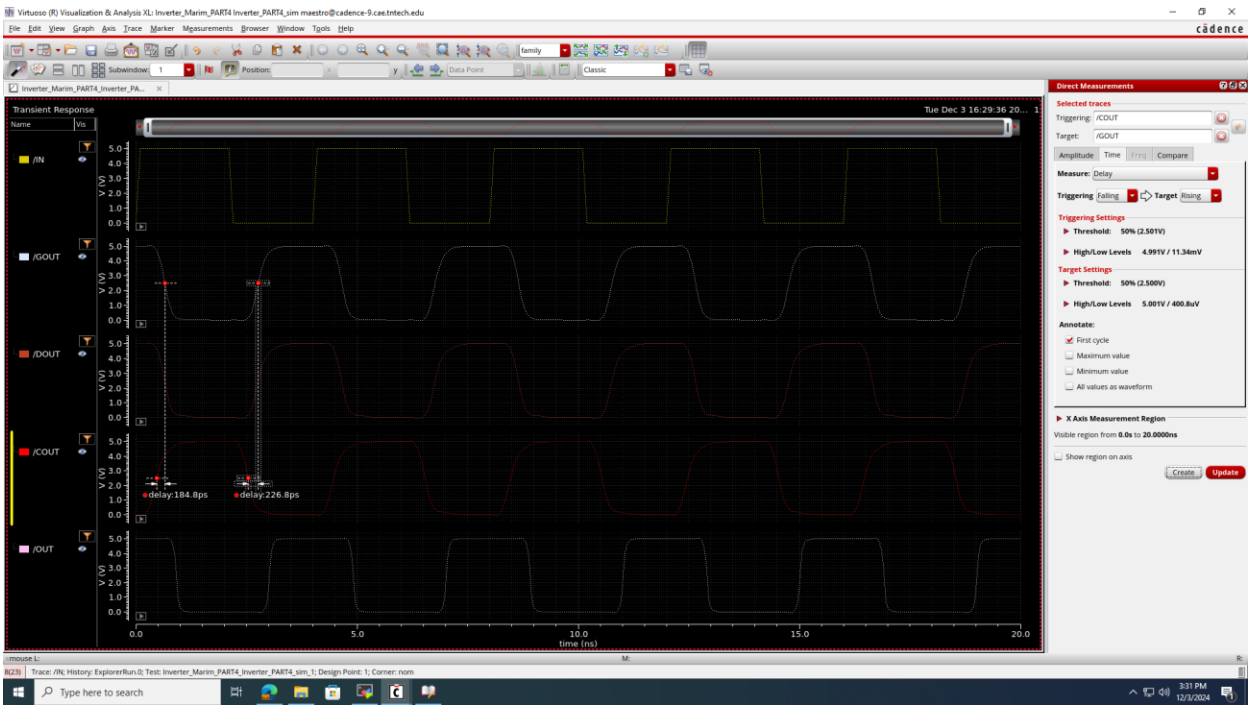

Figure 9: Node C Measured to Node G

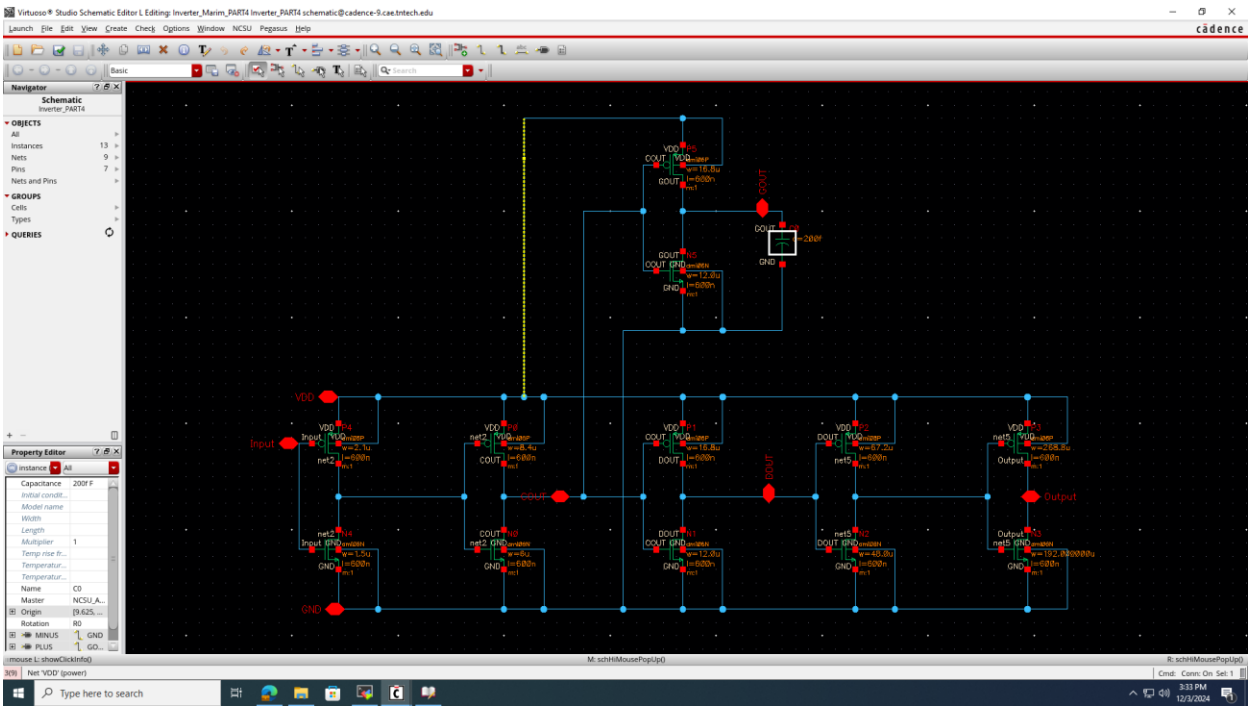

Figure 10: Transistor Level Circuit for Simulation

OBJECTIVE 5

Obtaining the best circuit choice in terms of delay by utilizing theory of logical effort

We were assigned a combination of a compound gate's logic equation, $\overline{(ABC + D)}$, with $C_{out} = 170C$ and our C_{in} represents the capacitance of the compound gate, which results in the worst-case resistance R. The following pictures show:

a) The paper-pencil analysis for the initial sizing of the compound gate, which involves worst-case analysis to ensure that each path has an equivalent resistance to that of a unit simulated inverter.
b) We then proceeded to draw the schematic for the compound gate.
c) We calculated the g values and p values for the compound gate.
d) We estimated the initial number of stages required for the design, considering our design choices, including the possible number of stages we planned to use.
e) Using paper-pencil analysis, we calculated the delays for all the chosen cases and sized the transistors accordingly. We provided the sizing for both the NMOS and PMOS transistors.
f) We compared the results of our paper-pencil analysis with the average-case simulation results in terms of propagation delay. We discussed the differences, noting that while the results may differ, the overall trend should remain consistent.

For the Non-Compound Gates:

g) We explored other possible circuit options to achieve the same load and logic without using compound gates.
h) We documented the steps we took to reach our design choices, including performing calculations to determine the appropriate number of stages.
i) We provided calculations for two different design options.
j) Finally, we confirmed our delay values by comparing them with the simulation results.

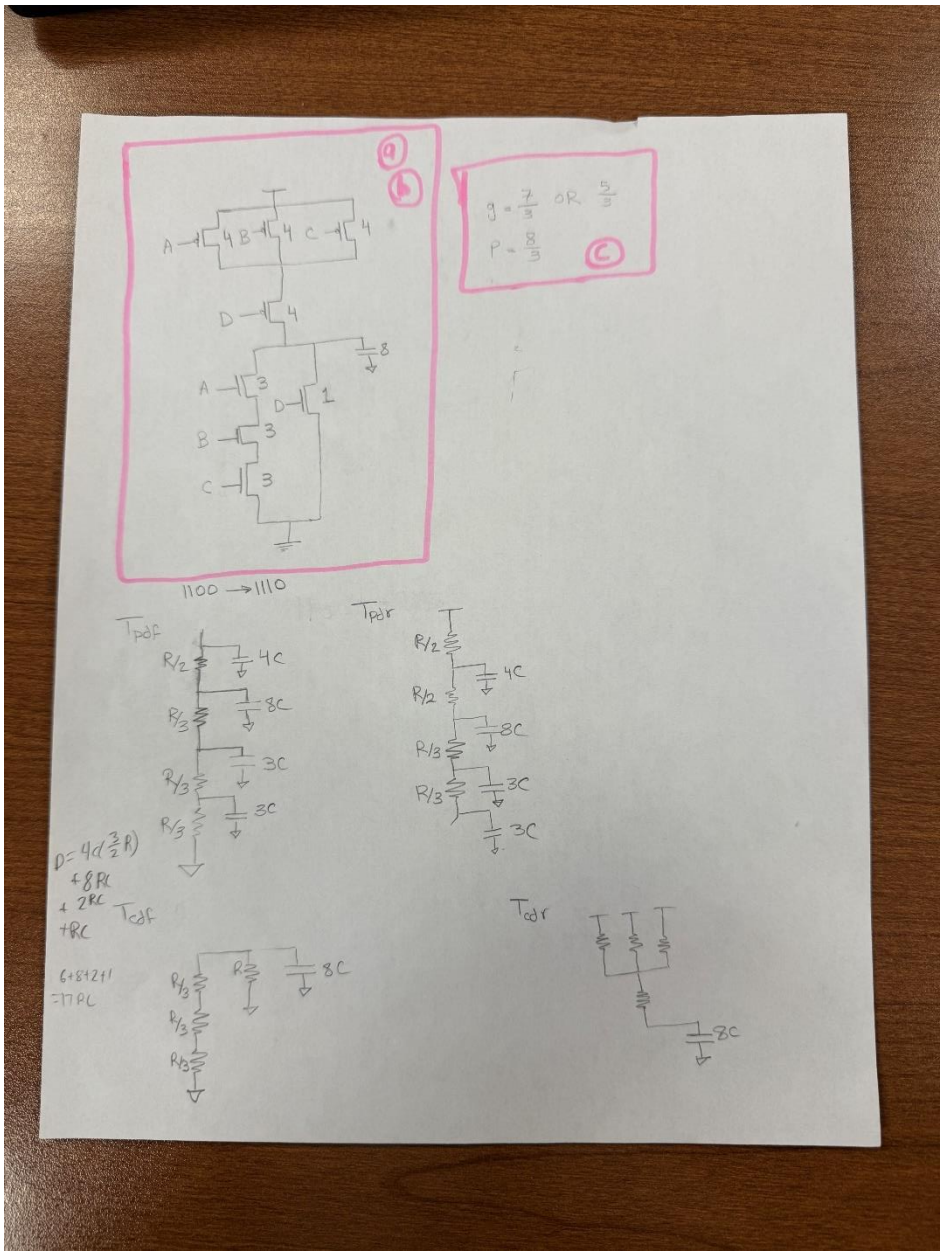

Figure 11: Hand Calculations for Parts A-C

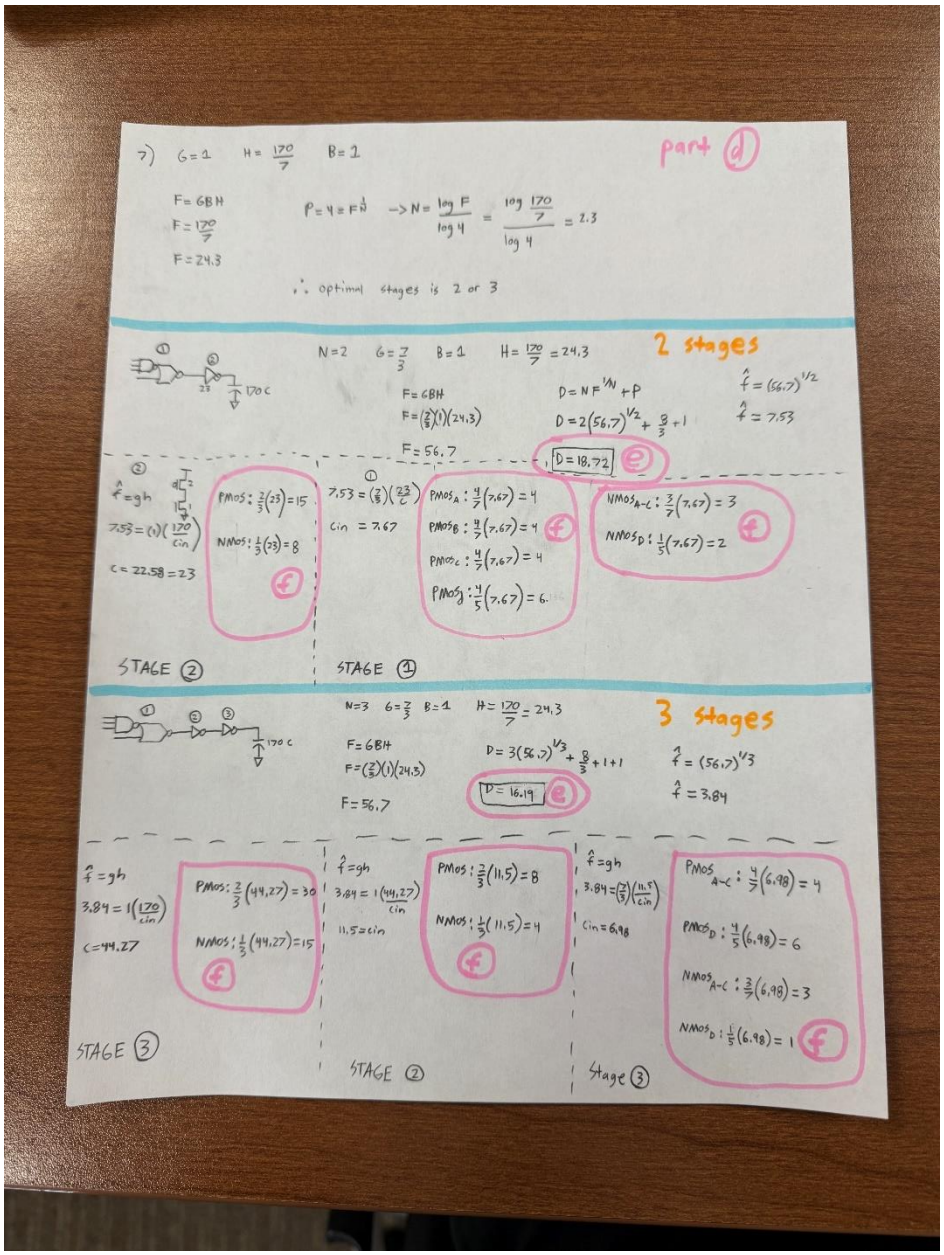

Figure 12: Hand Calculations for Parts D-F

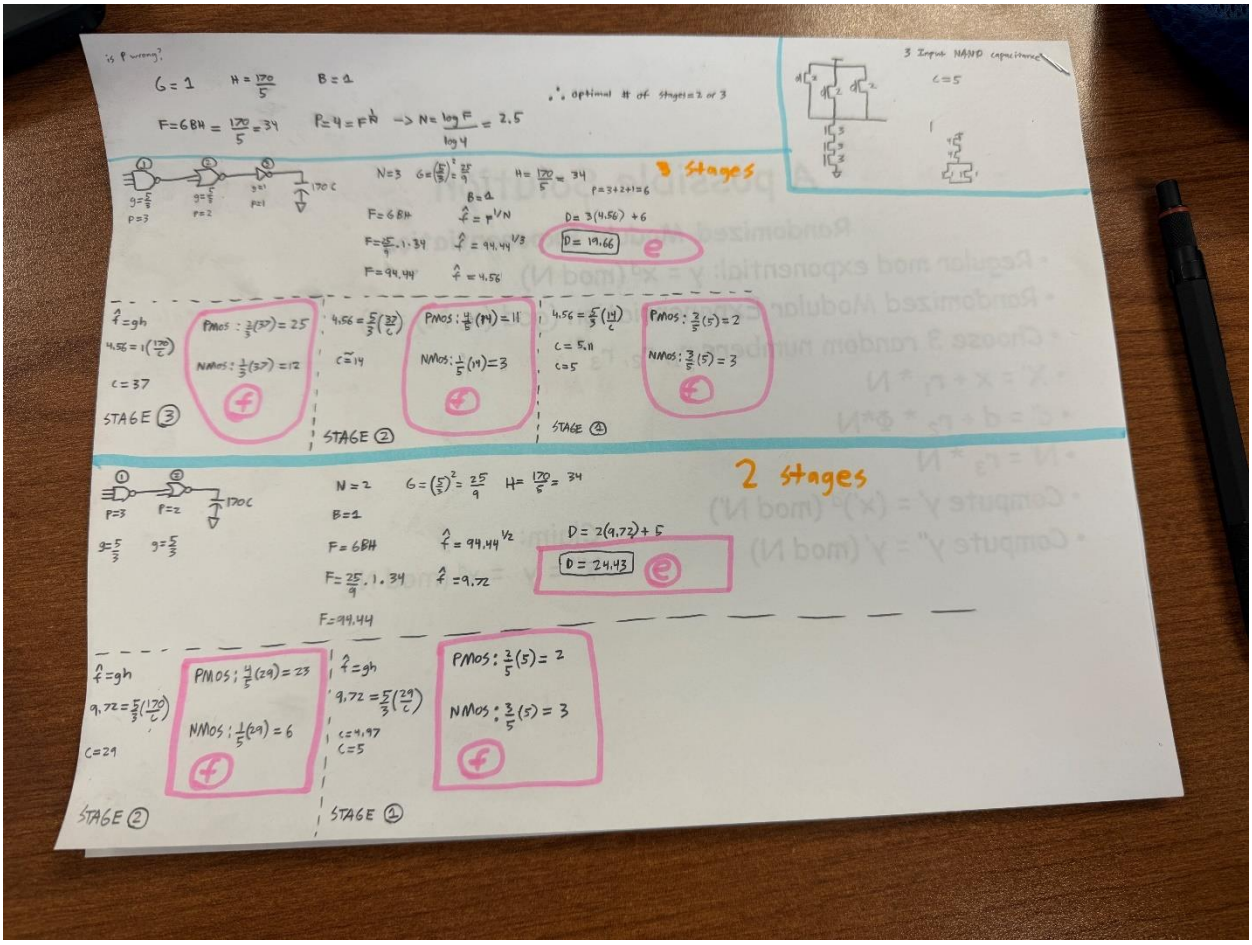

Figure 13: Hand Calculations for Non-Compound Gate

From observing the simulations for compound gate, it can be observed that the delay when 3 stages are used is smaller than the delay when 2 stages are used. For the non-compound gate, its simulation outputs shows that the delay for 3 stages is less than the delay for 2 stages.

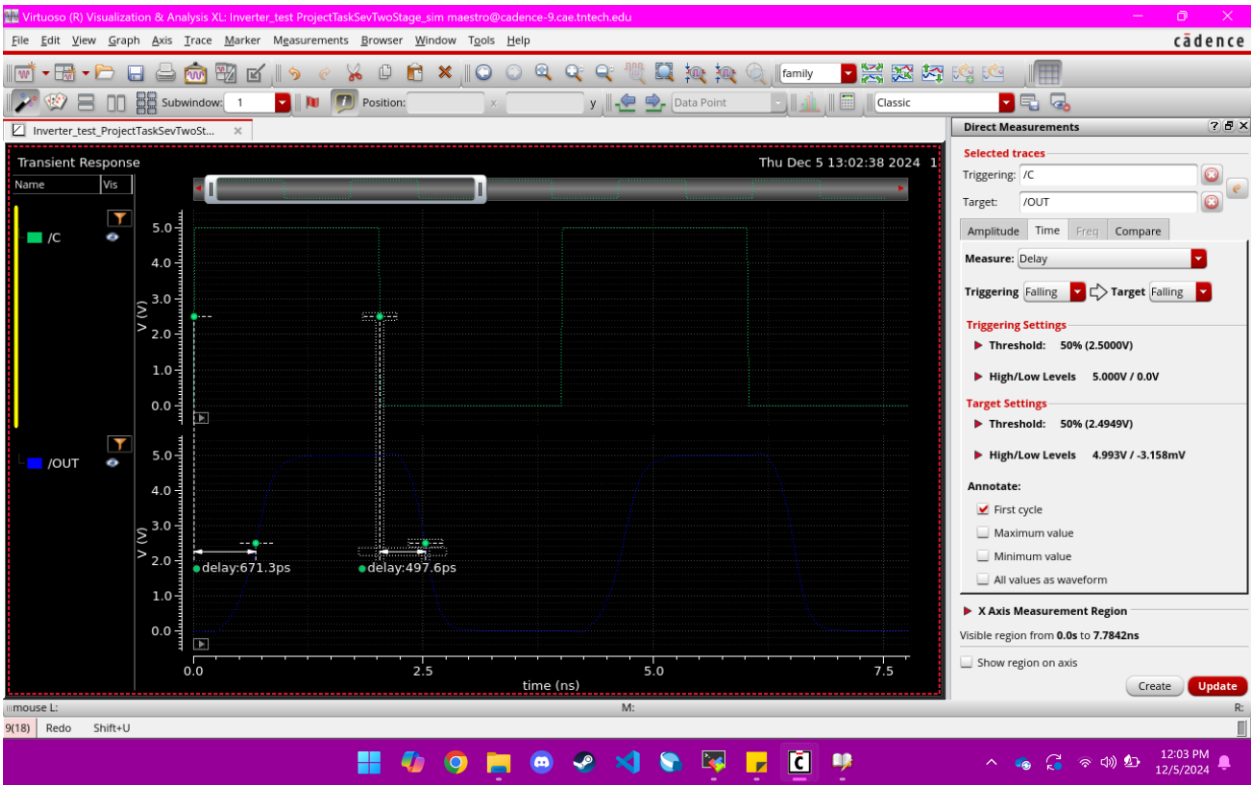

Figure 14: Compound gate 2 stages

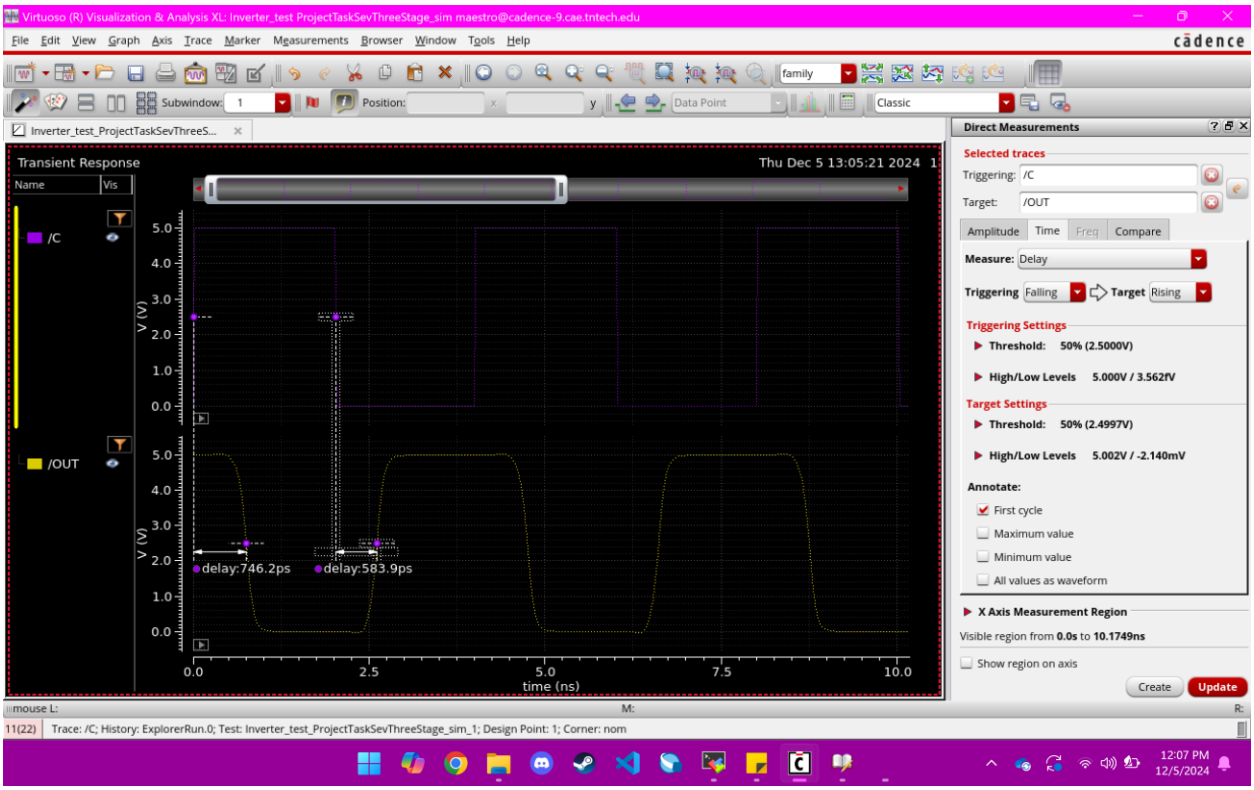

Figure 15: Compound gate 3 stages

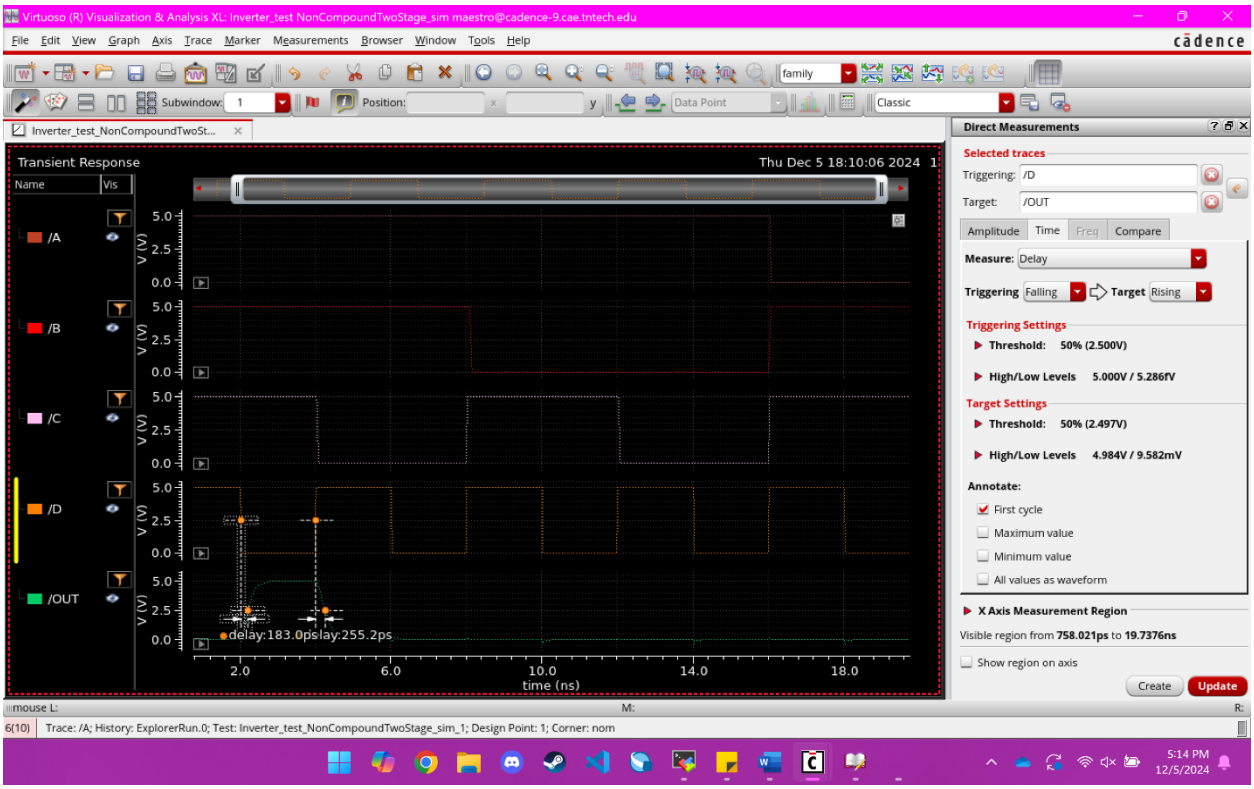

Figure 16: Non compound two stages

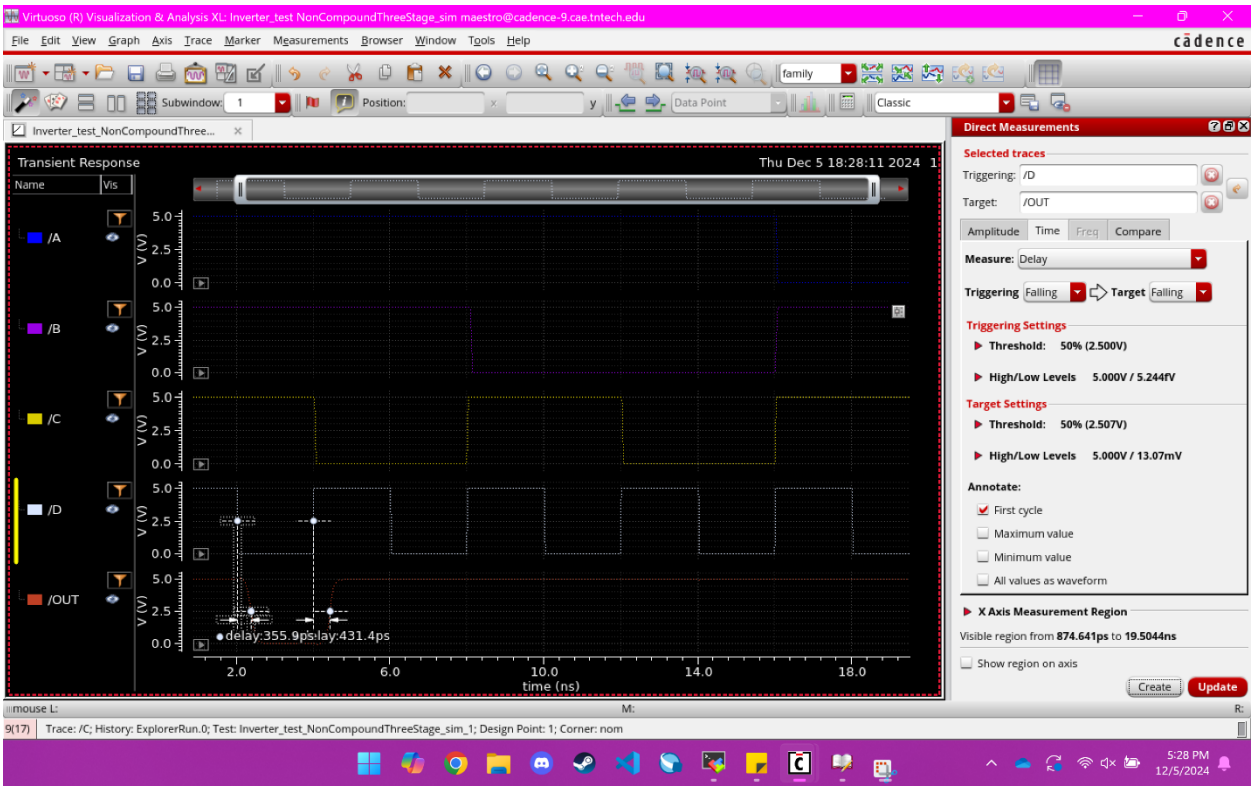

Figure 17: Non compound three stages