**CMPE 315: Principles of VLSI Design**

**Project Cover Page**

**Project Title : Cache Design [ Submission Part 1]**

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**Section : 01**

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**Introduction**

The purpose of this project is to design, implement, and simulate in VHDL, and a layout for a cache block.

**Design Process**

**Chip Design**

**Block Diagram**

Figure x shows the block diagram for the overall design of the chip.

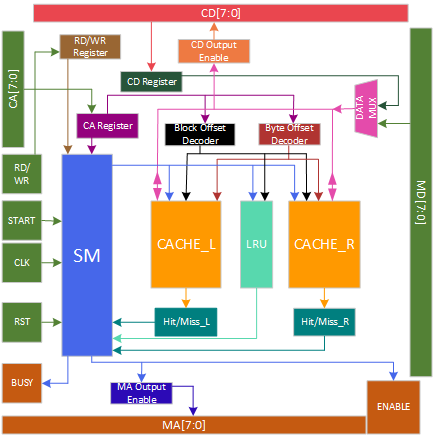


Table x details the inputs and outputs for the chip entity.

|  |  |
| --- | --- |
| Inputs | Outputs |
| CPU Address | Busy |
| CPU Data | Memory Enable |
| CPU RD/WR Signal | Memory Address |
| Start |  |
| CLK |  |
| Reset |  |
| Memory Data |  |
| Vdd |  |
| Gnd |  |

**Cache Design**

The cache is designed using the two-way associative cache design. The cache was designed using a hierarchical design. There is a 1-bit cache, 8-bit cache, cache block, and a full cache.

Figure x shows the schematic design for a 1-bit cache cell.

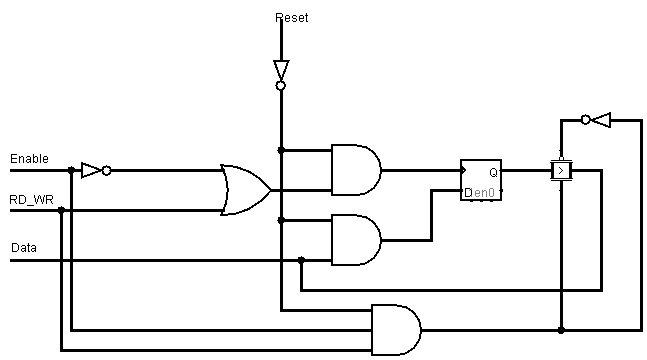


Table x details the input and output signals for each cache.

|  |  |
| --- | --- |
| Inputs | Outputs |
| Reset | Valid Bit Data (vb\_data) |
| Cache Enable Signal (Cache\_en) | Tag Data (tag\_data) |
| Hit/Miss Enable Signal (HM\_en) |  |
| Byte Select (CS) |  |
| Block Select (RS) |  |
| ValidBit/Tag RD/WR Signal (vb\_tag\_rd\_wr) |  |
| RD/WR signal (rd\_wr) |  |
| Valid Bit Data (vb\_data) |  |
| Tag Data (tag\_data) |  |

On a reset, the contents of each cache are zeroed out. The cache enable signal is received from the state machine. The left cache is enabled when this signal is low and the right cache is enabled when the signal goes high. The hit/miss enable signal is used to signify whether the state machine is currently determining whether there is a hit or a miss. When this signal is high, this signifies that both caches must be enabled to check for a hit or miss in both caches. The byte select value is received from the byte offset decoder and is used to select which byte to read or write from. This signal is active low. The block select value is received from the block offset decoder and is used to select which block to read or write from. This signal is active low. The valid and tag rd/wr signal is used to signify whether to read or write to the valid and tag. This signal is being received from the state machine. The rd/wr signal is used to signify whether to read or write to the appropriate byte. The valid bit data and tag data are inputs from the state machine and outputs to the hit/miss entity. The state machine will write this data to the cache when it is performing a read miss operation.

**State Machine Design**

Figure x shows the diagram for the state machine.

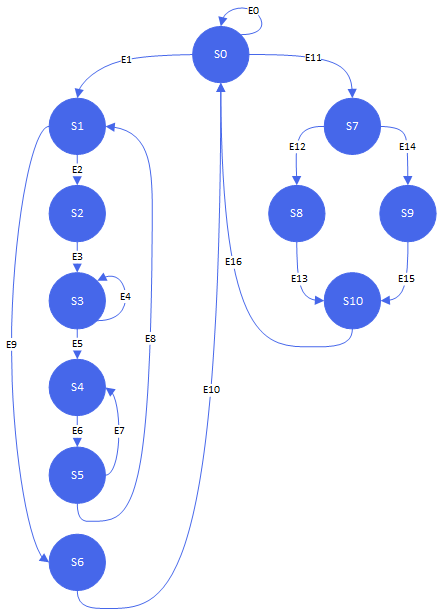


Table x details the inputs and outputs for the state machine

|  |  |
| --- | --- |
| Inputs | Outputs |
| CLK | Busy |
| Reset | CPU Data Output Enable |
| Start | Memory Address Output Enable |
| Hit/Miss Left | Data Mux Select |
| Hit/Miss Right | Valid Bit / Tag RD/WR |
| RD/WR | Cache RD/WR |
| CPU Address | Hit/Miss Enable Signal |
| LRU | Cache Enable |
|  | LRU RD/WR |
|  | Address |
|  | VB Data Left |
|  | VB Data Right |
|  | Tag Data Left |
|  | Tag Data Right |

When the reset input signal goes high, the state machine starts in the initial state 0. For any of the states, if the reset input signal goes high, the state machine will move to state 0. On edge 0, the state machine will remain in state 0 if start input signal remains low. From state 0, if the start signal goes high and the RD/WR input signal signifies a read operation, the state machine will move to state 1, otherwise the state machine will move to state 7 for a write operation. For edges 1 and 11, the busy output signal will be set high and the Hit/Miss output enable signal will be set high indicating that the state machine is currently doing a hit/miss operation.

**Read Operation**

For a read operation, the state machine will wait to receive the outcome of the hit/miss operation. If the hit/miss outcome for the left or right result in read hit, the state machine will move to state 6 on edge 9. During a read hit in state 6, the CPU data output enable signal will be set high. The LRU\_RD\_WR signal is also set low to indicate a write to the LRU. During edge 9, the busy output signal will be set low.

If the hit/miss operation during state 1 for both the left and right result in a read miss, the state machine will move to state 2. During state 2, the memory address is sent along with the memory output enable. The memory address that is sent is based on an address selector. For state 2, the last two bits in the memory address will be the first byte in the block (00).

Figure x shows the schematic for the address selector.

**Write Operation**

For a write operation, the state machine will wait to receive the outcome of the hit/miss operation. If the hit/miss operation for the left or right cache results in a hit, the state machine will move to state 8. During edge 12, the Cache RD/WR output signal will be set to 0 to indicate a write operation. In state 8, the LRU RD/WR output signal will be set to 0 to indicate a write to the LRU.

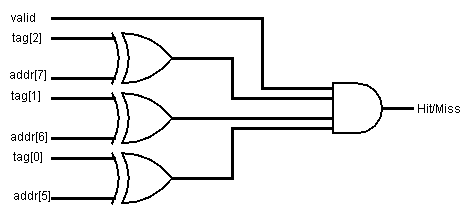
If the write operation results in a miss, the state machine will move to state 9. During a write miss, there is no operations to be made so the state machine will move from state 9 to state 10. During edge 15, the busy output signal will be set low.

**Hit/Miss Design**

Table x details the inputs and outputs for the hit/miss entity.

|  |  |
| --- | --- |
| Inputs | Outputs |
| Valid Data (valid) | Hit\_Miss (h\_m) |
| Tag Data [2:0] (tag) |  |
| CPU Address [7:5] (addr) |  |

Figure x shows the schematic for the hit/miss entity

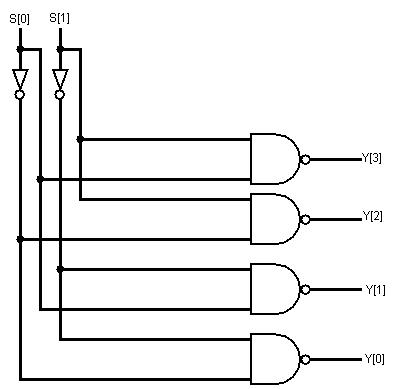


The valid and tag data input for the hit/miss entity is an output from the cache. The CPU address bits and the tag data bits are compared to see whether they match. The output of each xnor gate is then an input for an and gate with the valid bit. The hit/miss entity results in a hit when the valid bit is set to 1 and each CPU address bit matches the tag bits. There is a hit/miss entity for the left and the right cache.

**Decoder Design**

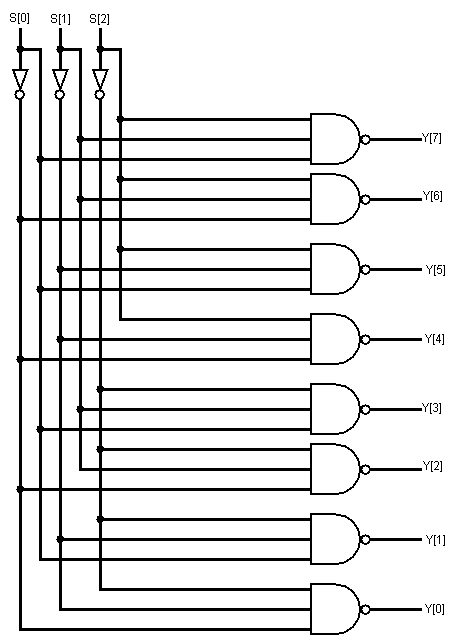
**Byte Offset Decoder**

Figure x shows the schematic design for the 2 to 4 decoder. This decoder is active low and is used for choosing the byte offset.

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**Block Offset Decoder**

Figure x shows the schematic design for the 3 to 8 decoder. This decoder is active low and is used for choosing the block offset.



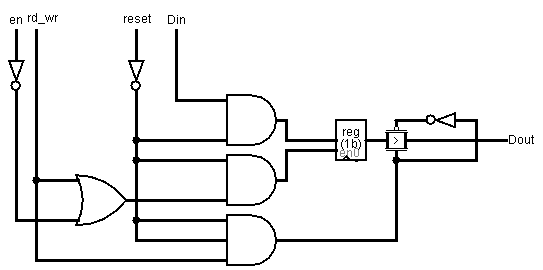
**LRU Design**

For the purpose of block replacement, there is a LRU entity that is used to determine the least recently used block in either of the caches. The LRU value for a block is written to when the state machine is at the end of a read hit/miss operation or a write hit operation. The state machine will read from the LRU entity during a read miss operation to see which cache block to write the new data to.

Table x details the inputs and outputs for the LRU entity.

|  |  |
| --- | --- |
| Inputs | Outputs |
| Enable (en) | Data Out (dout) |
| RD/WR (rd\_wr) |  |
| Reset (reset) |  |
| Data In (din) |  |

Figure x shows the schematic design for the 1 bit LRU entity.



The rd\_wr input signal is a signal from the state machine. When the state machine reads from the LRU, the transmission gate is turned on and the data from the latch will be the output.

Figure x shows the schematic design for the 8 bit LRU entity.

**Data Mux Design**

The data mux is used to select whether to be using memory data or cpu data. The data mux writes out data when

**Entity Architecture Pairs**

|  |  |
| --- | --- |
| **Entity** | **Using the Entity** |
| D\_latch |  |
| reg8 |  |
| oe8 |  |
| mux2to1\_8 |  |
| addr\_sel |  |
|  |  |
|  |  |

**Test Bench & Simulations**

Sample Inputs and Outputs

**Enscripted code**

**Work Break Up Sheet**

|  |  |
| --- | --- |
| **Ben** | **Marinna** |
| Cache Design (code) | Simple Logic Gate Code (and, xnor, tx, nand) |
| State Machine Output Logic | Decoder Design (code) |
|  | State Machine Input Logic |
| Test Benches for Two-way Associative | LRU Design |