**CMPE 315: Principles of VLSI Design**

**Project Cover Page**

**Project Title : Cache Design [ Submission Part 1]**

**Name : Marinna Ricketts-Uy & Ben Thompson**

**Section : 01**

**Date Submitted : April 22, 2018**

**TA / Grader Use Only:**

**Late Submission Deduction (20% per day late):**

**Other Deductions:**

**Final Project Grade:**

**Comments to student:**

**CONTENTS Page#**

**----------------------------------------------------------------------------------------------------------**

**Introduction**

**Chip Design**

Figure x shows the block diagram for the overall design of the chip. The design uses the two way associative cache.

[Insert Block Diagram]

For our design process, we implemented the design for the cache first and then designed the state machine.

**Cache Design**

Description of our design process, doing the two way associative cache

**State Machine Design**

Figure x shows the diagram for the

[Insert State Machine Design]

Detailed Description of the state machine

**Test Bench & Simulations**

Sample Inputs and Outputs

**Enscripted code**