This document describes the architecture and function specifics of AXI4 stream FIFO design.

# Top level

A computer screen shot of a diagram

Description automatically generated

Figure 1. Top level block diagram

## Port list

|  |  |  |
| --- | --- | --- |
| **Parameter name** | **Default value** | **Description** |
| DATA\_WIDTH | 8 | Integer Width of input and output data ports – acceptable values: 8, 16, 32, 64 |

Table 1. Top-level parameters

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **Direction** | **Bus width** | **Clock domain** | **Description** |
| s\_axis\_clk | I | 1 | - | Slave AXIS input clock |
| m\_axis\_clk | I | 1 | - | Slave AXIS output clock |
| m\_axis\_aresetn | I | 1 | s\_axis\_clk | Sync reset. Active low. |
| s\_axis\_tdata | I | DATA\_WIDTH | s\_axis\_clk | Slave (input) AXIS data bus |
| s\_axis\_tvalid | I | 1 | s\_axis\_clk | AXIS data valid flag |
| s\_axis\_tready | O | 1 | s\_axis\_clk | Slave (input) AXIS ready to receive |
| m\_axis\_tdata | O | DATA\_WIDTH | m\_axis\_clk | Master (output) AXIS data bus |
| m\_axis\_tvalid | O | 1 | m\_axis\_clk | Master (output) AXIS data valid flag |
| m\_axis\_tready | I | 1 | m\_axis\_clk | Master (output) AXIS ready to receive flag |

Table 2. Top-level parameters

TBD