FPGA ICE40HX1K 12MHz clk_div_ice_m 60MHz clk_div rst ULPI_clk) btn1 clk_out< ->clk_in clk_pulse X btn_debouncer LED_CLK_ICE_DIV_EN enable IO_BTNs[0](reset) btn_out btn2_trigger btn2 signal_trigger btn_debouncer clk_div_ULPI_m IO_BTNs[1](test) btn_in clk div btn_out input_signal output_signal clk_div_btn 60MHz clk_div clk_out< clk_in clk_pulse X clk_out< LED_CLK_ULPI_DIV_EN enable clk_pulse X IO_LEDs[0](clk_div_ice) enable UART IO_LEDs[1](clk_div_ULPI)) 1 10_LEDs[2](rst) 24 (IO_LEDs[3](ULPI_DIR) ULPI_op_stack 19 ULPI_op_stack UART_Rx) clk_Rx —X 10_LEDs[4](btn2_debounce) clk_Tx -X 0_DATA [8] [8] _{I_DATA} UART_Tx> [8] UART_DATA TiP X UART NxT UART_Rx_EMPTY NrD X send_data Tx_FULL op_stack_msg [16] NxT Rx_FULL -X op_stack_full —X op_stack_pull Rx_EMPTY op_stack_empty 3750000 ULPI ULPI rst clk_ice clk_ULPI PrW status -X main_controller PrR busy main_controller _[6] ADDR REG_VAL_W REG_VAL_R [8] force_send RxCMD -X RxLineState X [16] op_stack_msg RxVbusState X op_stack_pull op_stack_empty RxActive -X RxError X ULPI_busy RxHostDisconnect X _[8] ULPI_USB_DATA
_[16] ULPI_USB_INFO_DATA RxID X USB_DATA [8]
USB_INFO_DATA [16] ULPI_DATA_re ULPI_DATA_buff_empty ULPI_INFO_re ULPI_INFO_buff_empty DATA_re DATA_buff_full —X INFO_re DATA_buff_empty ULPI_REG_VAL_W [8] ULPI_ADDR [6] INFO_buff_full -X [8] ULPI_REG_VAL_R INFO_buff_empty ULPI_PrW DATA_out [8] ULPI_PrR ULPI_DIR) ULPI_STP) STP [8] NXT DATA_in UART_Tx_DATA [8] U_RST UART_Tx_FULL UART_send ULPI_NXT) ULPI_RST) (ULPI_DATA[7:0]