FPGA ICE40HX1K

12MHz

ULPI_clk

IO_BTNs[0](reset)

IO_BTNs[1](test)

UART_Rx

ULPI_DIR

ULPI_NXT

ULPI_DATA[7:0]

12MHz
60MHz
rst

btn1
btn_debouncer
clk
btn_in
btn_out

btn2
btn_debouncer
clk
btn_in
btn_out

btn2_trigger
signal_trigger
clk
input_signal
output_signal

60MHz
clk_div_btn
clk_div
clk_in
clk_out
clk_pulse
enable
DIVIDER
1
19

UART
UART
rst
clk
Rx
Tx
clk_Rx
clk_Tx
[8]
I_DATA
O_DATA
[8]
TiP
NrD
send_data
NxT
Tx_FULL
Rx_FULL
Rx_EMPTY
BAUDS
3750000

ULPI
ULPI
rst
clk_ice
clk_ULPI
PrW
PrR
[6]
[8]
ADDR
REG_VAL_W
status
busy
REG_VAL_R
[8]
RxCMD
RxLineState
RxVbusState
RxActive
RxError
RxHostDisconnect
RxID
USB_DATA
USB_INFO_DATA
[8]
[16]
DATA_re
INFO_re
DATA_buff_full
DATA_buff_empty
INFO_buff_full
INFO_buff_empty
DIR
NXT
[8]
DATA_in
DATA_out
[8]
STP
U_RST

ULPI_op_stack
ULPI_op_stack
rst
clk
[8]
UART_DATA
UART_Rx_EMPTY
UART_NxT
op_stack_pull
op_stack_msg
op_stack_full
op_stack_empty
[16]

main_controller
main_controller
rst
clk
force_send
[16]
op_stack_msg
op_stack_empty
op_stack_pull
ULPI_busy
[8]
[16]
ULPI_USB_DATA
ULPI_USB_INFO_DATA
ULPI_DATA_buff_empty
ULPI_INFO_buff_empty
[8]
ULPI_REG_VAL_R
ULPI_REG_VAL_W
ULPI_ADDR
ULPI_PrW
ULPI_PrR
ULPI_DATA_re
ULPI_INFO_re
[8]
[6]
[8]
UART_Tx_FULL
UART_Tx_DATA
UART_send

clk_div_ice_m
clk_div
clk_in
clk_out
clk_pulse
enable
DIVIDER
LED_CLK_ICE_DIV_EN

clk_div_ULPI_m
clk_div
clk_in
clk_out
clk_pulse
enable
DIVIDER
LED_CLK_ULPI_DIV_EN
24

IO_LEDs[0](clk_div_ice)
IO_LEDs[1](clk_div_ULPI)
IO_LEDs[2](rst)
IO_LEDs[3](ULPI_DIR)
IO_LEDs[4](btn2_debounce)
UART_Tx
ULPI_STP
ULPI_RST

[8]
6
0
1
2
[8]