

# Integrated Silicon Pressure Sensor On-Chip Signal Conditioned, Temperature Compensated and Calibrated

The MPxx5010 series piezoresistive transducers are state-of-the-art monolithic silicon pressure sensors designed for a wide range of applications, but particularly those employing a microcontroller or microprocessor with A/D inputs. This transducer combines advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure. The axial port has been modified to accommodate industrial grade tubing.

## Features

- 5.0% Maximum Error over 0° to 85°C
- Ideally Suited for Microprocessor or Microcontroller-Based Systems
- Durable Epoxy Unibody and Thermoplastic (PPS) Surface Mount Package
- Temperature Compensated over -40° to +125°C
- Patented Silicon Shear Stress Strain Gauge
- Available in Differential and Gauge Configurations
- Available in Surface Mount (SMT) or Through-hole (DIP) Configurations

## MPX5010 MPXV5010 MPVZ5010 Series

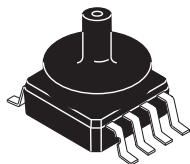
0 to 10 kPa (0 to 1.45 psi)  
(0 to 1019.78 mm H<sub>2</sub>O)  
0.2 to 4.7 V Output

## Application Examples

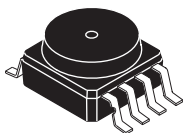
- Hospital Beds
- HVAC
- Respiratory Systems
- Process Control
- Washing Machine Water Level Measurement (Reference AN1950)
- Ideally Suited for Microprocessor or Microcontroller-Based Systems
- Appliance Liquid Level and Pressure Measurement

ORDERING INFORMATION								
Device Name	Case No.	# of Ports			Pressure Type			Device Marking
		None	Single	Dual	Gauge	Differential	Absolute	
Unibody Package (MPX5010 Series)								
MPX5010DP	867C			•		•		MPX5010DP
MPX5010GP	867B		•		•			MPX5010GP
MPX5010GS	867E		•		•			MPX5010D
MPX5010GSX	867F		•		•			MPX5010D
Small Outline Package (MPXV5010 Series)								
MPXV5010DP	1351			•		•		MPXV5010DP
MPXV5010G6U	482	•			•			MPXV5010G
MPXV5010GC6T1	482A		•		•			MPXV5010G
MPXV5010GC6U	482A		•		•			MPXV5010G
MPXV5010GC7U	482C		•		•			MPXV5010G
MPXV5010GP	1369		•		•			MPXV5010GP
Small Outline Package (Media Resistant Gel) (MPVZ5010 Series)								
MPVZ5010G6U	482	•			•			MPVZ5010G
MPVZ5010G7U	482B	•			•			MPVZ5010G
MPVZ5010GW6U	1735		•		•			MZ5010GW
MPVZ5010GW7U	1560		•		•			MZ5010GW

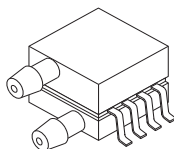
## SMALL OUTLINE PACKAGES SURFACE MOUNT



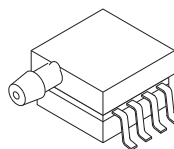
**MPXV5010GC6U/C6T1**  
CASE 482A-01



**MPXV5010G6U,  
MPVZ5010G6U**  
CASE 482-01



**MPXV5010DP**  
CASE 1351-01

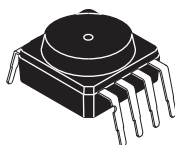


**MPXV5010GP**  
CASE 1369-01

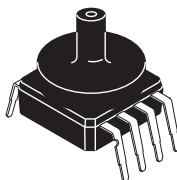


**MPVZ5010GW6U**  
CASE 1735-01

## SMALL OUTLINE PACKAGES THROUGH-HOLE



**MPVZ5010G7U**  
CASE 482B-03

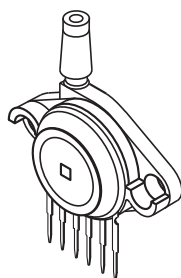


**MPXV5010GC7U**  
CASE 482C-03

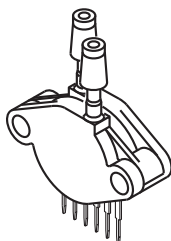


**MPVZ5010GW7U**  
CASE 1560-02

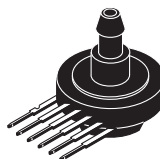
## UNIBODY PACKAGES



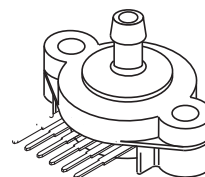
**MPX5010GP**  
CASE 867B-04



**MPX5010DP**  
CASE 867C-05



**MPX5010GS**  
CASE 867E-03



**MPX5010GSX**  
CASE 867F-03

## Operating Characteristics

**Table 1. Operating Characteristics** ( $V_S = 5.0$  Vdc,  $T_A = 25^\circ\text{C}$  unless otherwise noted,  $P_1 > P_2$ . Decoupling circuit shown in Figure 3 required to meet specification.)

Characteristic	Symbol	Min	Typ	Max	Unit
Pressure Range	$P_{OP}$	0	—	10 1019.78	kPa mm H <sub>2</sub> O
Supply Voltage <sup>(1)</sup>	$V_S$	4.75	5.0	5.25	Vdc
Supply Current	$I_o$	—	5.0	10	mAdc
Minimum Pressure Offset <sup>(2)</sup> @ $V_S = 5.0$ Volts	$V_{off}$	0	0.2	0.425	Vdc
Full Scale Output <sup>(3)</sup> @ $V_S = 5.0$ Volts	$V_{FSO}$	4.475	4.7	4.925	Vdc
Full Scale Span <sup>(4)</sup> @ $V_S = 5.0$ Volts	$V_{FSS}$	4.275	4.5	4.725	Vdc
Accuracy <sup>(5)</sup>	—	—	—	±5.0	% $V_{FSS}$
Sensitivity	V/P	—	450 4.413	—	mV/mm mV/mm H <sub>2</sub> O
Response Time <sup>(6)</sup>	$t_R$	—	1.0	—	ms
Output Source Current at Full Scale Output	$I_{O+}$	—	0.1	—	mAdc
Warm-Up Time <sup>(7)</sup>	—	—	20	—	ms
Offset Stability <sup>(8)</sup>	—	—	±0.5	—	% $V_{FSS}$

1. Device is ratiometric within this specified excitation range.

2. Offset ( $V_{off}$ ) is defined as the output voltage at the minimum rated pressure.

3. Full Scale Output ( $V_{FSO}$ ) is defined as the output voltage at the maximum or full rated pressure.

4. Full Scale Span ( $V_{FSS}$ ) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.

5. Accuracy (error budget) consists of the following:

Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.

Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.

Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the minimum or maximum rated pressure, at  $25^\circ\text{C}$ .

TcSpan: Output deviation over the temperature range of  $0^\circ$  to  $85^\circ\text{C}$ , relative to  $25^\circ\text{C}$ .

TcOffset: Output deviation with minimum rated pressure applied, over the temperature range of  $0^\circ$  to  $85^\circ\text{C}$ , relative to  $25^\circ\text{C}$ .

Variation from Nominal: The variation from nominal values, for Offset or Full Scale Span, as a percent of  $V_{FSS}$ , at  $25^\circ\text{C}$ .

6. Response Time is defined as the time for the incremental change in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.

7. Warm-up Time is defined as the time required for the product to meet the specified output voltage after the Pressure has been stabilized.

8. Offset Stability is the product's output deviation when subjected to 1000 hours of Pulsed Pressure, Temperature Cycling with Bias Test.

## Maximum Ratings

Table 2. Maximum Ratings<sup>(1)</sup>

Rating	Symbol	Value	Unit
Maximum Pressure (P1 > P2)	P <sub>max</sub>	40	kPa
Storage Temperature	T <sub>stg</sub>	−40 to +125	°C
Operating Temperature	T <sub>A</sub>	−40 to +125	°C

1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.

Figure 1 shows a block diagram of the internal circuitry integrated on a pressure sensor chip.

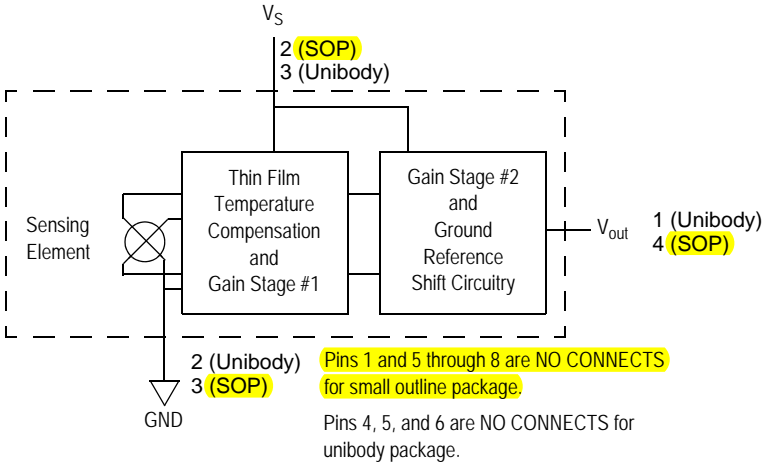


Figure 1. Fully Integrated Pressure Sensor Schematic

## ON-CHIP TEMPERATURE COMPENSATION AND CALIBRATION

The performance over temperature is achieved by integrating the shear-stress strain gauge, temperature compensation, calibration and signal conditioning circuitry onto a single monolithic chip.

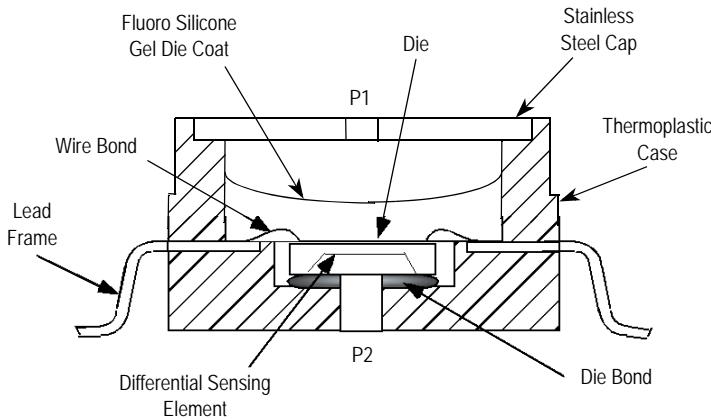
Figure 3 illustrates the Differential or Gauge configuration in the basic chip carrier (Case 482). A fluorosilicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the sensor diaphragm.

The MPxx5010G series pressure sensor operating characteristics, and internal reliability and qualification tests are based on use of dry air as the pressure media. Media,

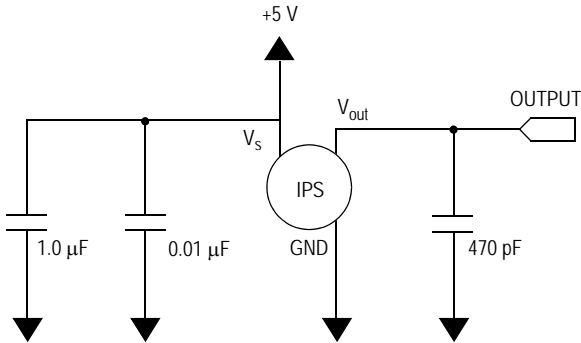
other than dry air, may have adverse effects on sensor performance and long-term reliability. Contact the factory for information regarding media compatibility in your application.

Figure 4 shows the recommended decoupling circuit for interfacing the integrated sensor to the A/D input of a microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

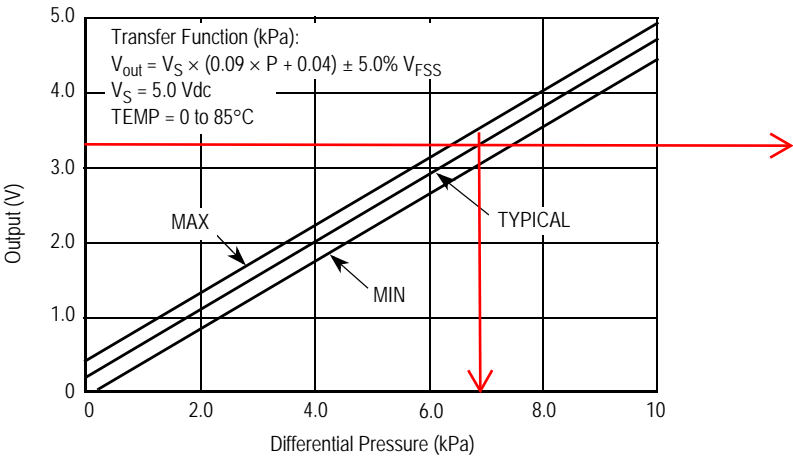
Figure 5 shows the sensor output signal relative to pressure input. Typical, minimum, and maximum output curves are shown for operation over a temperature range of 0° to 85°C using the decoupling circuit shown in Figure 4. The output will saturate outside of the specified pressure range.



**Figure 2. Cross-Sectional Diagram SOP (not to scale)**



**Figure 3. Recommended Power Supply Decoupling and Output Filtering**  
(For additional output filtering, please refer to Application Note AN1646.)

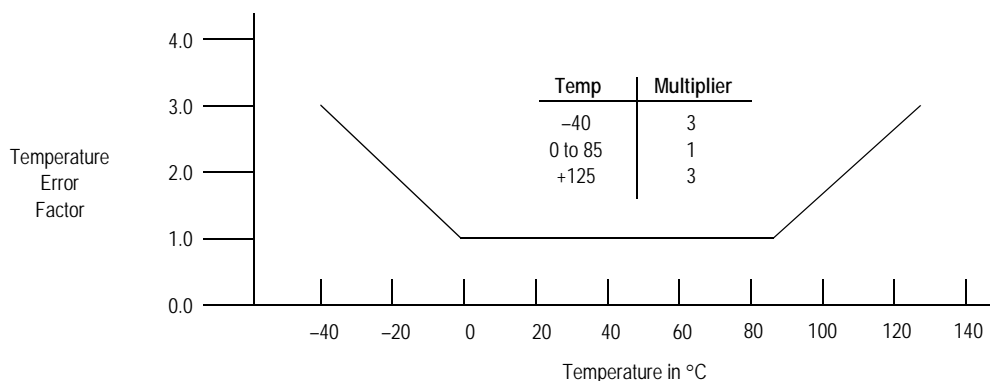


**Figure 4. Output vs. Pressure Differential**

## Transfer Function

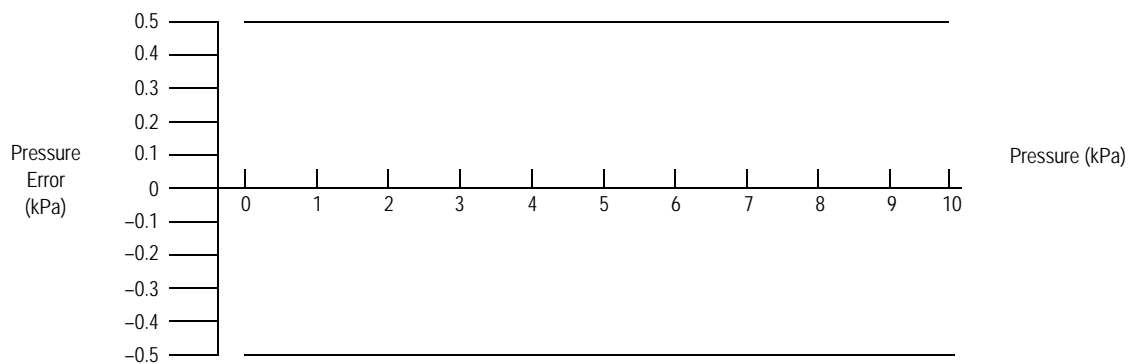
**Nominal Transfer Value:**  $V_{out} = V_S \times (0.09 \times P + 0.04)$   
 $\pm (\text{Pressure Error} \times \text{Temp. Factor} \times 0.09 \times V_S)$   
 $V_S = 5.0 \text{ V} \pm 0.25 \text{ Vdc}$

## Temperature Error Band



NOTE: The Temperature Multiplier is a linear response from 0° to -40°C and from 85° to 125°C.

## Pressure Error Band



Pressure	Error (Max)
0 to 10 (kPa)	±0.5 (kPa)

**PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE**

Freescale designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing fluorosilicone gel which protects the die from harsh media. The MPX pressure

sensor is designed to operate with positive differential pressure applied,  $P1 > P2$ .

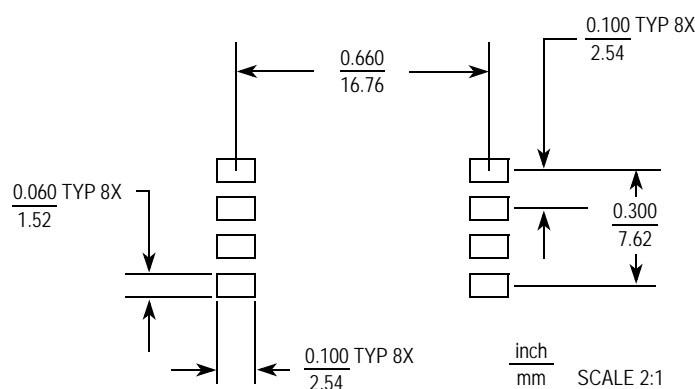
The Pressure (P1) side may be identified by using the table below:

Part Number	Case Type	Pressure (P1) Side Identifier
MPX5010DP	867C	Side with Part Marking
MPX5010GP	867B	Side with Port Attached
MPX5010GS	867E	Side with Port Attached
MPX5010GSX	867F	Side with Port Attached
MPXV5010G6U	482	Stainless Steel Cap
MPXV5010GC6U/6T1	482A	Side with Port Attached
MPXV5010GC7U	482C	Side with Port Attached
MPXV5010GP	1369	Side with Port Attached
MPXV5010DP	1351	Side with Part Marking
MPVZ5010G6U	482	Stainless Steel Cap
MPVZ5010G7U	482B	Stainless Steel Cap
MPVZ5010GW6U	1735	Vertical Port Attached
MPVZ5010GW7U	1560	Vertical Port Attached

**MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS**

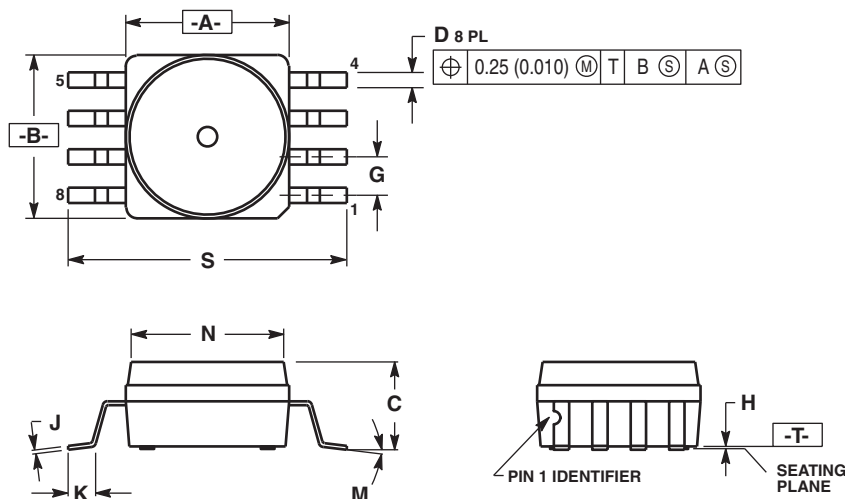
Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct

footprint, the packages will self align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.



**Figure 5. SOP Footprint (Case 482)**

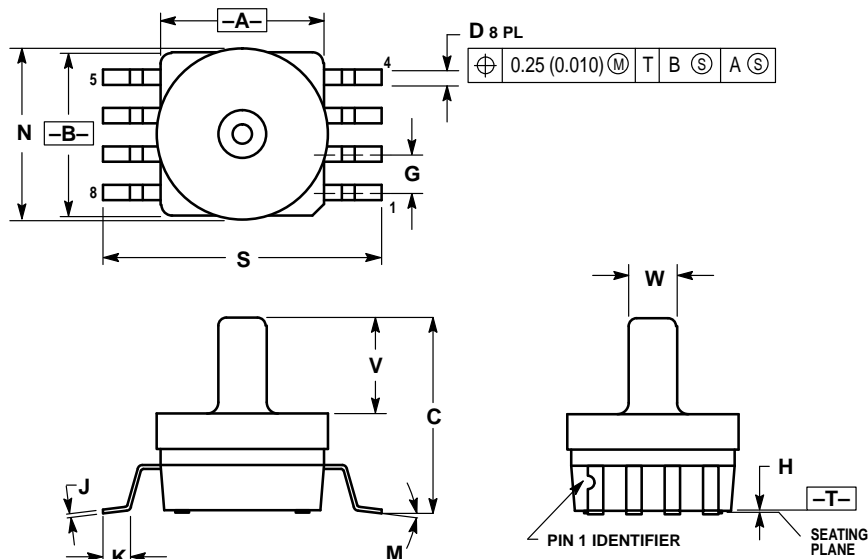
# PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
  5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.212	0.230	5.38	5.84
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
H	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0°	7°	0°	7°
N	0.405	0.415	10.29	10.54
S	0.709	0.725	18.01	18.41

**CASE 482-01  
ISSUE O  
SMALL OUTLINE PACKAGE**



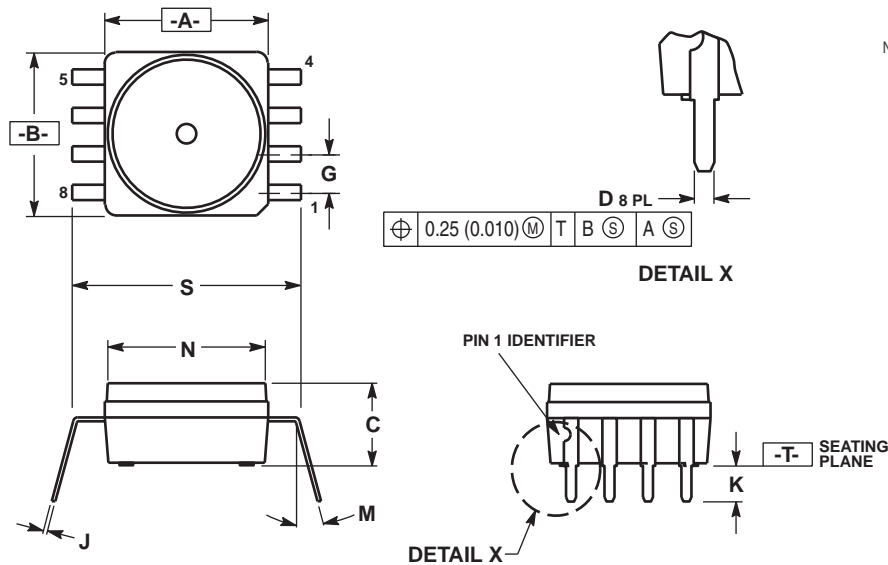
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
  5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.500	0.520	12.70	13.21
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
H	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0°	7°	0°	7°
N	0.444	0.448	11.28	11.38
S	0.709	0.725	18.01	18.41
V	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

**CASE 482A-0  
ISSUE A  
SMALL OUTLINE PACKAGE**



# PACKAGE DIMENSIONS

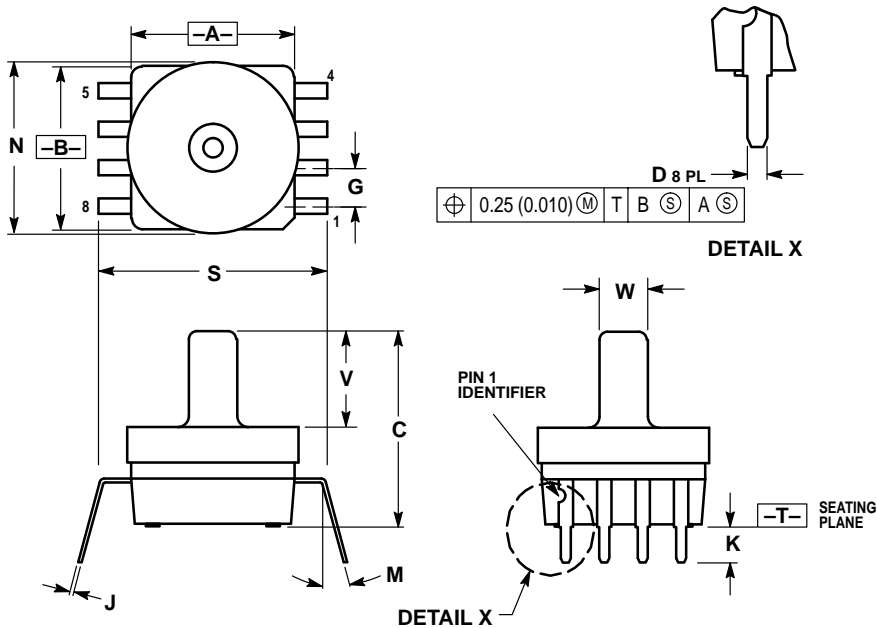


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.210	0.220	5.33	5.59
D	0.026	0.034	0.66	0.864
G	0.100 BSC		2.54 BSC	
J	0.009	0.011	0.23	0.28
K	0.100	0.120	2.54	3.05
M	0°	15°	0°	15°
N	0.405	0.415	10.29	10.54
S	0.540	0.560	13.72	14.22

**CASE 482B-03  
ISSUE B  
SMALL OUTLINE PACKAGE**



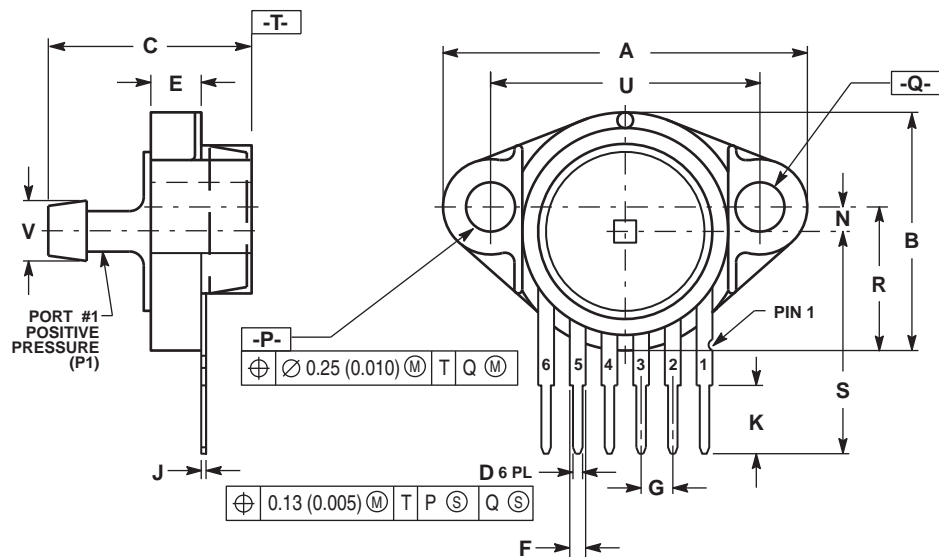
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.500	0.520	12.70	13.21
D	0.026	0.034	0.66	0.864
G	0.100 BSC		2.54 BSC	
J	0.009	0.011	0.23	0.28
K	0.100	0.120	2.54	3.05
M	0°	15°	0°	15°
N	0.444	0.448	11.28	11.38
S	0.540	0.560	13.72	14.22
V	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

**CASE 482C-03  
ISSUE B  
SMALL OUTLINE PACKAGE**

# PACKAGE DIMENSIONS



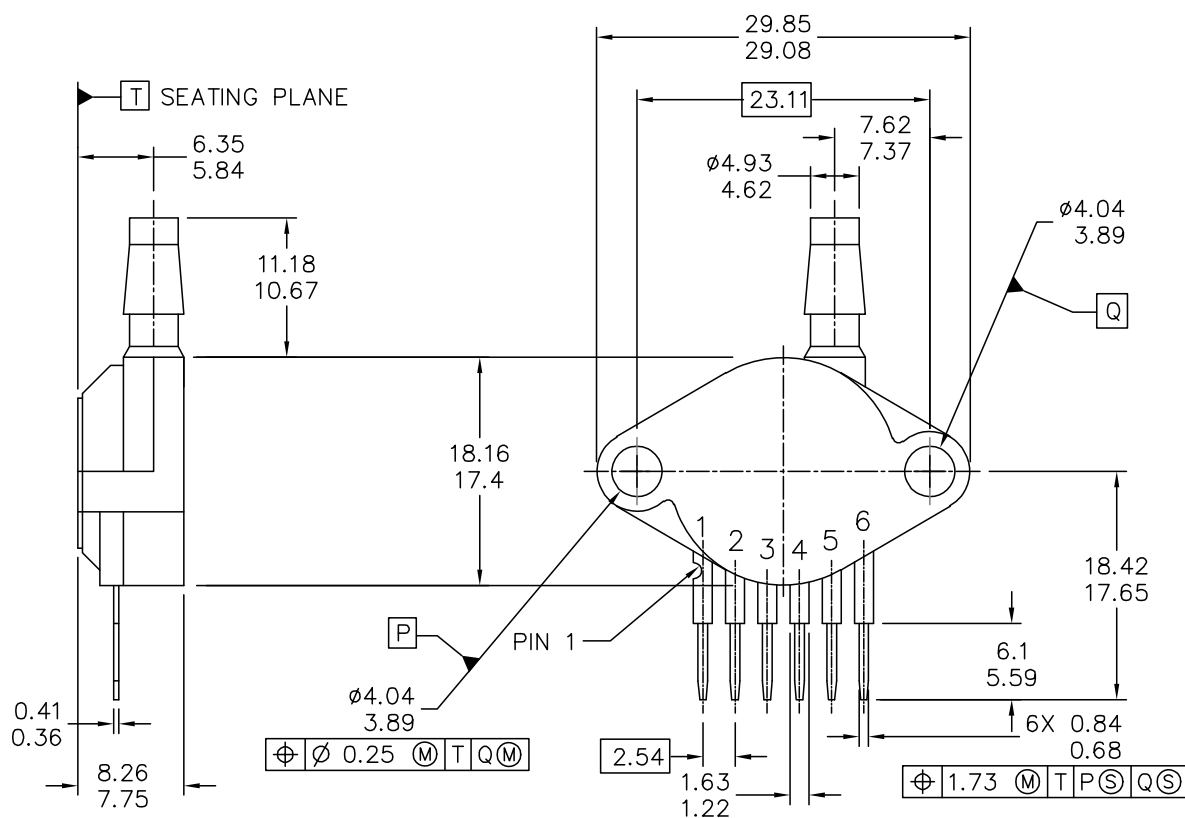
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.080	1.120	27.43	28.45
B	0.740	0.760	18.80	19.30
C	0.630	0.650	16.00	16.51
D	0.027	0.033	0.68	0.84
E	0.160	0.180	4.06	4.57
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.220	0.240	5.59	6.10
N	0.070	0.080	1.78	2.03
P	0.150	0.160	3.81	4.06
Q	0.150	0.160	3.81	4.06
R	0.440	0.460	11.18	11.68
S	0.695	0.725	17.65	18.42
U	0.840	0.860	21.34	21.84
V	0.182	0.194	4.62	4.93

STYLE 1:  
 PIN 1: V<sub>OUT</sub>  
 2: GROUND  
 3: V<sub>CC</sub>  
 4: V<sub>1</sub>  
 5: V<sub>2</sub>  
 6: V<sub>EX</sub>

**CASE 867F-03  
 ISSUE D  
 UNIBODY PACKAGE**

## PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE:  SENSOR, 6 LEAD UNIBODY CELL, AP & GP 01ASB09087B		DOCUMENT NO: 98ASB42796B		REV: G	
		CASE NUMBER: 867B-04		28 JUL 2005	
		STANDARD: NON-JEDEC			

PAGE 1 OF 2

**CASE 867B-04  
ISSUE G  
UNIBODY PACKAGE**



**PACKAGE DIMENSIONS**

NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- 3. 867B-01 THRU -3 OBSOLETE, NEW STANDARD 867B-04.

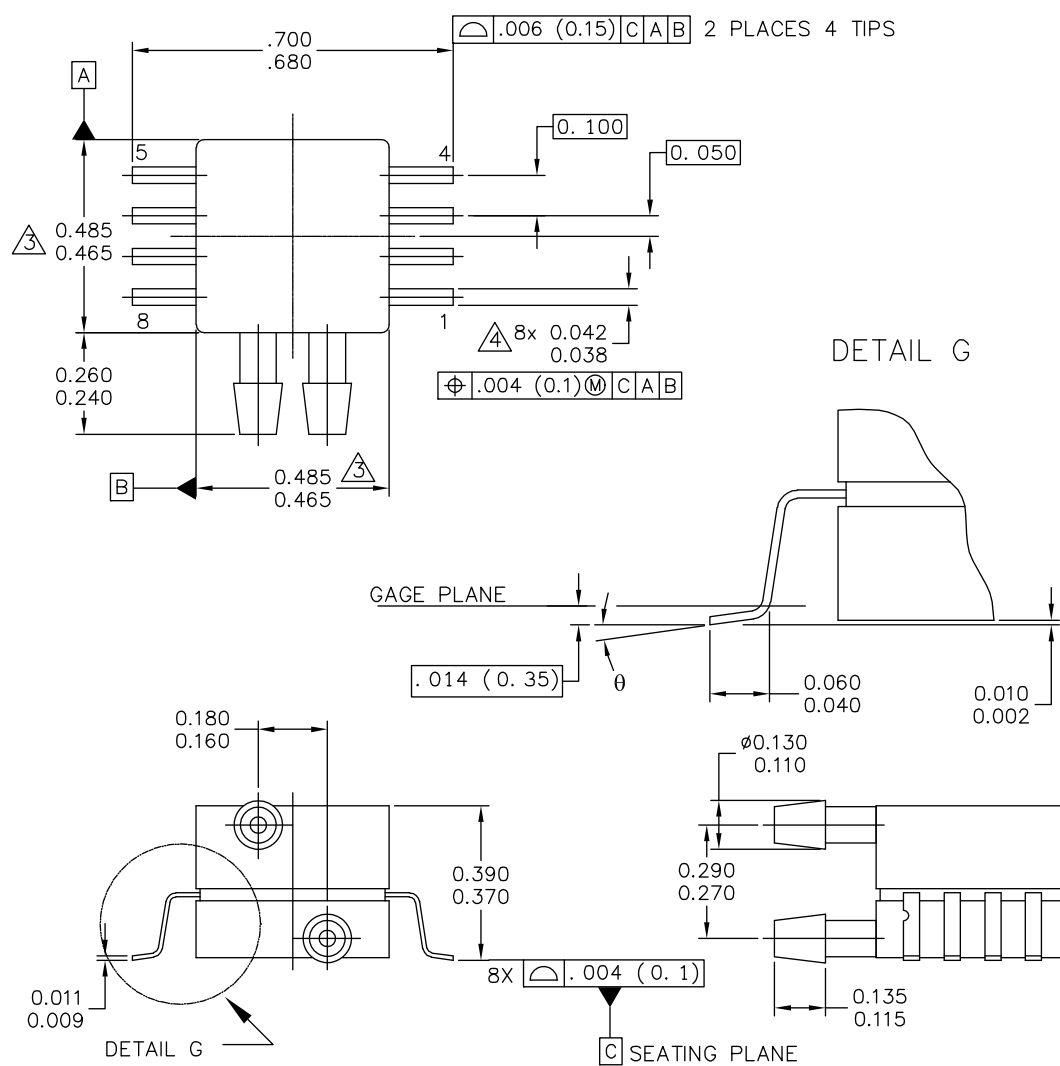
STYLE 1:

- PIN 1: V OUT
- 2: GROUND
- 3: VCC
- 4: V1
- 5: V2
- 6: V EX

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: SENSOR, 6 LEAD UNIBODY CELL, AP & GP 01ASB09087B	DOCUMENT NO: 98ASB42796B		REV: G
	CASE NUMBER: 867B-04		28 JUL 2005
	STANDARD: NON-JEDEC		

**CASE 867B-04  
ISSUE G  
UNIBODY PACKAGE**

## PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		<b>MECHANICAL OUTLINE</b>		PRINT VERSION NOT TO SCALE	
TITLE:  8 LD SNSR, DUAL PORT		DOCUMENT NO: 98ASA99255D		REV: A	
		CASE NUMBER: 1351-01		27 JUL 2005	
		STANDARD: NON-JEDEC			

PAGE 1 OF 2

**CASE 1351-01**  
**ISSUE A**  
**SMALL OUTLINE PACKAGE**

**MPX5010**

## PACKAGE DIMENSIONS

### NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.

4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR  
PROTRUSION SHALL BE .008 MAXIMUM.

#### STYLE 1:

PIN 1: GND  
PIN 2: +Vout  
PIN 3: Vs  
PIN 4: -Vout  
PIN 5: N/C  
PIN 6: N/C  
PIN 7: N/C  
PIN 8: N/C

#### STYLE 2:

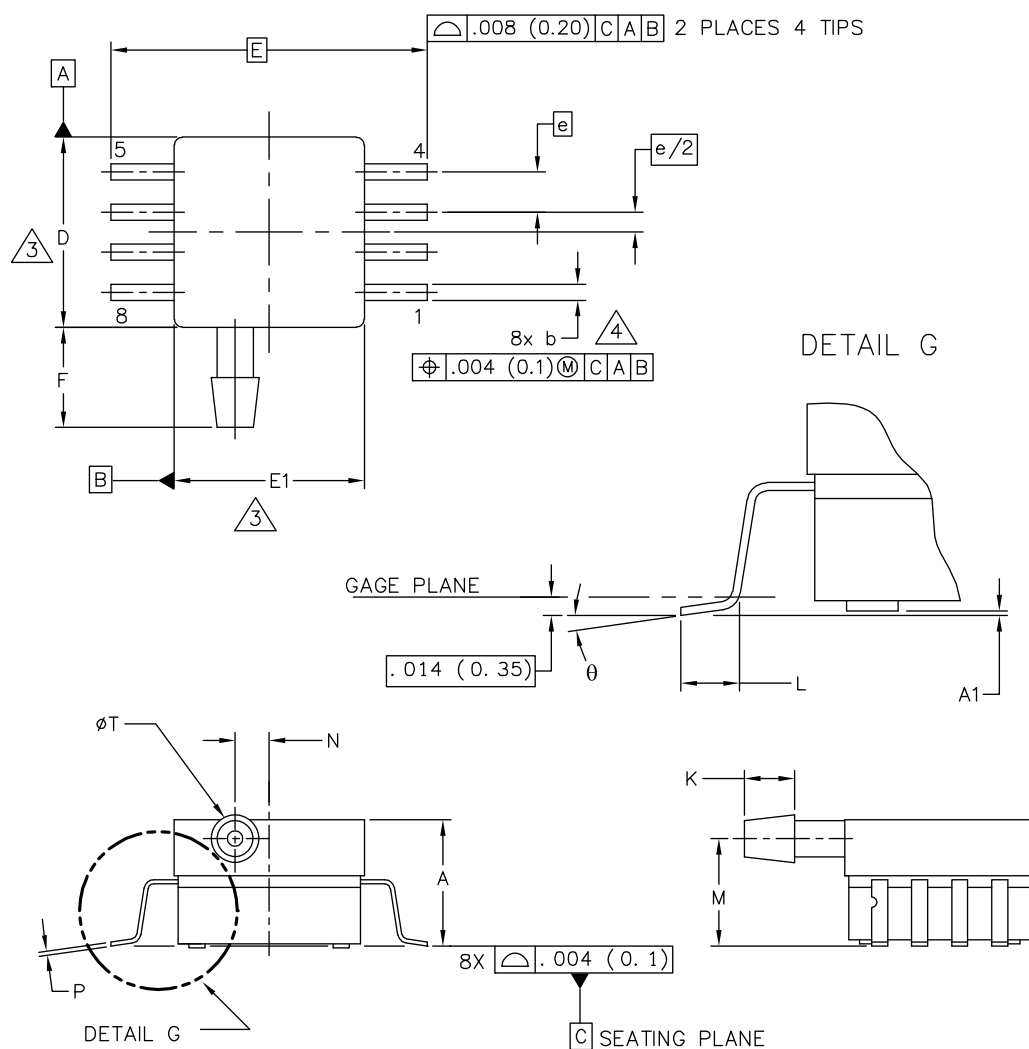
PIN 1: N/C  
PIN 2: Vs  
PIN 3: GND  
PIN 4: Vout  
PIN 5: N/C  
PIN 6: N/C  
PIN 7: N/C  
PIN 8: N/C

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TITLE:  8 LD SNSR, DUAL PORT		DOCUMENT NO: 98ASA99255D		REV: A	
		CASE NUMBER: 1351-01		27 JUL 2005	
		STANDARD: NON-JEDEC			

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**CASE 1351-01  
ISSUE A  
SMALL OUTLINE PACKAGE**

## PACKAGE DIMENSIONS



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TITLE:  8 LD SOP, SIDE PORT		DOCUMENT NO: 98ASA99303D		REV: B	
		CASE NUMBER: 1369-01		24 MAY 2005	
		STANDARD: NON-JEDEC			

PAGE 1 OF 2

**CASE 1369-01  
ISSUE B  
SMALL OUTLINE PACKAGE**

# PACKAGE DIMENSIONS

## NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

③ DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.

④ DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

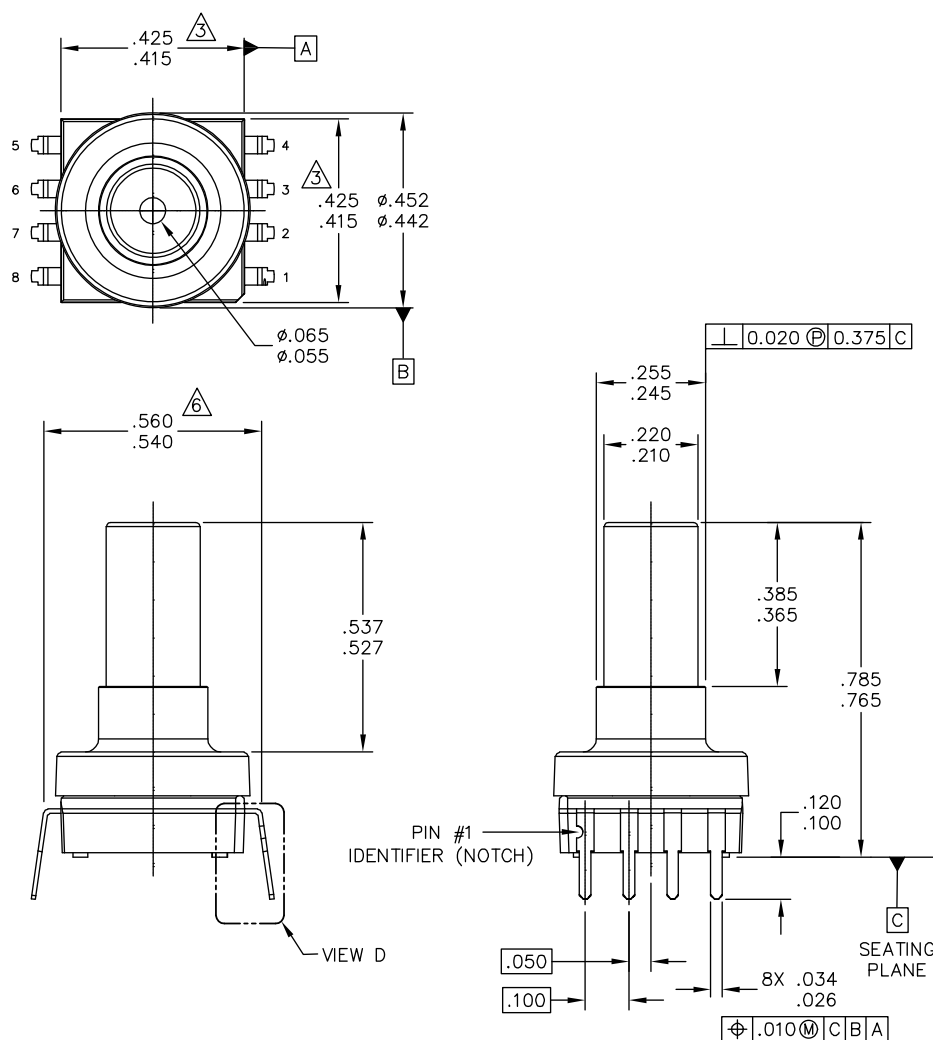
DIM	INCHES		MILLIMETERS		DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.300	.330	7.11	7.62	θ	0°	7°	0°	7°
A1	.002	.010	0.05	0.25	—	---	---	---	---
b	.038	.042	0.96	1.07	—	---	---	---	---
D	.465	.485	11.81	12.32	—	---	---	---	---
E	.717 BSC		18.21 BSC		—	---	---	---	---
E1	.465	.485	11.81	12.32	—	---	---	---	---
e	.100 BSC		2.54 BSC		—	---	---	---	---
F	.245	.255	6.22	6.47	—	---	---	---	---
K	.120	.130	3.05	3.30	—	---	---	---	---
L	.061	.071	1.55	1.80	—	---	---	---	---
M	.270	.290	6.86	7.36	—	---	---	---	---
N	.080	.090	2.03	2.28	—	---	---	---	---
P	.009	.011	0.23	0.28	—	---	---	---	---
T	.115	.125	2.92	3.17	—	---	---	---	---
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TITLE:  8 LD SOP, SIDE PORT					DOCUMENT NO: 98ASA99303D			REV: B	
					CASE NUMBER: 1369-01			24 MAY 2005	
					STANDARD: NON-JEDEC				

PAGE 2 OF 2

**CASE 1369-01  
ISSUE B  
SMALL OUTLINE PACKAGE**



## PACKAGE DIMENSIONS

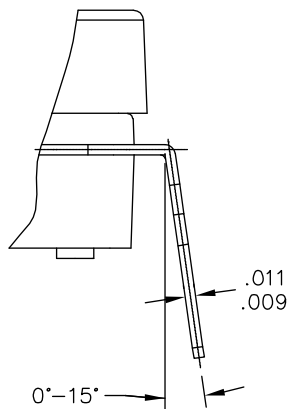


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TITLE:  SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH		DOCUMENT NO: 98ASA10611D		REV: D	
		CASE NUMBER: 1560-03		25 FEB 2009	
		STANDARD: NON-JEDEC			

PAGE 1 OF 3

**1560-03  
ISSUE C  
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS



VIEW D

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TITLE:  SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10611D		REV: D	
	CASE NUMBER: 1560-03		25 FEB 2009	
	STANDARD: NON-JEDEC			

**CASE 1560-03  
ISSUE D  
SMALL OUTLINE PACKAGE**

# PACKAGE DIMENSIONS

## NOTES:

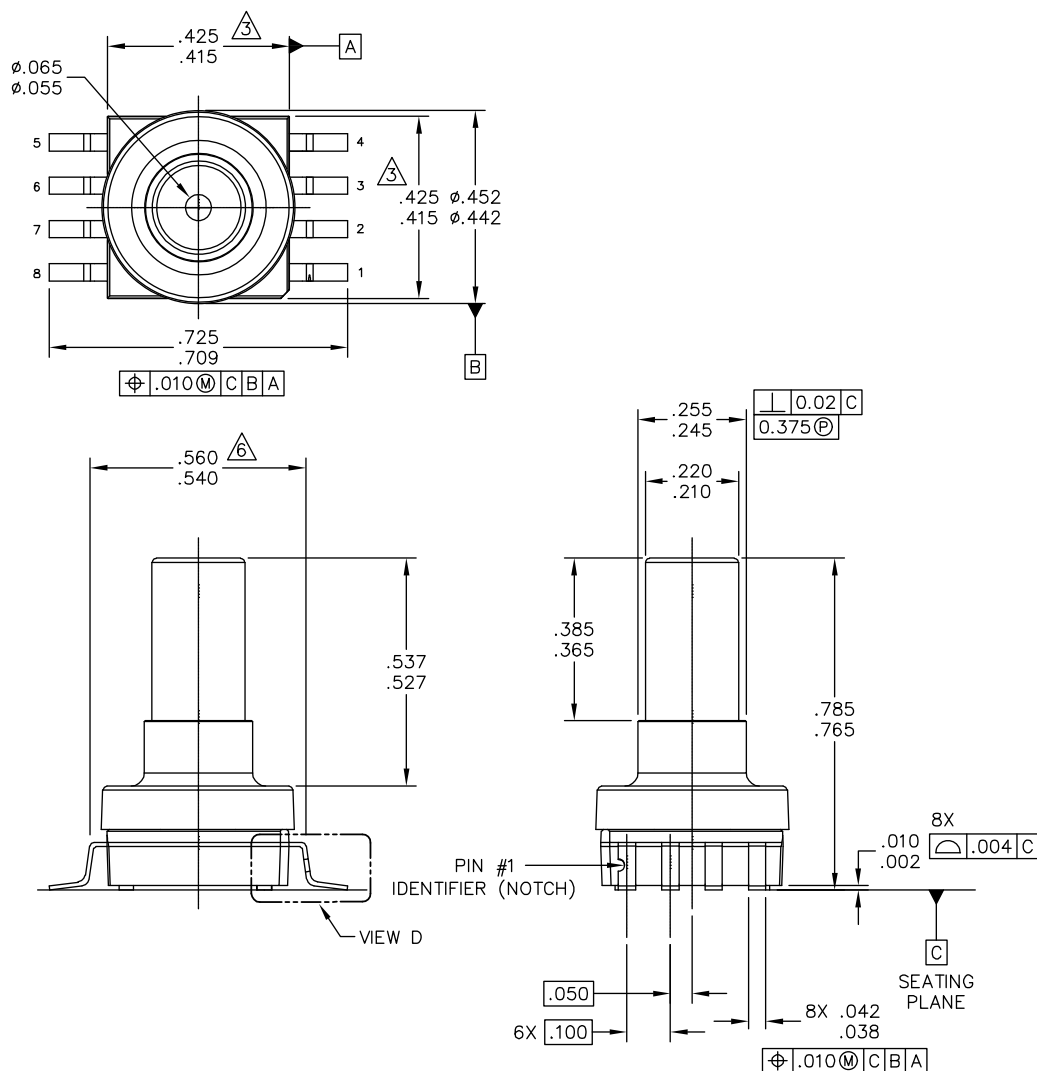
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION IS .006.
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

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TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10611D		REV: D
	CASE NUMBER: 1560-03		25 FEB 2009
	STANDARD: NON-JEDEC		

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**CASE 1560-03**  
**ISSUE D**  
**SMALL OUTLINE PACKAGE**

## PACKAGE DIMENSIONS

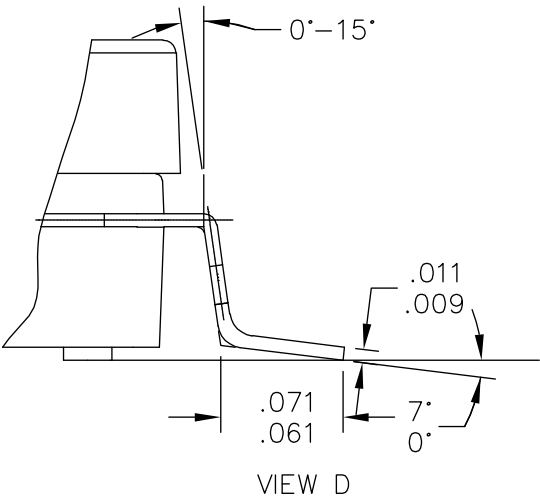


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TITLE:  SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10686D		REV: B	
	CASE NUMBER: 1735-02		19 FEB 2009	
	STANDARD: NON-JEDEC			

PAGE 1 OF 3

**CASE 1735-02  
ISSUE B  
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS



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TITLE:  SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH		DOCUMENT NO: 98ASA10686D		REV: B	
		CASE NUMBER: 1735-02		19 FEB 2009	
		STANDARD: NON-JEDEC			

CASE 1735-02  
ISSUE B  
SMALL OUTLINE PACKAGE

**PACKAGE DIMENSIONS**

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION IS .006.
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

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TITLE:  SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10686D		REV: B	
	CASE NUMBER: 1735-02		19 FEB 2009	
	STANDARD: NON-JEDEC			

PAGE 3 OF 3

**CASE 1735-02  
ISSUE B  
SMALL OUTLINE PACKAGE**

**Table 3. Revision History**

Revision number	Revision date	Description of changes
13	10/2012	<ul style="list-style-type: none"> <li>Deleted references to device number MPVZ5010G6T1, MPVZ5010G6U/T1 and MPVZ5010G6U/6T1 throughout the document</li> </ul>

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