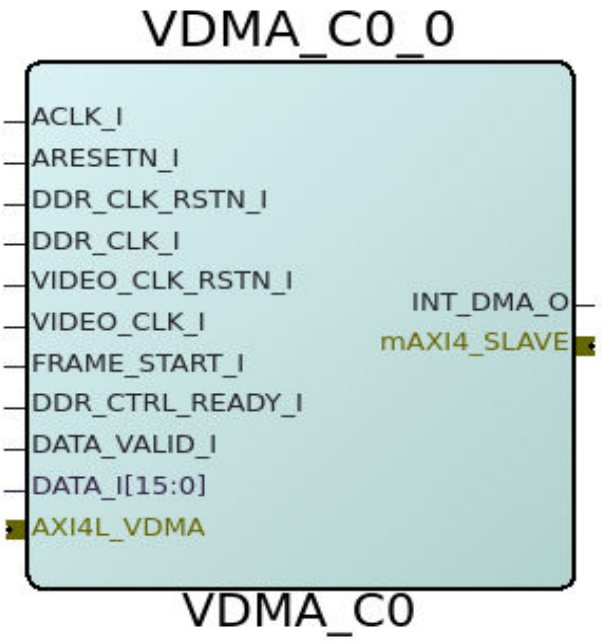
Introduction (Ask a Question)

In the video applications space, it is required to write a continuous stream of incoming data (frames) from sources such as a video camera to memory. Video Direct Memory Access (VDMA) IP attempts to address the need for writing a continuous burst of data to DDR memory.

There are control registers that need to be configured within the IP. These registers are configured through AXI4 Lite interface.

The following figure shows the VDMA input and output ports.

Figure 1. VDMA Input Output Ports



Summary

The following table provides a summary of the Video DMA IP characteristics.

Table 1. Video DMA IP Characteristics

Core Version	This document applies to Video DMA IP v1.1
Supported Device Families	The Video DMA IP supports the following families: • PolarFire® SoC • PolarFire • RTG4™ • IGLOO® 2 • SmartFusion® 2
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases
Licensing	No RTL license is required for this IP and clear RTL is available.

Features

The Video DMA IP has the following key features:

- 32-bit addressing for the AXI4 Lite Interface
- 38-bit addressing for the AXI4 Interface to DDR
- Configurable Input Data Bus Width to 8-bit, 16-bit, and 32-bit
- Fixed Output Data Bus Width of 64-bit
- Supports Interrupt generation
- 32-bit Programmable Buffer Address to write the frames to DDR
- Supports Multiple Resolution (example: 640 × 360, 1280 × 720, 1920 × 1080)
- Frame Size for every written frame Available

Installation Instructions

The IP core must be installed to the IP Catalog of Libero® SoC software automatically through the IP Catalog update function in Libero SoC software, or it is manually downloaded from the catalog. Once the IP core is installed in Libero SoC software IP Catalog, it is configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Table of Contents

1. Description (Ask a Question)

A video source generates a continuous stream of data which needs to be written to the DDR memory as video frames. The memory location for the frame buffers is configured through the control registers. For each processed frame, VDMA presents the frame size in the corresponding control register.

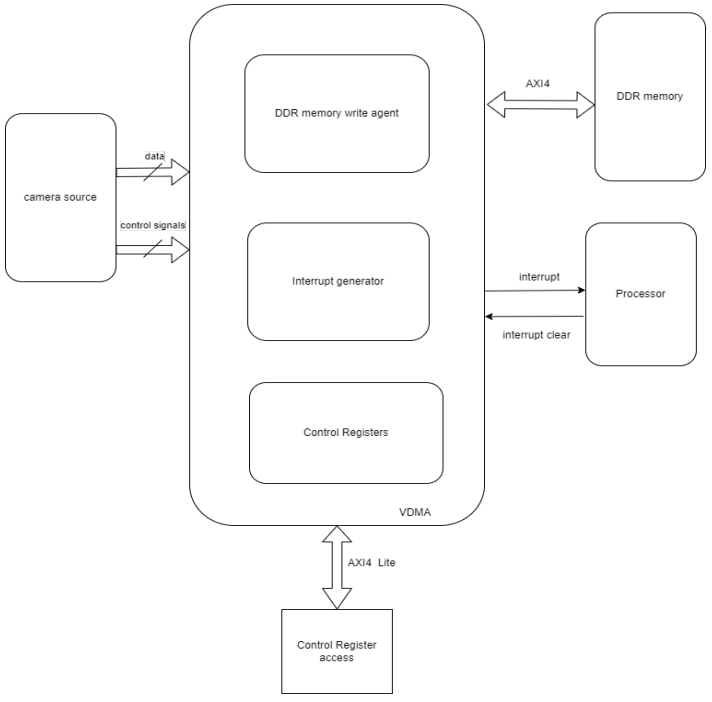
DDR memory requires 38-bit addressing. The processor provides for the 32-bit address to which the video frame has to be written. The VDMA appends all 0s to the lower 6 bits of the required 38-bit address, that is, 38-bit address = "MSB 32-bit address provided by the processor" + "LSB 6 bits are 0". Multiple buffer addresses are provided and stored in VDMA. Maximum number of pending buffer addresses within VDMA is 32, at any given instance.

The DDR memory write agent is responsible to collect the video data from camera and write these as frame data to the DDR memory. It uses AXI4 interface to access the DDR memory. VDMA has internal buffers which store the incoming data before writing it to DDR through the AXI4 interface.

The global interrupt register needs to be set to use the interrupt feature of the VDMA IP. When enabled, the required interrupts are enabled as seen from the control register map. For all the enabled interrupts, processor receives interrupt onto a single line. For example, when the end of frame interrupt is enabled, for every frame written to the DDR memory an interrupt is generated. This interrupt line to the processor is held high till the processor clears it through the interrupt status control register. Hence, the processor is notified whenever the frame is available for processing. An event may take place wherein, while the processor is clearing the interrupt, another interrupt event occurs. In such scenarios, VDMA IP raises the interrupt line high immediately after the processor clears the first interrupt. The processor identifies the source of the interrupt from the interrupt status control register. The same register is used to clear the interrupt as well.

The following figure shows the DMA architecture block diagram.

Figure 1-1. DMA Architecture Block Diagram



2. Configuration Settings (Ask a Question)

User can select 8, 16, and 32-bit Input Data Width for the Video DMA IP.

3. Inputs and Output Signals (Ask a Question)

The following table lists the Video DMA IP input and output signals.

Table 3-1. Input and Output Signal Description

Signal name	Direction	Width	Description
ACLK_I	Input	1	AXI4 Lite interface clock
ARESETN_I	Input	1	AXI4 Lite interface reset signal
DDR_CLK_I	Input	1	DDR clock for writing
DDR_CLK_RSTN_I	Input	1	DDR clock reset signal
VIDEO_SOURCE_CLK_I	Input	1	Video clock for data input
VIDEO_SOURCE_CLK_RSTN_I	Input	1	Video clock reset signal
DDR_CTRL_READY_I	Input	1	DDR controller ready signal to indicate that DDR memory is ready to accept commands from the VDMA IP
FRAME_START_I	Input	1	Indicates a start of frame for the camera data input
DATA_VALID_I	Input	1	Indicates that a valid data is available on the data bus
DATA_I	Input	8, 16, and 32	Camera data which has to be written to DDR memory
AXI4L_VDMA	Input	AXI4 Lite interface	AXI4 Lite interface to access control registers of the VDMA IP
INT_DMA_O	Output	1	This signal is held high till an interrupt clear signal is received. It will be generated for every frame data written to the DDR memory.
mAXI4_SLAVE	Output	AXI4 interface	This mirrored AXI4 slave interface is connected to the DDR memory for the frames to be written

4. Design Specifications (Ask a Question)

The following table lists the design specifications of the VDMA IP.

Table 4-1. Design Specification and Parameter

Sr num	Design parameter	Value
1	Buffer address FIFO	WIDTH: 32 DEPTH: 32
2	Frame size FIFO	WIDTH: 32 DEPTH: 32

5. Register Summary and Maps (Ask a Question)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	IP_VER	7:0	IP VERSION[7:0]							
		15:8	IP VERSION[15:8]							
		23:16	IP VERSION[23:16]							
		31:24								
0x04	Control_Register	7:0						FIFO RESET	IP RESET	ENABLE/ DISABLE
		15:8								
		23:16								
		31:24								
0x08	GLBL_INT_EN	7:0								GLOBAL INTERRUPT ENABLE
		15:8								
		23:16								
		31:24								
0x0C	Interrupt_Status	7:0				FRAME SIZE FIFO EMPTY	FRAME SIZE FIFO FULL	BUFFER ADDRESS FIFO EMPTY	BUFFER ADDRESS FIFO FULL	END OF FRAME INTERRUPT
		15:8								
		23:16								
		31:24								
0x10	Interrupt_Enable	7:0				FRAME SIZE FIFO EMPTY	FRAME SIZE FIFO FULL	BUFFER ADDRESS FIFO EMPTY	BUFFER ADDRESS FIFO FULL	END OF FRAME INTERRUPT
		15:8								
		23:16								
		31:24								
0x14 ... 0x1B	Reserved									
0x1C	Buffer_Address_FIFO	7:0	BUFFER ADDRESS FIFO[7:0]							
		15:8	BUFFER ADDRESS FIFO[15:8]							
		23:16	BUFFER ADDRESS FIFO[23:16]							
		31:24	BUFFER ADDRESS FIFO[31:24]							
0x20 ... 0x23	Reserved									
0x24	Frame_Size_FIFO	7:0	FRAME SIZE FIFO[7:0]							
		15:8	FRAME SIZE FIFO[15:8]							
		23:16	FRAME SIZE FIFO[23:16]							
		31:24	FRAME SIZE FIFO[31:24]							

5.1 IP Version (Ask a Question)

Name: IP_VER
Offset: 0x000
Reset: 0x10100
Property: Read-only

Current Video DMA IP version number

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	IP VERSION[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	1

Bit	15	14	13	12	11	10	9	8
	IP VERSION[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
	IP VERSION[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – IP VERSION[23:0] Current Video DMA IP version number

5.2 Control Register (Ask a Question)

Name: Control_Register
Offset: 0x004
Reset: 0x1
Property: Read/Write

Register to Enable/Disable/Reset the Video DMA IP

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						FIFO RESET	IP RESET	ENABLE/ DISABLE
Access						W	W	R/W
Reset						0	0	1

Bit 2 – FIFO RESET Writing a value of '1' flushes all the FIFOs within the Video DMA IP core. It does not hold the written value, that is, writes are combinatorial in nature

Bit 1 – IP RESET Writing a value of '1' resets the IP core and flushes all the FIFOs within the Video DMA IP core. It does not hold the written value, that is, writes are combinatorial in nature.

Bit 0 – ENABLE/DISABLE This setting manages the activation and deactivation of the IP. Setting it to '1' will enable the IP, while setting it to '0' will disable it.

5.3 Enable Global Interrupt (Ask a Question)

Name: GLBL_INT_EN
Offset: 0x008
Reset: 0x0
Property: Read/Write

Global Interrupt Enable

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								GLOBAL INTERRUPT ENABLE
Access								R/W
Reset								0

Bit 0 – GLOBAL INTERRUPT ENABLE Enables the interrupts globally at Video DMA IP level.

5.4 Interrupt Status (Ask a Question)

Name: Interrupt_Status
Offset: 0x00C
Reset: 0x0
Property: Read/Write

Interrupt Status Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				FRAME SIZE FIFO EMPTY	FRAME SIZE FIFO FULL	BUFFER ADDRESS FIFO EMPTY	BUFFER ADDRESS FIFO FULL	END OF FRAME INTERRUPT
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – FRAME SIZE FIFO EMPTY When enabled, it indicates to the processor that the frame size FIFO is getting empty. Writing a value of '1' will clear this interrupt.

Bit 3 – FRAME SIZE FIFO FULL When enabled, it indicates to the processor that the frame size FIFO is in full condition. Writing a value of '1' will clear this interrupt.

Bit 2 – BUFFER ADDRESS FIFO EMPTY When enabled, buffer address FIFO empty interrupt will be generated, when the Video DMA IP has processed all the buffer addresses provided by the processor. Writing a value of '1' will clear this interrupt.

Bit 1 – BUFFER ADDRESS FIFO FULL When enabled, buffer address FIFO full interrupt will be generated when the Video DMA IP is unable to accept any more buffer addresses from the processor, indicating that the FIFO is in full condition. Writing a value of '1' will clear this interrupt.

Bit 0 – END OF FRAME INTERRUPT When enabled, End Of Frame interrupt is generated after every frame is written to the memory. This frame is written to the buffer address provided by the processor. Reading a value of '1' in this register indicates that the Frame End interrupt event has occurred. Writing a value of '0' clears the interrupt.

5.5 Enable Interrupt (Ask a Question)

Name: Interrupt_Enable
Offset: 0x010
Reset: 0x0
Property: Read/Write

Interrupt Enable Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				FRAME SIZE FIFO EMPTY	FRAME SIZE FIFO FULL	BUFFER ADDRESS FIFO EMPTY	BUFFER ADDRESS FIFO FULL	END OF FRAME INTERRUPT
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – FRAME SIZE FIFO EMPTY Writing a value of '1' enables the interrupt generation for frame size FIFO empty condition.

Bit 3 – FRAME SIZE FIFO FULL Writing a value of '1' enables the interrupt generation for frame size FIFO full condition.

Bit 2 – BUFFER ADDRESS FIFO EMPTY Writing a value of '1' enables the interrupt generation for buffer address FIFO empty condition.

Bit 1 – BUFFER ADDRESS FIFO FULL Writing a value of '1' enables the interrupt generation for buffer address FIFO full condition.

Bit 0 – END OF FRAME INTERRUPT Writing a value of '1' enables the Frame End interrupt. The interrupt will be generated for every frame getting written to the memory.

5.6 FIFO Buffer Address (Ask a Question)

Name: Buffer_Address_FIFO
Offset: 0x01C
Reset: 0x0
Property: Write-only

Buffer address provided by the external agent, like processor, should be written to this address register.

Bit	31	30	29	28	27	26	25	24
	BUFFER ADDRESS FIFO[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BUFFER ADDRESS FIFO[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	BUFFER ADDRESS FIFO[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUFFER ADDRESS FIFO[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – BUFFER ADDRESS FIFO[31:0] The buffer address, to which the frame should be written, is programmed by the external agency into this control register. The provided 32-bit address is internally converted to 38-bit address, as shown below. This 38-bit address is used by the FIC interface to access the DDR memory, by the MSS processor.

Value	Description
MSS 37:6 address	32-bit address programmed into the buffer address FIFO
MSS 5:0 address	Lower 6 bits are hard coded to the value of 0

5.7 FIFO Frame Size (Ask a Question)

Name: Frame_Size_FIFO
Offset: 0x024
Reset: 0x0
Property: Read-only

Size of the frame which was written to the DDR memory

Bit	31	30	29	28	27	26	25	24
	FRAME SIZE FIFO[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	FRAME SIZE FIFO[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FRAME SIZE FIFO[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FRAME SIZE FIFO[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

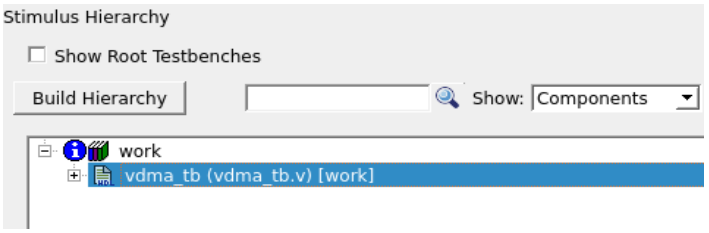
Bits 31:0 – FRAME SIZE FIFO[31:0] Frame size, which is written to the DDR memory, can be read from this control register. This register should be read after receiving the End Of Frame interrupt, which indicates a valid memory write operation.

6. Testbench Simulation (Ask a Question)

A sample testbench is provided to simulate the VDMA IP core. To simulate the testbench, perform the following steps:

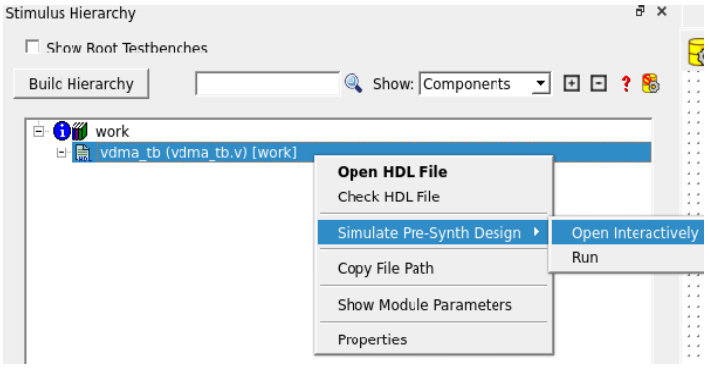
1. In Libero SoC tool, click **View** > **Windows** > **IP Catalog** and search for **VDMA** entry.
2. To configure the IP, double-click **VDMA** and click **OK**.
3. Navigate to **Stimulus Hierarchy** and click **Build Hierarchy**, as shown in the following figure.

Figure 6-1. Stimulus Hierarchy



4. To run the testbench in interactive mode, navigate to the **Stimulus Hierarchy** tab, right-click **vdma_tb** > **Simulate Pre-Synth Design** > **Open Interactively**. The IP gets simulated for a single frame with 320 × 240 resolution, as shown in the following figure.

Figure 6-2. Pre-Synth Design Simulation



The testbench runs and the simulator waveforms are added to view the data transfer from the video source to the VDMA IP, as shown in the following figures.

Figure 6-3. Testbench Transcript

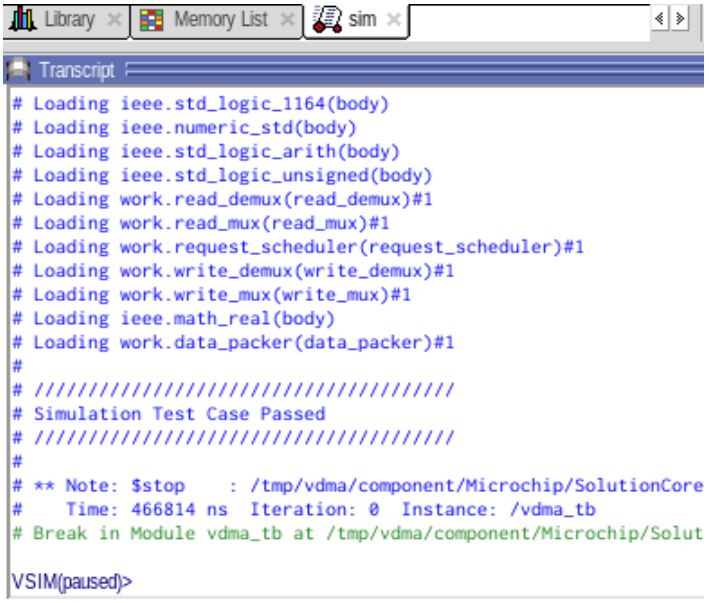
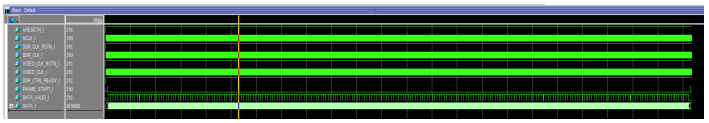


Figure 6-4. Model Sim Tool Window



Important: If the simulation is interrupted due to the runtime limit specified in the `.do` file, use the `run -all` command to complete the simulation.

7. Resource Utilization (Ask a Question)

The following table lists the resource utilization of VDMA IP design made for PolarFire® SoC.

Table 7-1. Resource Utilization of VDMA IP for 8-bit Data Input Configuration

Family	Device	Fabric 4LUT	Fabric DFF	Interface 4LUT	Interface DFF	uSRAM	LSRAM	Chip Global
PolarFire® SoC	MPFS250TS	1052	1093	624	321	1	17	3

8. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 8-1. Revision History

Revision	Date	Description
B	05/2024	Added Register Maps, see: 5. Register Summary and Maps.
A	02/2024	Initial Release

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