Organization of Digital Computer Lab
EECS112L/CSE 132L

Final Project
Pipeline MIPS

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March 13, 2016

1 Description

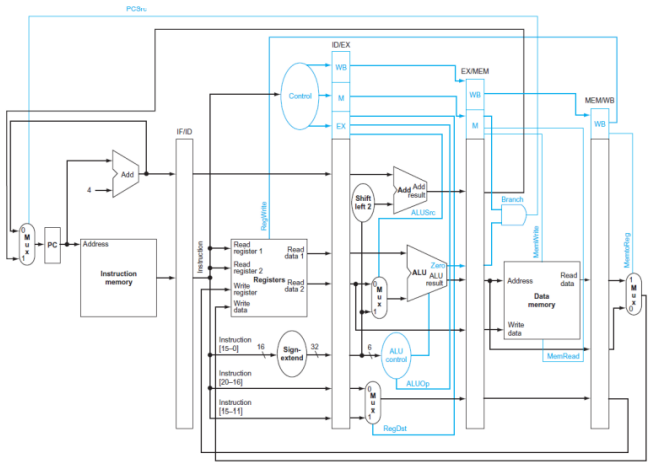
In this lab, we extended the functionality of our previous single-cycle MIPS processor to support pipelining. In this version, our processor takes in two inputs, clock and reset, and is able to execute all R-type and I-type instructions, jump, jump and link, and branch on equal. The components of our processor include adders, multiplexers, a control unit, an ALU-control unit, an instruction memory, a program counter, sign extenders, ALU, register file, and data memory. For this lab, we designed four new registers to enable the pipeline stages and also a hazard unit to control forwarding. Furthermore, the data paths of the processor were updated in order to implement pipelining and hazard detection.

2 Input/Output Port Description

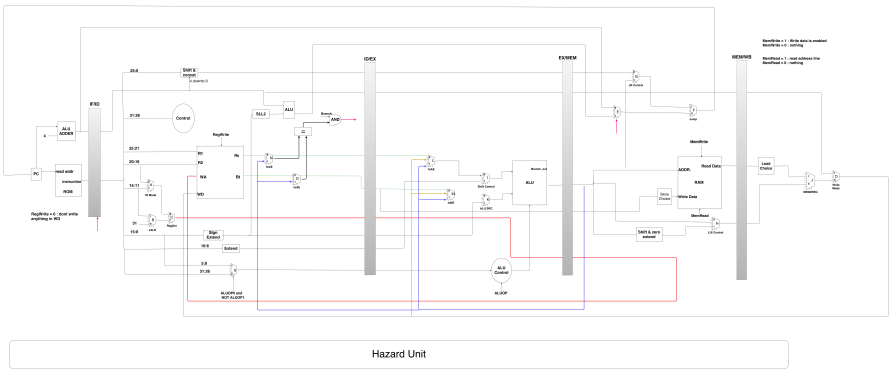
Port Name	Port Size	Port Type	Description
ref_clk	1	IN	processor clock
reset	1	IN	processor reset

3 Design Schematic

3.1 Book Schematic



3.2 Team Schematic



4 Simulation

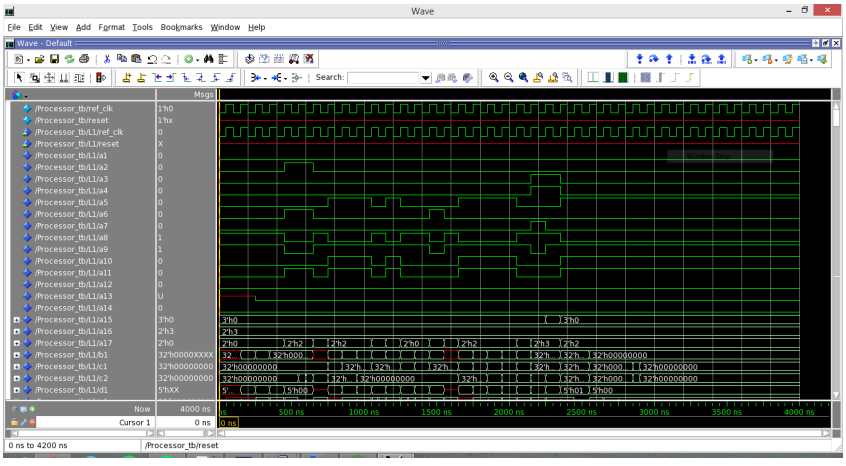
To test our design, we implemented a testbench using SystemVerilog and simulated the design using Questasim. Since the only ports of the processor are the clock and reset, the testbench only supplies the processor with the those inputs. To ensure correct functionality, we wrote our own test program in the *imem.h* file to store it into the instruction memory for the processor to run. Next we ran the simulation and inspected the inputs and outputs of each component and the values in the registers in the simulation waveforms.

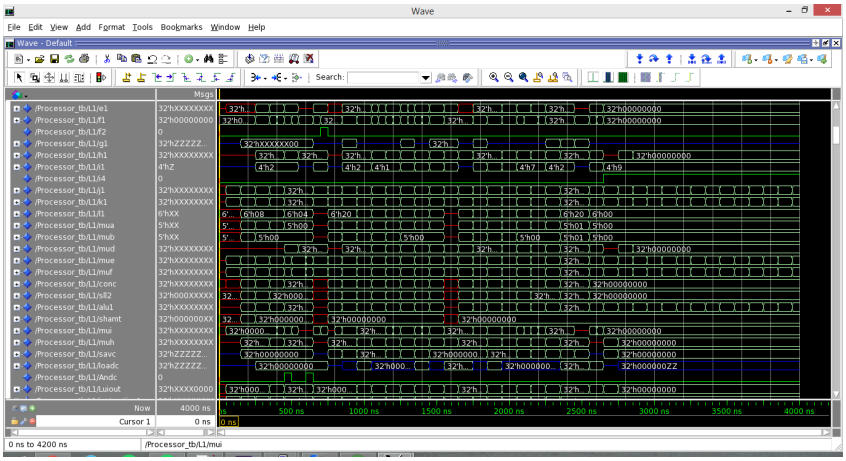
4.1 Test Program

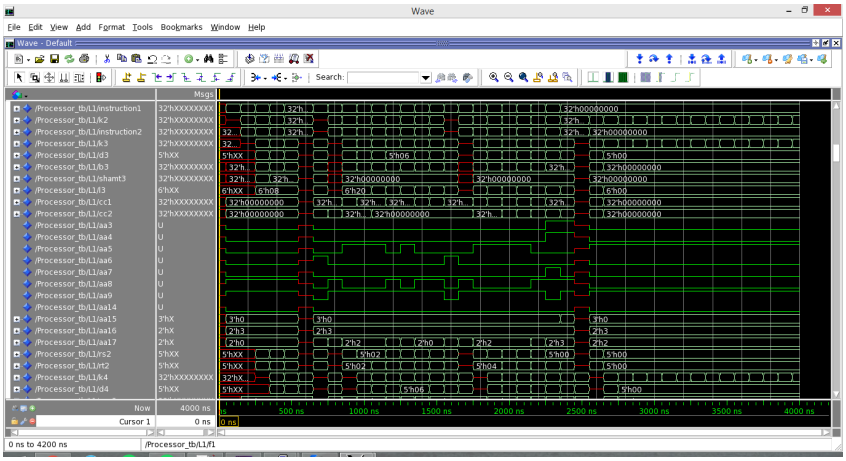
The program below, which we used to test our processor, implements a sequence of logic and arithmetic operations and then checks the resulting values in the registers to determine whether or not to perform a branch operation. The unconditional branch and load and store operations are also implemented. The instructions are written in hexadecimal, binary, and assembly with comments on the side for readability and comprehensive purposes.

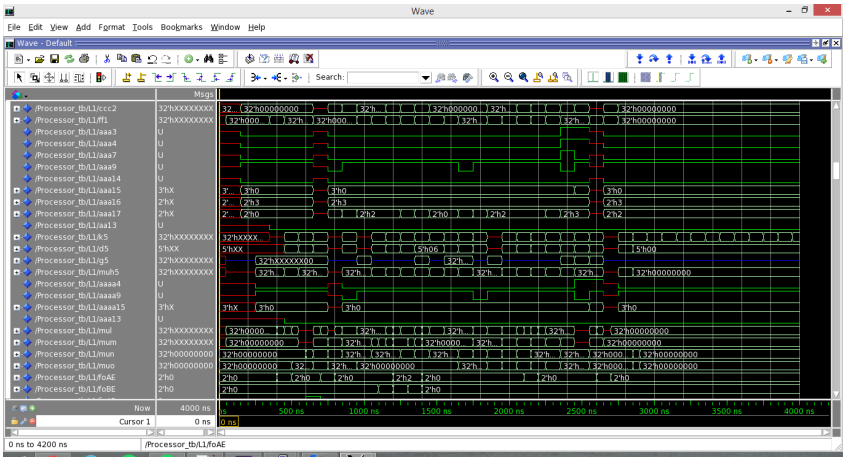
```
2001fffc        001000 00000 00001 1111111111111100     addi    r1, r0, -4              r1 = -4
20220006        001000 00001 00010 0000000000000110     addi    r2, r1, 6               r2 = 2
200f0002        001000 00000 01111 0000000000000010     addi    r15, r0, 2              r15 = 2
11e20002        000100 01111 00010 0000000000000010     beq     r2, r15, [2]            skip to add r3, r1, r2
-------------------------------------------------------------------------------------------------------------------
20100003        001000 00000 10000 0000000000000011     addi    r16, r0, -4             r16 = 3   SKIPPED BY BRANCH
2011000a        001000 00000 10001 0000000000001010     addi    r17, r0, 10             r17 = 10   SKIPPED BY BRANCH
-------------------------------------------------------------------------------------------------------------------
00221820        000000 00001 00010 00011 00000 100000   add     r3, r1, r2              r3 = -2
00422020        000000 00010 00010 00100 00000 100000   add     r4, r2, r2              r4 = 4
00442825        000000 00010 00100 00101 00000 100101   or      r5, r4, r2              r5 = 6
34a6000a        001101 00101 00110 0000000000001010     ori     r6, r5, 10              r6 = 14
00c53022        000000 00110 00101 00110 00000 100010   sub     r6, r6, r5              r6 = 8
20470009        001000 00010 00111 0000000000001001     addi    r7, r2, 9               r7 = 11
30a8000a        001100 00101 01000 0000000000001010     andi    r8, r5, 10              r8 = 2
8000011         000010 00000000000000000000 010001      j       address[17]             skip to and, r9, r3, r4
-------------------------------------------------------------------------------------------------------------------
20100003        001000 00000 10000 0000000000000011     addi    r16, r0, -4             r16 = 3     SKIPPED BY JUMP
2011000a        001000 00000 10001 0000000000001010     addi    r17, r0, 10             r17 = 10   SKIPPED BY JUMP
2012000f        001000 00000 10010 0000000000001111     addi    r18, r0, 15             r18 = 10   SKIPPED BY JUMP
-------------------------------------------------------------------------------------------------------------------
00644824        000000 00011 00100 01001 00000 100100   and     r9, r3, r4              r9 = 4
00a45026        000000 00101 00100 01010 00000 100110   xor     r10, r5, r4             r10 = 2
00c71027        000000 00110 00111 00010 00000 100111   nor     r2, r6, r7              r2 = -12
0043402a        000000 00010 00011 01000 00000 101010   slt     r8, r2, r3              r8 = 1
29240003        001010 01001 00100 0000000000000011     slti    r4, r9, 3               r4 = 0
ac070004        101011 00000 00111 0000000000000100     sw      r7, 4(0)                4(0) = 11
8c030004        100011 00000 00011 0000000000000100     lw      r3, 4(0)                r3 = 11
00620820        000000 00011 00010 00001 00000 100000   add     r1, r3, r2              r1 = -1
```

4.2 Waveforms




Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/Processor_tb/L1/e1
/Processor_tb/L1/f1
/Processor_tb/L1/f2
/Processor_tb/L1/g1
/Processor_tb/L1/h1
/Processor_tb/L1/i1
/Processor_tb/L1/i4
/Processor_tb/L1/j1
/Processor_tb/L1/k1
/Processor_tb/L1/l1
/Processor_tb/L1/mua
/Processor_tb/L1/mub
/Processor_tb/L1/mud
/Processor_tb/L1/mue
/Processor_tb/L1/muf
/Processor_tb/L1/conc
/Processor_tb/L1/sll2
/Processor_tb/L1/alu1
/Processor_tb/L1/shamt
/Processor_tb/L1/mui
/Processor_tb/L1/muh
/Processor_tb/L1/savc
/Processor_tb/L1/loadc
/Processor_tb/L1/Andc
/Processor_tb/L1/Luiout
Now
Cursor 1
0 ns to 4200 ns
/Processor_tb/L1/mui


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/Processor_tb/L1/Instruction1
/Processor_tb/L1/k2
/Processor_tb/L1/Instruction2
/Processor_tb/L1/k3
/Processor_tb/L1/d3
/Processor_tb/L1/b3
/Processor_tb/L1/shamt3
/Processor_tb/L1/i3
/Processor_tb/L1/cc1
/Processor_tb/L1/cc2
/Processor_tb/L1/aa3
/Processor_tb/L1/aa4
/Processor_tb/L1/aa5
/Processor_tb/L1/aa6
/Processor_tb/L1/aa7
/Processor_tb/L1/aa8
/Processor_tb/L1/aa9
/Processor_tb/L1/aa14
/Processor_tb/L1/aa15
/Processor_tb/L1/aa16
/Processor_tb/L1/aa17
/Processor_tb/L1/rs2
/Processor_tb/L1/rt2
/Processor_tb/L1/k4
/Processor_tb/L1/d4
Now
Cursor 1
0 ns to 4200 ns
/Processor_tb/L1/f1


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
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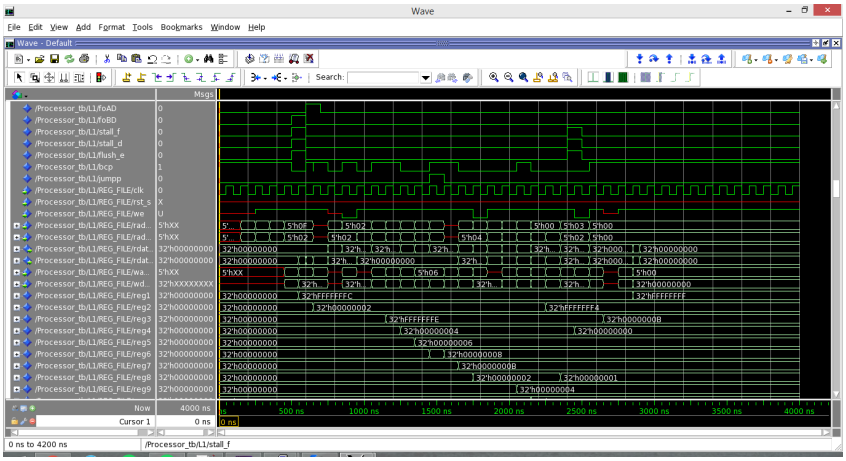
/Processor_tb/L1/ff1
/Processor_tb/L1/aaa3
/Processor_tb/L1/aaa4
/Processor_tb/L1/aaa7
/Processor_tb/L1/aaa9
/Processor_tb/L1/aaa14
/Processor_tb/L1/aaa15
/Processor_tb/L1/aaa16
/Processor_tb/L1/aaa17
/Processor_tb/L1/aa13
/Processor_tb/L1/k5
/Processor_tb/L1/d5
/Processor_tb/L1/g5
/Processor_tb/L1/muh5
/Processor_tb/L1/aaaa4
/Processor_tb/L1/aaaa9
/Processor_tb/L1/aaaa15
/Processor_tb/L1/aaa13
/Processor_tb/L1/mul
/Processor_tb/L1/mum
/Processor_tb/L1/mun
/Processor_tb/L1/muo
/Processor_tb/L1/foAE
/Processor_tb/L1/foBE
Now
Cursor 1
0 ns to 4200 ns
/Processor_tb/L1/foAE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File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
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Msgs
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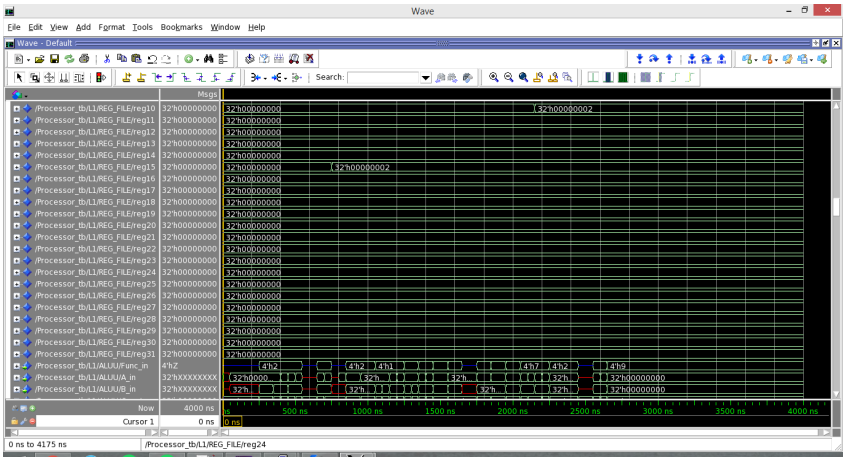
/Processor_tb/L1/stall_f
/Processor_tb/L1/stall_d
/Processor_tb/L1/flush_e
/Processor_tb/L1/fbcp
/Processor_tb/L1/jumpp
/Processor_tb/L1/REG_FILE/clk
/Processor_tb/L1/REG_FILE/rst_s
/Processor_tb/L1/REG_FILE/we
/Processor_tb/L1/REG_FILE/rad...
/Processor_tb/L1/REG_FILE/rad...
/Processor_tb/L1/REG_FILE/dat...
/Processor_tb/L1/REG_FILE/dat...
/Processor_tb/L1/REG_FILE/wa...
/Processor_tb/L1/REG_FILE/wd...
/Processor_tb/L1/REG_FILE/reg1
/Processor_tb/L1/REG_FILE/reg2
/Processor_tb/L1/REG_FILE/reg3
/Processor_tb/L1/REG_FILE/reg4
/Processor_tb/L1/REG_FILE/reg5
/Processor_tb/L1/REG_FILE/reg6
/Processor_tb/L1/REG_FILE/reg7
/Processor_tb/L1/REG_FILE/reg8
/Processor_tb/L1/REG_FILE/reg9
Now
Cursor 1
0 ns to 4200 ns
/Processor_tb/L1/stall_f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File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
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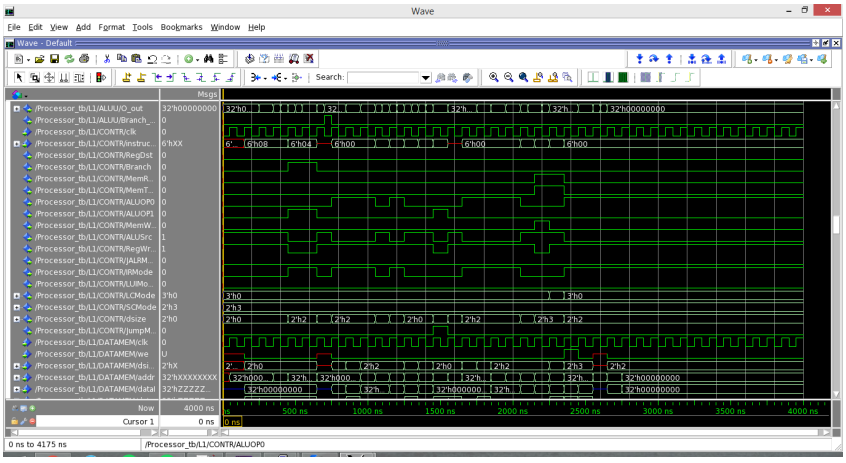
/Processor_tb/L1/REG_FILE/reg12
/Processor_tb/L1/REG_FILE/reg13
/Processor_tb/L1/REG_FILE/reg14
/Processor_tb/L1/REG_FILE/reg15
/Processor_tb/L1/REG_FILE/reg16
/Processor_tb/L1/REG_FILE/reg17
/Processor_tb/L1/REG_FILE/reg18
/Processor_tb/L1/REG_FILE/reg19
/Processor_tb/L1/REG_FILE/reg20
/Processor_tb/L1/REG_FILE/reg21
/Processor_tb/L1/REG_FILE/reg22
/Processor_tb/L1/REG_FILE/reg23
/Processor_tb/L1/REG_FILE/reg24
/Processor_tb/L1/REG_FILE/reg25
/Processor_tb/L1/REG_FILE/reg26
/Processor_tb/L1/REG_FILE/reg27
/Processor_tb/L1/REG_FILE/reg28
/Processor_tb/L1/REG_FILE/reg29
/Processor_tb/L1/REG_FILE/reg30
/Processor_tb/L1/REG_FILE/reg31
/Processor_tb/L1/ALUU/Func_in
/Processor_tb/L1/ALUU/A_in
/Processor_tb/L1/ALUU/B_in
Now
Cursor 1
0 ns to 4175 ns
/Processor_tb/L1/REG_FILE/reg24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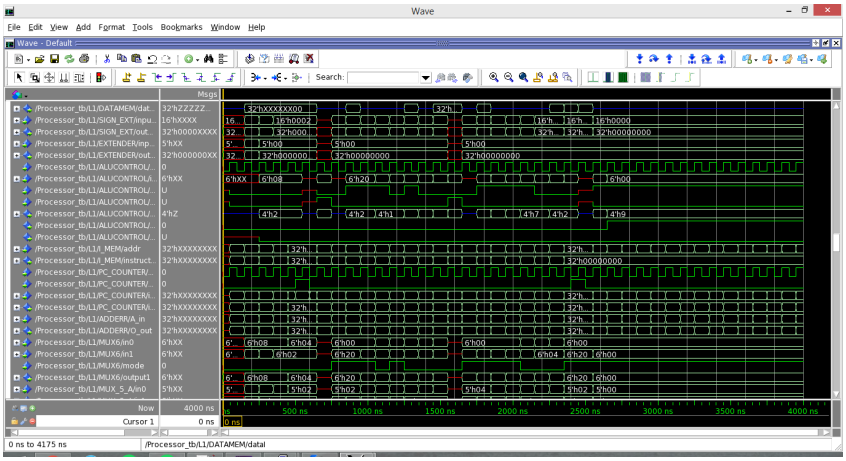
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/Processor_tb/L1/ALUU/O_out
/Processor_tb/L1/ALUU/Branch_...
/Processor_tb/L1/CONTR/clk
/Processor_tb/L1/CONTR/instruc...
/Processor_tb/L1/CONTR/RegDst
/Processor_tb/L1/CONTR/Branch
/Processor_tb/L1/CONTR/MemR...
/Processor_tb/L1/CONTR/MemT...
/Processor_tb/L1/CONTR/ALUOP0
/Processor_tb/L1/CONTR/ALUOP1
/Processor_tb/L1/CONTR/MemW...
/Processor_tb/L1/CONTR/ALUSrc
/Processor_tb/L1/CONTR/RegW...
/Processor_tb/L1/CONTR/JALRM...
/Processor_tb/L1/CONTR/IRMode
/Processor_tb/L1/CONTR/LUIMo...
/Processor_tb/L1/CONTR/LCMode
/Processor_tb/L1/CONTR/SCMode
/Processor_tb/L1/CONTR/dsize
/Processor_tb/L1/CONTR/JumpM...
/Processor_tb/L1/DATAMEM/clk
/Processor_tb/L1/DATAMEM/we
/Processor_tb/L1/DATAMEM/dsi...
/Processor_tb/L1/DATAMEM/addr
/Processor_tb/L1/DATAMEM/datal
Now
Cursor 1
0 ns to 4175 ns
/Processor_tb/L1/CONTR/ALUOP0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File Edit View Add Format Tools Bookmarks Window Help
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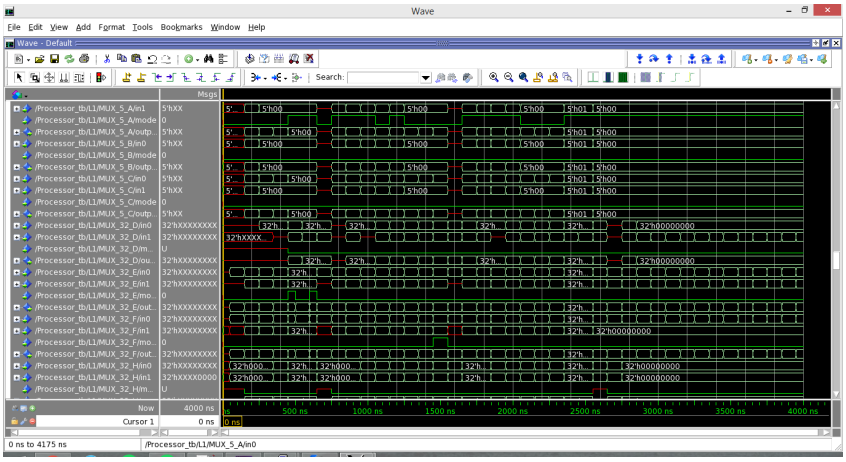
Search:
Msgs
Now
4000 ns
Cursor 1
0 ns
0 ns to 4175 ns
/Processor_tb/L1/DATAMEM/datal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Msgs
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Cursor 1
0 ns
0 ns to 4175 ns
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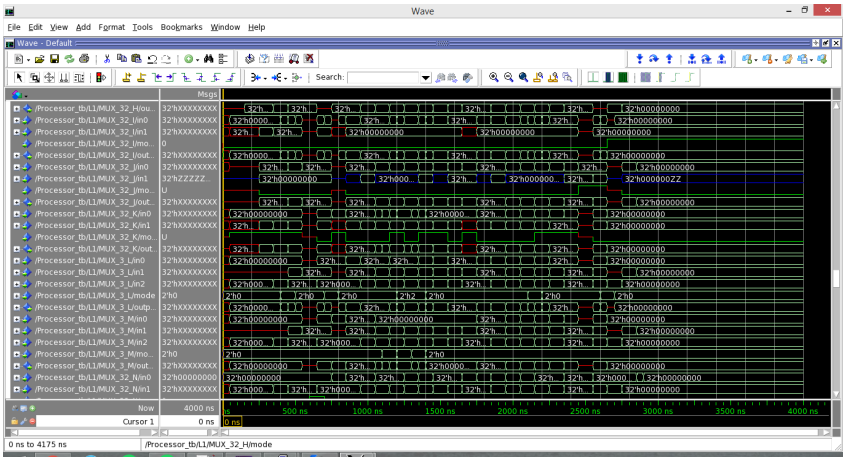
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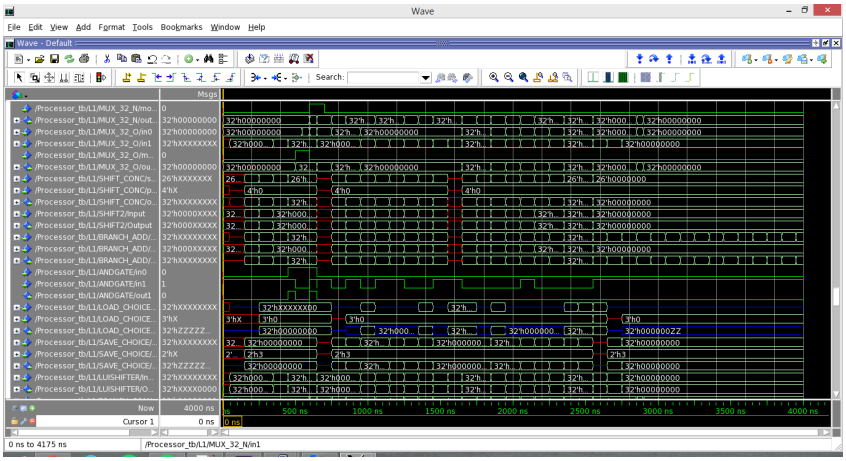
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Msgs
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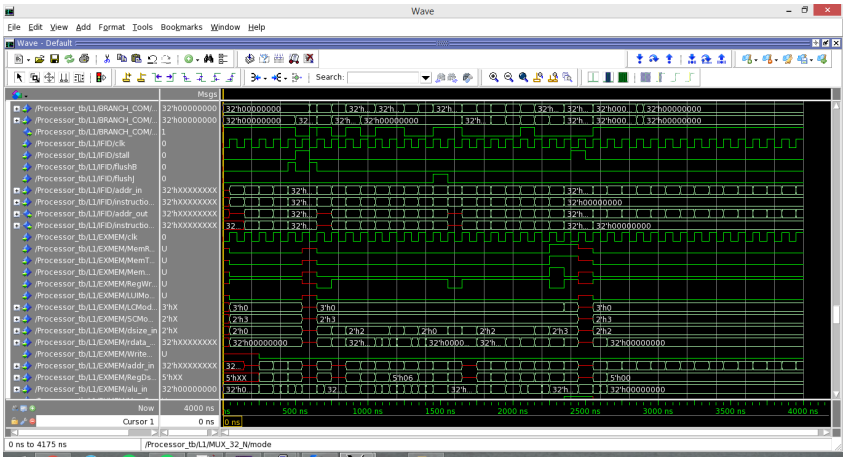
4000 ns
Cursor 1
0 ns
0 ns to 4175 ns
/Processor_tb/L1/MUX_32_N/in1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File Edit View Add Format Tools Bookmarks Window Help
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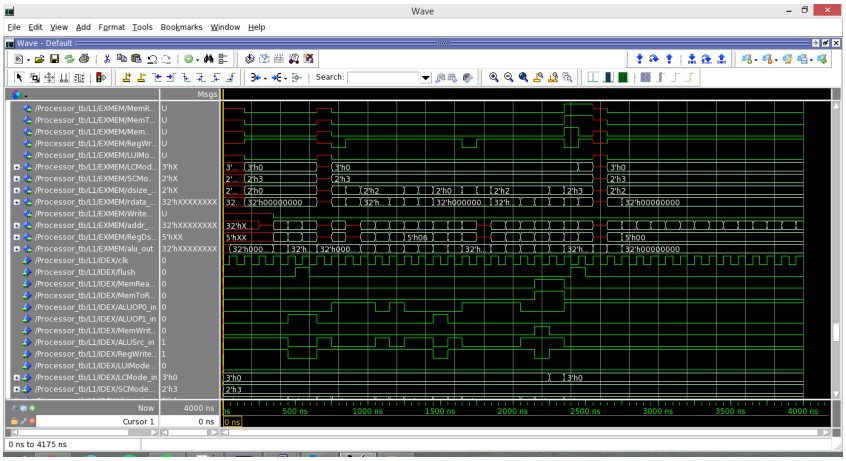
Search:
Msgs
Now
4000 ns
Cursor 1
0 ns
0 ns to 4175 ns
/Processor_tb/L1/MUX_32_N/mode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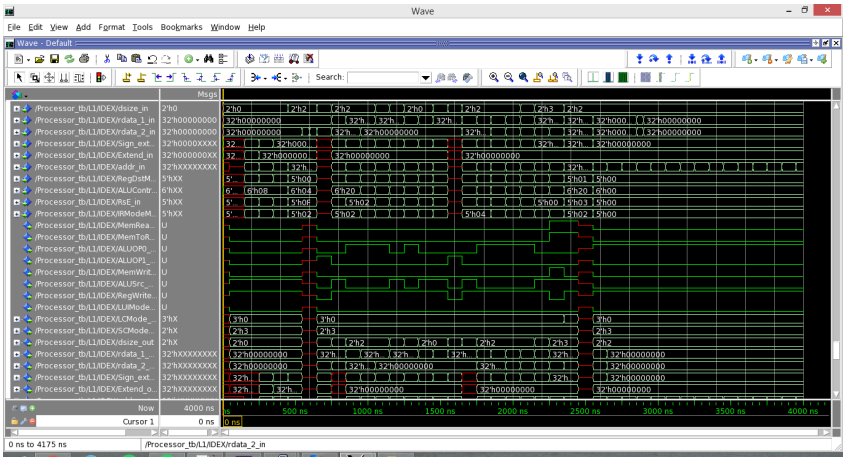
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
Now
4000 ns
Cursor 1
0 ns
0 ns to 4175 ns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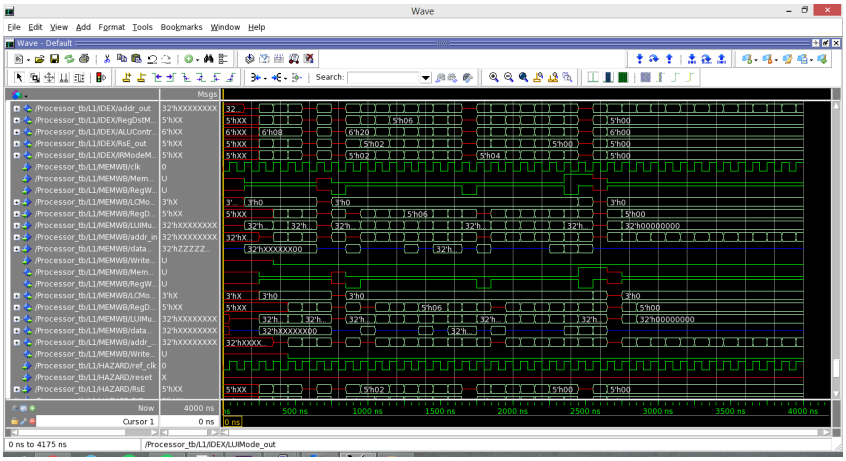
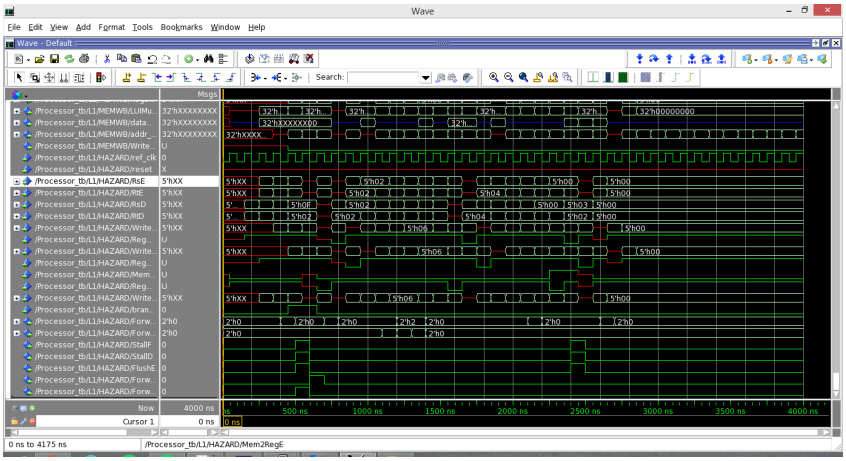
Search:
Msgs
Now
4000 ns
Cursor 1
0 ns
0 ns to 4175 ns
/Processor_tb/L1/IDEX/rdata_2_in


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
Now
4000 ns
Cursor 1
0 ns
0 ns to 4175 ns
/Processor_tb/L1/IDEX/LUIMode_out


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
Now
4000 ns
Cursor 1
0 ns
0 ns to 4175 ns
/Processor_tb/L1/HAZARD/Mem2RegE

5 Synthesis

In this lab, we were able to synthesize our processor. We experienced some difficulties when synthesizing including the synthesizer removing some of our components when optimizing. To solve that issue, we had to specify some options when synthesizing to prevent the optimization.

5.1 Area

```
Number of ports:                         34
Number of nets:                        1374
Number of cells:                         38
Number of combinational cells:            2
Number of sequential cells:               0
Number of macros/black boxes:             0
Number of buf/inv:                        1
Number of references:                    38

Combinational area:              16977.581641
Buf/Inv area:                      783.271812
Noncombinational area:           11965.862345
Macro/Black Box area:                0.000000
Net Interconnect area:           11959.287554

Total cell area:                 28943.443986
Total area:                      40902.731540
```

```
Area of detected synthetic parts
--------------------------------
                                          Perc. of
  Module               Implem.  Count       Area cell area
  -------------------- -------  ----- ---------- ---------
  DP_OP_45J4_122_6278     str       1   539.2930      1.9%
  DW01_add             apparch      2   318.1884      1.1%
  DW_cmp               apparch      2   423.4039      1.5%
  -------------------- -------  ----- ---------- ---------
  DP_OP Subtotal:                   1   539.2930      1.9%
  Total:                            5  1280.8852      4.4%

Estimated area of ungrouped synthetic parts
-------------------------------------------
                                Estimated  Perc. of
  Module     Implem.  Count       Area cell area
  ---------- -------  ----- ---------- ---------
  DW_cmp     apparch     18   176.8322      0.6%
  DW_leftsh     astr      1   535.9893      1.9%
  DW_rightsh    astr      1   429.7576      1.5%
  DW_sra        astr      1   541.3268      1.9%
  ---------- -------  ----- ---------- ---------
  Total:                 21  1683.9059      5.8%

Subtotal of datapath(DP_OP) cell area:  539.2930  1.9%  (estimated)
Total synthetic cell area:              2964.7911  10.2%  (estimated)
```

5.2 Power

Hierarchy	Switch Power	Int Power	Leak Power	Total Power	%
Processor	27.369	5.74e+03	2.20e+10	2.78e+04	100.0

5.3 Timing

data arrival time			1.98
clock clk (rise edge)		2.00	2.00
clock network delay (ideal)		0.00	2.00
EXMEM/alu_out_reg[29]/CLK (DFFX1_LVT)		0.00	2.00 r
library setup time		-0.02	1.98
data required time			1.98
data required time			1.98
data arrival time			-1.98
slack (MET)			0.00

Since we get zero slack when running our processor with a clock period of 2 ns. The frequency of our processor would be 500 MHz