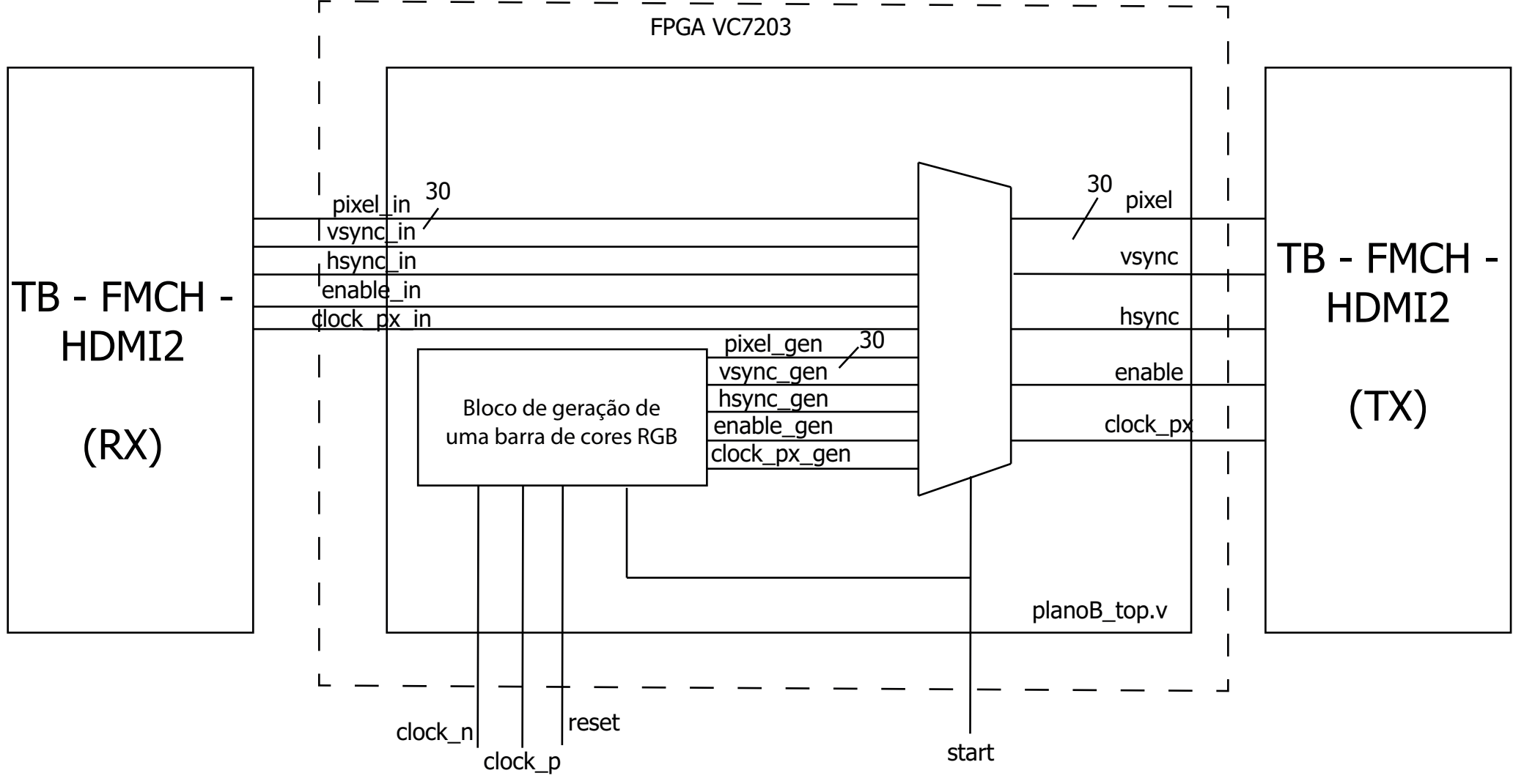
FPGA VC7203
TB - FMCH - HDMI2
(RX)
pixel_in
30
vsync_in
hsync_in
enable_in
clock_px_in
Bloco de geração de uma barra de cores RGB
pixel_gen
30
vsync_gen
hsync_gen
enable_gen
clock_px_gen
30
pixel
vsync
hsync
enable
clock_px
planoB_top.v
TB - FMCH - HDMI2
(TX)
clock_n
clock_p
reset
start