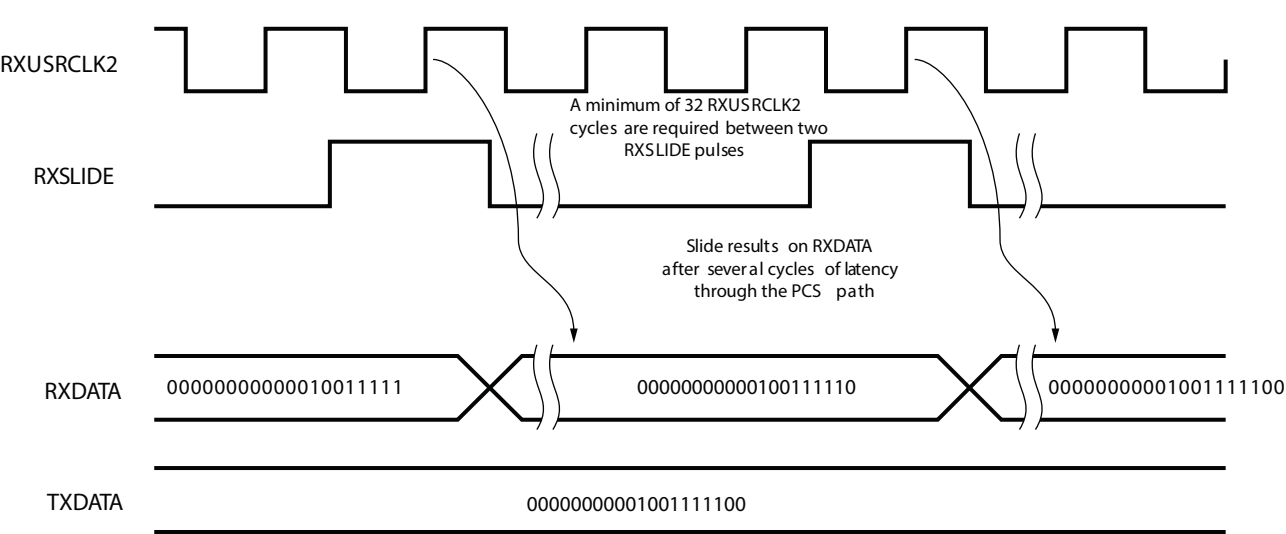
RXUSRCLK2
RXSLIDE
A minimum of 32 RXUSRCLK2 cycles are required between two RXSLIDE pulses
Slide results on RXDATA after several cycles of latency through the PCS path
RXDATA
00000000000010011111
00000000000100111110
00000000001001111100
TXDATA
00000000001001111100