Assignment No. VI, Monday
Computer Organisation - CS220

---

1. The objective of this assignment is to compute the 32-bit IEEE single-precision floating-point addition. Once you have written the code in Verilog, you need to create an FPGA IP of that, interface the created IP with the Zynq processor, and verify the design on the FPGA.

2. The objective of this assignment is to compute the 32-bit IEEE single-precision floating-point multiplier. Once you have written the code in Verilog, you need to create an FPGA IP of that, interface the created IP with the Zynq processor, and verify the design on the FPGA. You can use the "*" operator to multiply two integers.