Assignment No. IV, Monday
Computer Organisation - CS220

1. This assignment aims to create an SRAM architecture using two-level decoding, as discussed in class.

   - Design an SRAM of dimension 16×32 using D-flipflop, decoder and multiplexer. The block diagram of this SRAM is shown in Figure 1
   - Using this 16×32, design a memory of dimension 512×8.

   You need to verify the design on the simulation using the Vivado tool (using post-implementation simulation)

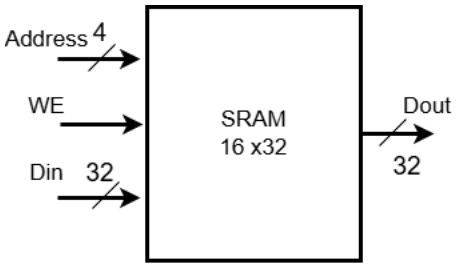

Figure 1: 16×32 SRAM

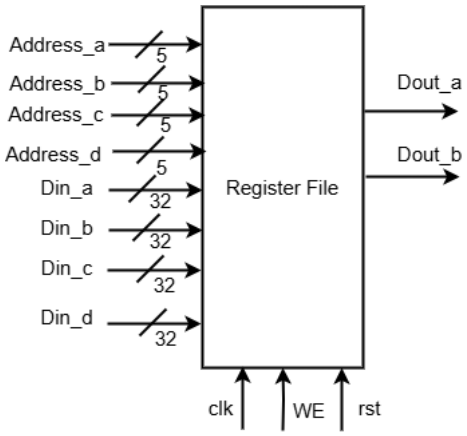

Figure 2: Target Register File

2. Tyrion Lannister wants to create a register file with two read ports and four write ports. The block diagram of the register file is shown in Figure 2. The register file has four address inputs, four data input ports, two data output ports, one write enable, clock, and reset signal. The register file contains 32 registers, each of 32 bits. Write a Verilog code to implement this register file. Note that "write" happens in the register file only when WE is 1. Also, note that during a collision, port a has the highest priority for write, followed by port b, c, and d.

   - You need to solve this question using the structural coding style.
   - You need to verify the design on the FPGA using the IP.