**Assignment No. II, Monday**
Computer Organisation - CS220

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1. Design a mod-10 gray code counter using structural style coding. Verify the design using a test bench. You do not need to develop an IP for this and verify the design on FPGA. The storage element used in this code has to be T flip-flops. A mod 10 gray counter starts counting from state 000 and then counts 0001, 0011,0010, 0110,0111, 0101, 0100, 1100, 1101. After it reached 1101, it goes back to state 0000. Your code must have a synchronous reset.

2. Professor Calculus wants to develop an FPGA adder only using $LUT6\_2$ and $CARRY4$ primitives. But he wants the adder to require $n$ LUTS and to have a delay of only $n/2$ carry chains. He asked his friend Tintin to help him to achieve this objective. Tintin comes up with the following idea:
"A single LUT can generate outputs of two or five input functions if the inputs are shared. Let us consider the scenario where we need to produce the carry output $C_i$ from the inputs $A_{i-1}, Ai-2$, $B_{i-1}, B_{i-2}$ and $C_{i-2}$.

$$C_{i-1} = G_{i-2} + P_{i-2}.C_{i-2},\ G_{i-2} = A_{i-2}.B_{i-2},\ P_{i-2} = A_{i-2} \oplus B_{i-2}$$
$$C_i = G_{i-1} + P_{i-1}.C_{i-1},\ G_{i-1} = A_{i-1}.B_{i-1},\ P_{i-1} = A_{i-1} \oplus B_{i-1}$$

If we now combine these two equations, we will get

$$C_i = G_{i-1:i-2} + P_{i-1:i-2}C_{i-2}$$
$$C_i = \overline{P_{i-1:i-2}}.G_{i-1:i-2} + P_{i-1:i-2}C_{i-2}$$
$$G_{i-1:i-2} = (A_{i-1}.B_{i-1})|(A_{i-1} \oplus B_{i-1}).(A_{i-2}.B_{i-2})$$
$$P_{i-1:i-2} = (A_{i-1} \oplus B_{i-1}).(A_{i-2} \oplus B_{i-2})$$

We can produce propagate for two-bit signals ($P_{i-1:i-2}$) and generate for two-bit signals ($G_{i-1:i-2}$) from a single LUT. Hence, this architecture can generate the carry output of an $n$ bit addition using $n/2$ LUTs."
Professor Calculus understood this design but was still confused as there were still open questions regarding how to produce the sum bits. Help Professor Calculus by designing this adder architecture that will require $n$ LUTs and $n/2$ carry chain delay

- You need to verify the design on FPGA using IP for n=1024.
- You need to compare the design performance by measuring the path delay and comparing it with that of normal ripple carry based 1024 bit adder. An additional video will be uploaded to HelloIITK to show how to measure path delay.