Assignment No. III, Monday

Computer Organisation - CS220

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1. Design a 3-bit gray code counter that has reset, clock as inputs, and a single bit "z" as output. The counter should be capable of counting as per gray code up to 7 and produces "Z=1" for every 8 clock cycles. After the 7th state is reached, the counter goes to the initial state.

    - You need to solve this question using the behavioral coding style of coding a Finite State Machine, as shown in the FSM template of the last lecture.
    - You need to verify the design on the simulation using the Vivado tool (using post-implementation simulation)

2. You have to design a synchronous sequential circuit that produces output "1" whenever any of the following input sequences "1100", "1010" or "1001" occurs. The circuit resets to the initial state after a "1" output is generated

    - You need to solve this question using the behavioral coding style of coding a Finite State Machine, as shown in the FSM template of the last lecture.
    - You need to verify the design on the simulation using the Vivado tool (using post-implementation simulation)