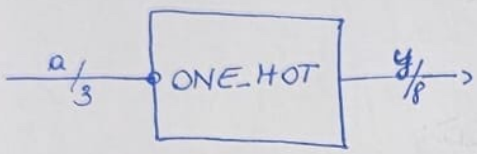
Limbaje de descriere hardware 6.11.2024
Curs 5

*1) Să se implementeze un decodor ONE HOT cu o intrare pe 8 biți.



a[2]	a[1]	a[0]	y[7...0]
0	0	0	00000001
0	0	1	00000010
0	1	0	00000100
0	1	1	...
1	0	0	...
1	0	1	...
1	1	0	...
1	1	1	10000000

```
LIBRARY ieee
USE ieee.std_logic_1164.all
ENTITY cod_one_hot is
    PORT(a: IN std_logic_vector(2 DOWNTO 0);
         y: OUT std_logic_vector(7 DOWNTO 0));
END cod_one_hot;
ARCHITECTURE atr_directa OF cod_one_hot is
BEGIN
    y(0)<= NOT a(2) AND NOT a(1) AND NOT a(0);
    y(1)<= NOT a(2) AND NOT a(1) AND a(0);
    ...
    y(6)<= a(2) AND a(1) AND a(0);
END atr_directa;
```

2) Implementarea modulului ONE HOT utilizând specificația WHEN/ELSE.

```
ARCHITECTURE atribuire_condiționată OF dec_ONE_HOT IS
BEGIN
   y<="00000001" WHEN a="000" ELSE
      "00000010" WHEN a="001" ELSE
      ..... .....
      "01000000" WHEN a="110" ELSE
      "10000000";
END atribuire_condițională;
```

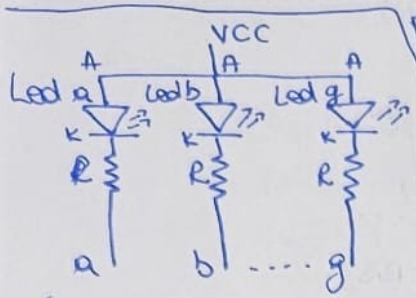
3) Implementarea folosind specificație selectivă

```
ARCHITECTURE atribuirea_selectivă OF dec_ONE_HOT IS
   BEGIN
      WITH a SELECT
         y<= x"01" WHEN "000",
             x"02" WHEN "001",
             ..... .....
             x"40" WHEN "110",
             x"80" WHEN OTHERS;
END atribuire_selectivă;
```

În vederea implementării unui modul de viteză, se recomandă implementarea circuitului ONE HOT prin prima metodă folosind atribuire directă.

Fiind un tabel de adevăr, implementarea cea mai rapidă a acestuia se face prin atribuirea selectivă în care sunt scrise explicit alternativele fiecărei în parte.

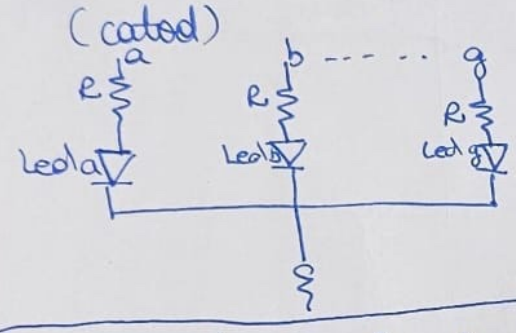
* 4) Să se implementeze un decodor din 7 segmente cu posibilitatea de stingere a segmentelor cu activarea sau dezactivarea unui pin EN (enable). Segmentele afișoare au anodul comun.



(anod comun)

Led-ul se comandă în curent și nu în tensiune.

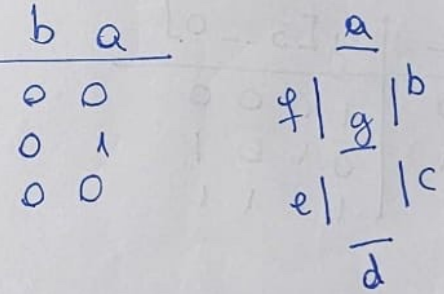
0 = led aprins
1 = led stins

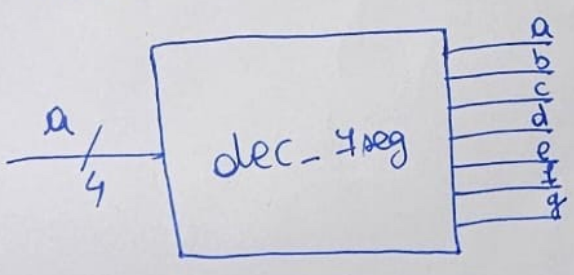


1 = led aprins
0 = led stins

tabel pt ~~anod~~ anod comun

a_in[3..0]	g	f	d	c	b	a
0 0 0 0	1	0	0	0	0	0
0 0 0 1	1	1	1	0	0	1
0 0 1 0	1	1	0	1	0	0
⋮	0	1				
⋮	⋮					
1 1 1 1	0	0	1	1	1	0



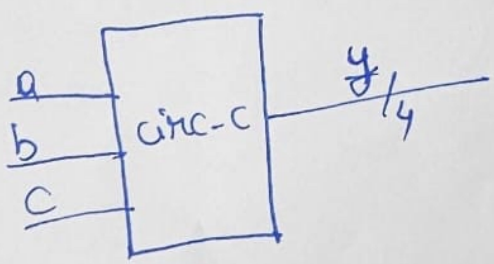


```
LIBRARY ieee
USE ieee.std_logic_1164.all
ENTITY dec_7seg is
   PORT (a_in : IN std_logic_vector (3 DOWNTO 0);
         a,b,c,d,e,f,g: std_logic);
END dec_7seg;
ARCHITECTURE dscr OF dec_7seg IS
   SIGNAL temp :std_logic_vector (6 DOWNTO 0);
BEGIN
   WITH a_in SELECT
     temp <= "1000000" WHEN "0000",
             "1111001" WHEN "0001",
             ..........
             "0001110" WHEN OTHERS;

   a <=temp(0);
   b <=temp(1);
   :
   g <=temp(6);
END dscr;
```

alta situație:

a	b	c	y[3..0]
0	0	0	1 0 0 0
0	0	1	0 1 0 1
in rest			1 1 1 1



```
LIBRARY IEEE
USE IEEE.std_logic_1164.all
ENTITY circuit_c IS
   PORT (a,b,c:IN std_logic;
         y : OUT std_logic_vector(3 DOWNTO 0));
END circuit_c;
ARCHITECTURE dacn OF circuit_c IS
   SIGNAL temp: std_logic_vector (2DOWNTO 0);
BEGIN
   temp <= a & b & c;
   WITH temp SELECT
     y <= "1000" WHEN "0000";
          "0101" WHEN "0001",
          "1111" WHEN OTHERS;
END dacn;
```

& = si