





Design Rules Verification Report

Filename : C:\Users\Marius\Documents\GitHub\LCD_Timer_Clock\HW\PCB_TOP\PCB_TOP.CSPcbDoc

Warnings 2
Rule Violations 0

Warnings	
Multilayer Pads with 0 size Hole found	2
Total	2

Rule Violations	
Clearance Constraint (Gap=0.1mm) (All),(All)	0
Width Constraint (Min=0.125mm) (Max=2mm) (Preferred=0.2mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((Disabled)(All))	0
Minimum Annular Ring (Minimum=0.2mm) (All)	0
Hole Size Constraint (Min=0.2mm) (Max=6.3mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.05mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.15mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.153mm) (All),(All)	0
Silk primitive without silk layer	0
Unpoured Polygon (Allow unpoured: False)	0
Total	0

Multilayer Pads with 0 size Hole found	
Pad FIDJ101-1(-18.7mm,31.2mm) Multi-Layer	
Pad FIDJ100-1(12.8mm,-33.1mm) Multi-Layer	

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for Timer_Clock_TOP.PrjPcb