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Division of Industrial Electronics

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Development of the smart transformer average model for
analysis of selected control algorithms

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Abstract

Over time the number of renewable energy sources and new loads in the distribution grids increases. Therefore, the topic of Smart Transformer (ST) as a key element of the Smart Grids is becoming very popular. One of the important elements of the ST design process is to create its entire simulation model along with its complete control strategy. Unfortunately, the construction of a switching model of the whole ST due to many switches results in a huge complexity of calculations. Therefore, the main goal of the thesis is to develop the ST average model which allows verifying the considered topology of ST from the control point of view. As a result, the average model the ST has been created and its correctness has been proved by comparing the detailed model and the average model behaviour of individual parts of the ST. The developed model has allowed to significant reduction in simulation time which has made possible to analyse the behaviour of entire ST with selected control algorithms.

Keywords: Smart Transformer, Solid State Transformer, Average model

Opracowanie uśrednionego modelu inteligentnego transformatora do analizy wybranych algorytmów sterowania

Streszczenie

Z biegiem czasu rośnie liczba odnawialnych źródeł energii i nowych obciążeń w sieciach energetycznych. W związku z tym temat inteligentnego transformatora jako kluczowego elementu inteligentnych sieci staje się bardzo popularny. Jednym z ważnych elementów procesu projektowania inteligentnego transformatora jest utworzenie jego całego modelu symulacyjnego wraz z pełną strategią sterowania. Niestety konstrukcja modelu łączniowego wiąże się z ogromną złożonością obliczeniową z uwagi na dużą ilość elementów półprzewodnikowych. Dlatego głównym celem pracy jest opracowanie

modelu uśrednionego transformatora inteligentnego, który pozwala zweryfikować kompletną strategię sterowania rozważanej topologii. W rezultacie został sporządzony model uśredniony rozważanej topologii transformatora inteligentnego, a jego poprawność została zweryfikowana poprzez porównanie zachowania modelów łączniowego i opracowanego modelu poszczególnych części transformatora inteligentnego. Zastosowanie opracowanego modelu pozwoliło na znaczne skrócenie czasu symulacji, co umożliwiło przeanalizować zachowanie całego transformatora inteligentnego łącznie z jego wybranymi algorytmami sterowania.

Słowa kluczowe: Inteligentny transformator, Transformator półprzewodnikowy, Model uśredniony

Warsaw, 15 wrzesień 2019

POLITECHNIKA WARSZAWSKA
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Contents

1	Introduction	1
1.1	History of the Smart Transformer	1
1.2	Solid State Transformer architectures	2
1.3	Simulation complexity of the ST detailed model	4
1.4	Aim of the thesis	5
2	Averaged model of considered ST	6
2.1	Considered ST structure	6
2.2	Averaged model of star-connected Cascaded H-Bridge converter	7
2.3	Averaged model of isolated DC-MV/DC-LV converter	10
2.4	Averaged model of modular 4 leg LV-DC/LV-AC T-Type converter	17
2.5	Conclusions	20
3	Basic control methods of ST	21
3.1	Control algorithm of AC-MV/DC-MV part od ST	21
3.2	Control algorithm of DC-MV/DC-LV part od ST	24
3.3	Control algorithm of DC-LV/AC-LV stage	26
3.4	Load Identification Algorithms for LV side of ST	28
3.4.1	Load models	28
3.4.2	Accurate Load Identification	30
3.4.3	Load Sensitivity Identification	33
3.4.4	Overload protection control	35
3.4.5	Soft Load Reduction Control	36
4	Simulation study	38
4.1	Comparison of detailed and average models of each ST part	38
4.2	The behaviour of the ST average model in specific conditions	43
4.3	Load identification algorithm: Simulation results	45
4.3.1	Converter and load models	45
4.3.2	Accurate Load Identification	46

4.3.3	Load Sensitivity Identification	49
4.3.4	Overload protection control	49
4.3.5	Soft load reduction control	51
5	Final Conclusions	53

Podziękowania

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Chapter 1

Introduction

1.1 History of the Smart Transformer

For the first time in the science community, the term Solid State Transformer (SST) appeared in the McMurray's patent in 1968 [1]. The SST concept contained solid state switches that allow building an internal high-frequency circuit with a much smaller transformer. The SST features from the patent were similar to a low-frequency transformer [2].

However, the first application of SST took place in the 1990s in traction system. In those days, the popular traction energy systems worked at 16.6 Hz what created a problem of large size and high weight of classical transformers [2]. Therefore, it was decided to replace them with SST. It allowed reducing the mass and volume of the device by about 20-50%. Moreover, it increased efficiency from 93% to 96% [2].

Over time, the SST was less important in traction networks, which more often were transformed from the frequency of 16.6 Hz into 50 Hz. In 50 Hz systems the profits of the SST was not such attractive.

The topic of SST returned to the context of smart grids, where its smaller dimensions and weight are less important, however its additional functions, among others, classical solution like the ability to control the medium voltage (MV) AC and low voltage (LV) AC sides makes it attractive from the power management point of view.

Nowadays the SST is a power electronic converter which allows scaling the voltage level between input and output but also controlling power flow in both directions and provides galvanic isolation [3]. In a broader context, the SST as integrated part of the smart grid through its communication and control functionalities and with the possibility of direct connection of energy storage is named a Smart Transformer (ST) [2]. It means that the ST in its structure

must contain at least two power stages to ensure DC-link connectivity [4]. The ST also provides ancillary services such as reactive power compensation from the MV side as well as the possibility of adjustment loads on the LV side. Moreover, the ST enables reduction of harmonics and transients from both the input and output side and also simpler integration with both DC and AC systems. The ST, in contrast to the SST, thanks to its additional functions for distribution grids allows optimizing their efficiency.

To sum up, the ST is a response to the ever-changing distribution grid that includes more and more renewable energy sources (RES) and more and more new loads like electric vehicles (EVs) [5].

1.2 Solid State Transformer architectures

A wide range of SST structures and topologies can be found in the literature. The SST classification due to the number of power stages and the modularity of its structure is presented in Figure 1.1 and 1.2 respectively [4].

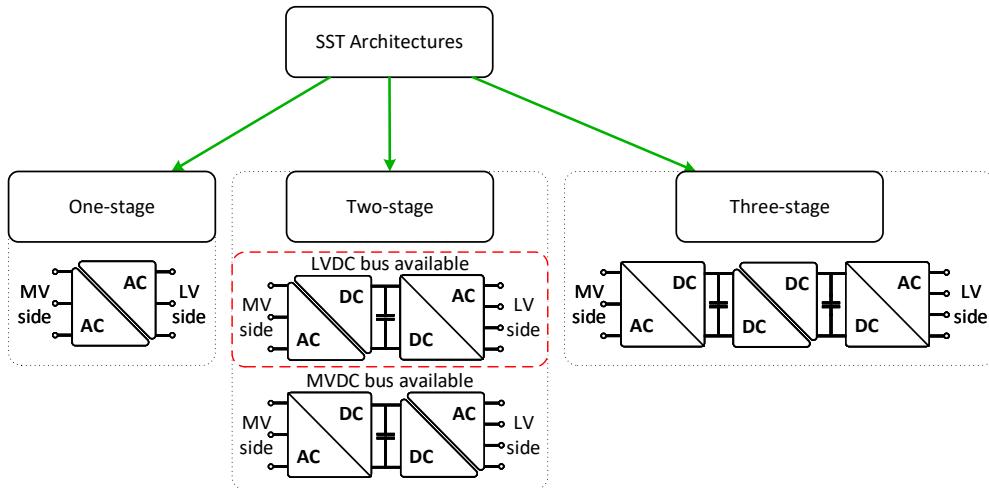


Figure 1.1: Classification of the SST architectures due to the number of power stages with marked considered ST structure

One of the possible structure of SST with one power stage is AC/AC converter [6]. It is characterized by high efficiency and high power density but on the other hand, there is no DC-link to provide the possibility of direct connection of energy storage which makes its control functionalities limited. Therefore, the one stage SST cannot meet the requirement of SST

integration with the energy storage and advance power management, which characterized ST [4]. The other possible structure is two-stage SST. This architecture contains one DC bus therefore it allows for cooperation with the energy storage. It means that SST with two power stages can be ST. In the literature there are also three-stage SSTs. They contain much more bulky elements such as capacitors, but they offer the most control functionality due to access to MV and LV DC buses. Both two-stage and three-stage allow to decouple the input side from the output side of SST.

Another SST classification is based on modularity (Figure 1.2). One of them is the non-modular SST architecture, which disadvantage is necessary to use high-voltage semiconductor switches on the SST high-voltage side. This architecture also causes problems in creating fault tolerant structure [4], but on the other hand, the advantage of the architecture is a small amount of semiconductor, sensors and single high-frequency transformers which reduces the chance of a fault. The modular architecture allows relatively simple to create a fault tolerant structure of SST and implement fault strategy. Modularity also allows to scalability in power and voltage, more simple maintenance as well as smaller electromagnetic interference emissions in comparison to non-modular architectures. A similar concept to the modular structure is the semi-modular structure. It is characterized by the same advantages as a modular structure but the number of required semiconductor switches is reduced. Moreover, the cells are more complicated and the structure of the semi-modular architecture is based on a single multi-port high-frequency transformer [4].

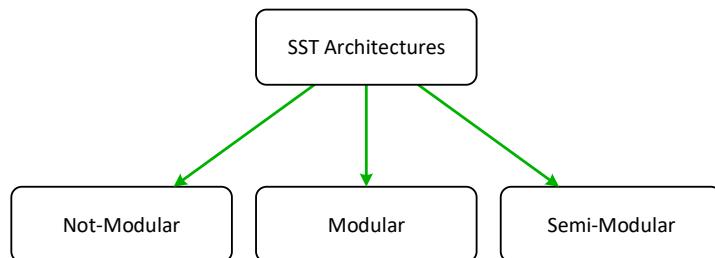


Figure 1.2: Classification of the SST architectures due to modularity

1.3 Simulation complexity of the ST detailed model

The problem of building a large detailed model of the ST results from the simulation method of switching processes. Due to the fact that power converters in their structure usually contain many switching elements, it makes their power circuit non-linear. Therefore, e.g. PLECS software uses a dedicated algorithm to simulate electrical circuits with switching elements, which has been described in detail in the PLECS manual [7].

The PLECS algorithm creates a linear time-varying (LTV) state space associated with all signals in the simulated model (Eq. 1.1).

$$\begin{aligned}\dot{x} &= A_\sigma x + B_\sigma u \\ y &= C_\sigma x + D_\sigma u\end{aligned}\quad (1.1)$$

The index σ means that the algorithm creates a set of state-space matrices for each possible state change of switching elements. It means the circuit is represented by numbers of linear time-invariant (LTI) models. The method of operation of the algorithm is shown in Figure 1.3.

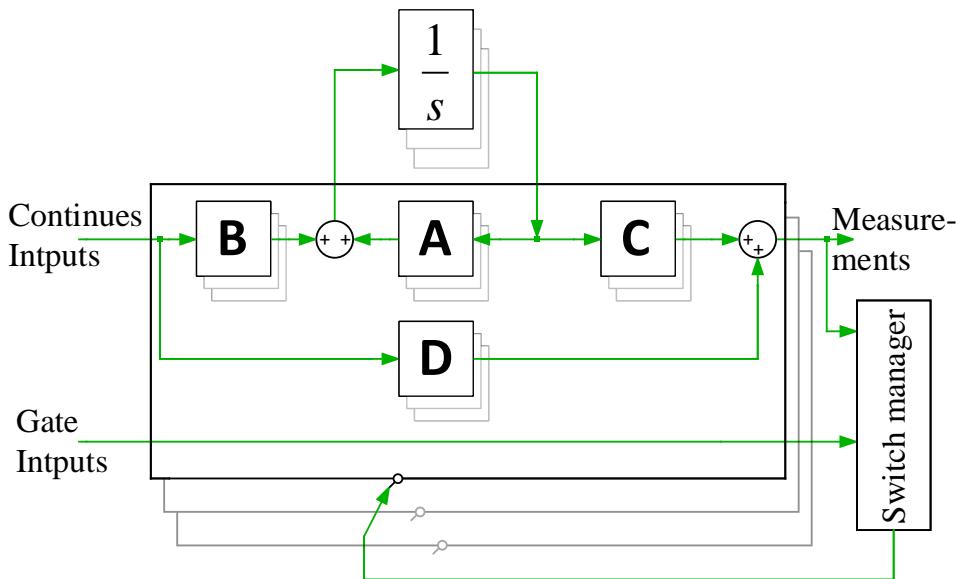


Figure 1.3: Block diagram of the physical model in PLECS software

In addition to these LTI state spaces, there is a block which is called the Switch Manager presented in Figure 1.3. The block observes the signals and makes decisions whether a changing the LTI state space is necessary.

That method allows to obtain the model which is linear and time-invariant for each switch state permutation. Moreover it allows determining the output vector y in an efficient way. But on the other hand, this way of representing switching circuit makes a number of state space permutation equals 2 to the power on n , where n is the total number of switching elements. That means the number of modes grows exponentially with the numbers of switches in the circuit, which requires a lot of memory. Moreover increasing the size of the simulation model have an influence on increasing in the size of matrices A, B, C and D . Therefore, it causes the complexity of calculations and thus also the simulation time increases significantly with the increase of the switches. Therefore, in case of it is a good practice to create the ST average model instead of the full switching model.

1.4 Aim of the thesis

The main goal of the thesis is to develop a ST simulation model which allows verifying the considered topology of ST from the control point of view. Moreover, the model should give the opportunity to test the whole advance control algorithm of the ST.

Due to the fact that the detailed model with a large number of switching elements is characterized by a large computational complexity, construction of an average model is a very important part of the ST development process.

This Master's thesis is carried out within the framework of the project entitled "Highly efficient and fault tolerant SiC-based smart transformer in distributed energy systems", the considered average ST structure is dedicated to the purposes of this project.

The dissertation is split into five chapters. The first chapter contains a brief description of ST history, currently considered SST structures, explanation of the problem of simulating large converter models and the purpose of the thesis. The next chapter describes the process of averaging model of individual parts of ST to create the average model of the whole ST. The third chapter describes the basic control algorithms of each part of ST and load identification algorithms for LV side of ST. An analysed control strategies are implemented on individual parts of ST on both detailed and average models in order to compare their behaviour (Chapter 4). At the end of the thesis final conclusions are formulated (Chapter 5).

Chapter 2

Averaged model of considered ST

Average modelling is an effective way to analyse the dynamic behaviour of power electronics converters (PEC). It brings many benefits due to its simplicity and significant reduction of simulation time in comparison with detailed models. However, it is worth paying attention to the fact that in the averaging process, it omits signal fluctuations resulting from switching processes. It means that the average model is able to reproduce only slow-changing signals. This is due to the fact that averaging operation is one of the low-pass filters. Fortunately, from considered ST control strategy point of view, the signal ripple resulting from the switching processes can be omitted in simulation study. In the thesis a module is understood as the smallest averaged parts of ST from which the whole average model ST is built.

2.1 Considered ST structure

The considered structure of the ST prototype is depicted in Figure 2.1. It exposes a huge number of switches (154 transistors and 154 diodes), which confirms the need to build an average ST model.

The ST has a modular multi-stage structure in which two main stages can be distinguished what is shown in Figure 2.1. The first is AC-MV/DC-LV converter which contains a star-connected cascaded H-bridge and an isolated DC-MV/DC-LV converter. The second one is a modular 4-leg DC/AC T-Type converter as a DC-LV/AC-LV stage of the ST. The process of creating the average model of ST is considered separately for each part of ST. The way of forming individual averaging models are described in the sections 2.2-2.4. After that, the whole average model is verified.

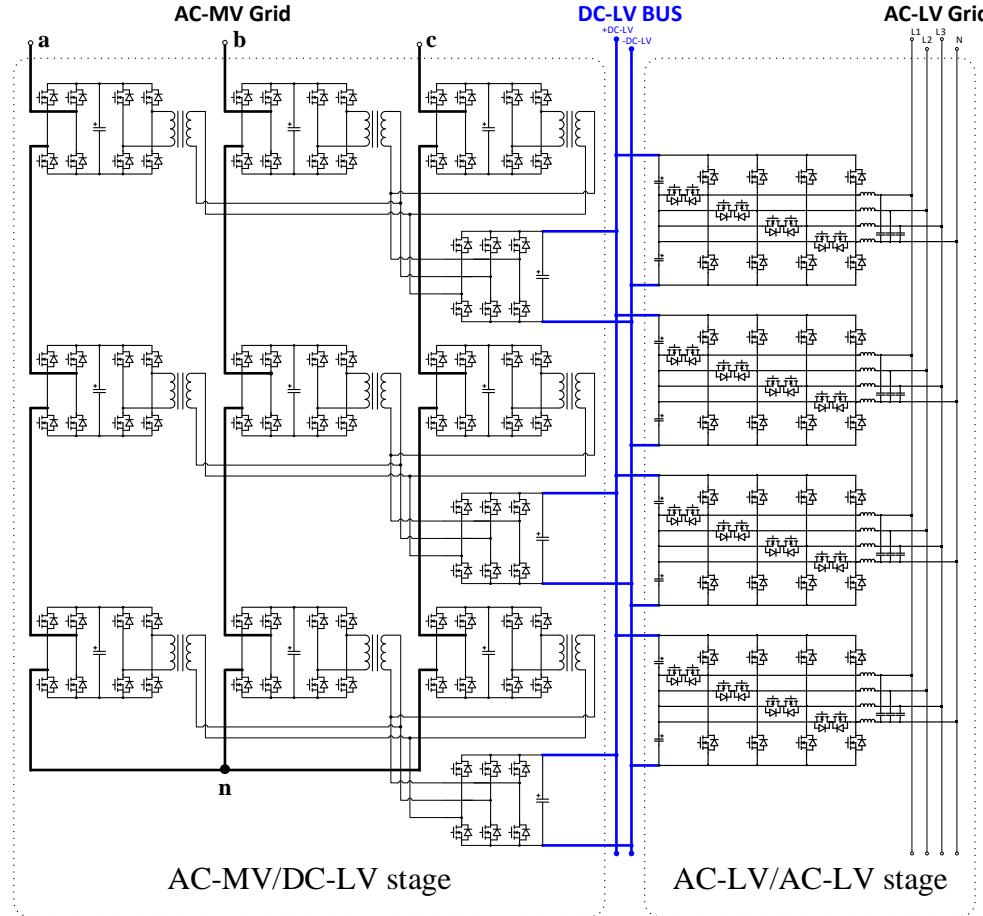


Figure 2.1: The considered ST structure with highlighted power stages and LV-DC bus.

2.2 Averaged model of star-connected Cascaded H-Bridge converter

Star-connected Cascaded H-Bridge (CHB) converter contains lots of switching elements. Therefore, it seems necessary to split this converter into smaller modules which can be average in a less complicated way what is shown in Figure 2.2.

The main aim of the average model of each part of ST is the ability to test a control algorithm which is in detail described in Section 3.1. The algorithm

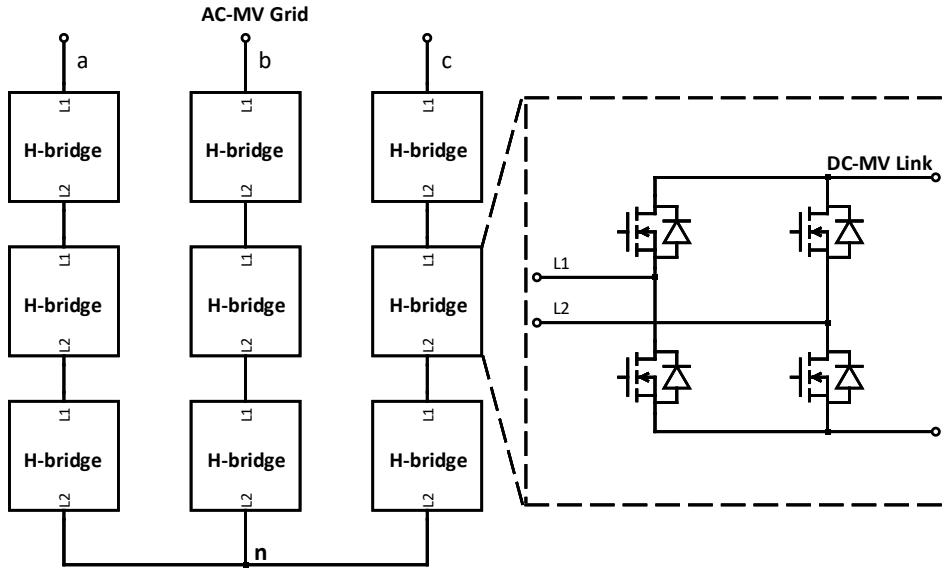


Figure 2.2: The block scheme of star-connected CHB converter

returns nine output signals where each of them control one bridge. Therefore the basic switching module to average is one H-bridge (Figure 2.3).

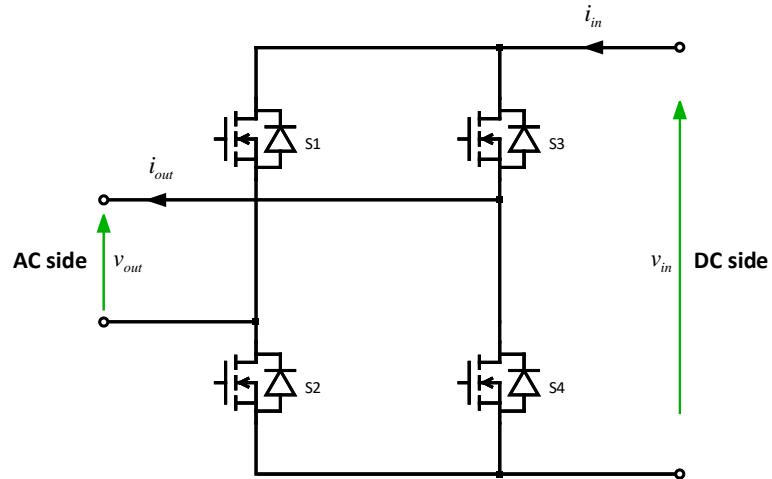


Figure 2.3: Detailed model of H-bridge

Based on the theory described in the literature Large-Signal average model of H-bridge can be represented by one controlled voltage source from the AC side and one controlled current source from the DC side of the bridge (Figure 2.4) [8].

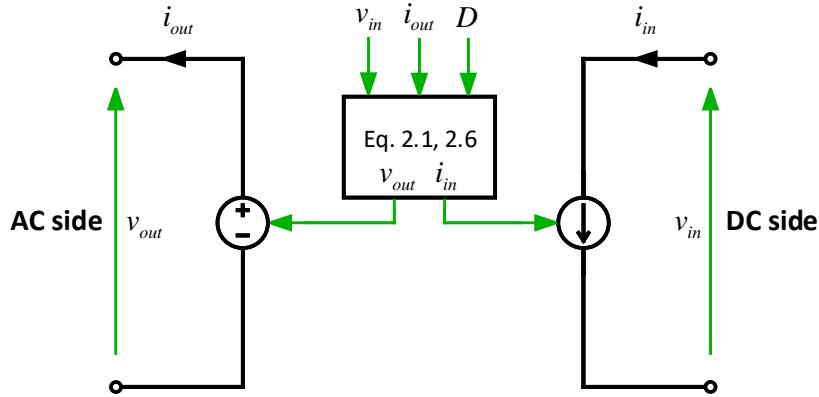


Figure 2.4: Averaged model of H-Bridge

In the detailed model (Figure 2.3) the modulator causes switching of transistors S1,S2,S3 and S4 determining the average value of the AC voltage v_{out} during the each PWM period T_s based on DC voltage v_{in} and control signal D :

$$v_{out} = v_{in}D \quad (2.1)$$

This makes the voltage value of the controlled voltage source easy to determine by multiplying the control signal D and measured voltage DC voltage v_{in} .

The dc-side represented by the controlled current source is derived using the principle of power balance. The considered model assumes that all the losses in H-bridge are negligible. That means the power on the input side P_{in} has to be equal to the power on the output side P_{out} :

$$P_{in} = P_{out} \quad (2.2)$$

$$v_{in}i_{in} = v_{out}i_{out} \quad (2.3)$$

$$i_{in} = \frac{v_{out}i_{out}}{v_{in}} \quad (2.4)$$

Based on Eq. 2.1:

$$i_{in} = \frac{v_{in} D i_{out}}{v_{in}} \quad (2.5)$$

$$i_{in} = i_{out} D \quad (2.6)$$

It can be noticed that the AC voltage cannot exceed the v_{dc} and be less than $-v_{dc}$, therefore the value of control signal D must be in the range $< -1; 1 >$. Thus, the average model of H-bridge should also contain a saturation block to limit the control signal D value.

The last step of creating the average model of this part of the ST is to replace all nine H-bridges from the detailed models (Figure 2.2) into average models (Figure 2.4). The final average model of star-connected CHB converter is presented in Figure 2.5.

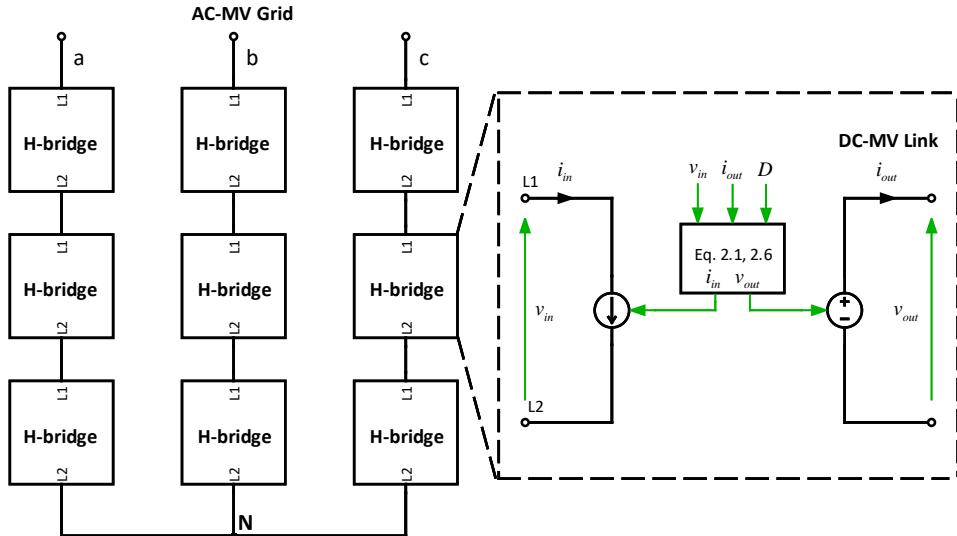


Figure 2.5: Averaged model of star-connected CHB converter

2.3 Averaged model of isolated DC-MV/DC-LV converter

The DC-MV/DC-LV part of the ST contains three identical modules in its structure (Figure 2.1). One module uses three H-bridges, each connected

to one of the three high-frequency transformers while the secondary winding triangular connected of these transformers are linked with three legs converter from the LV side (Figure 2.6) [9].

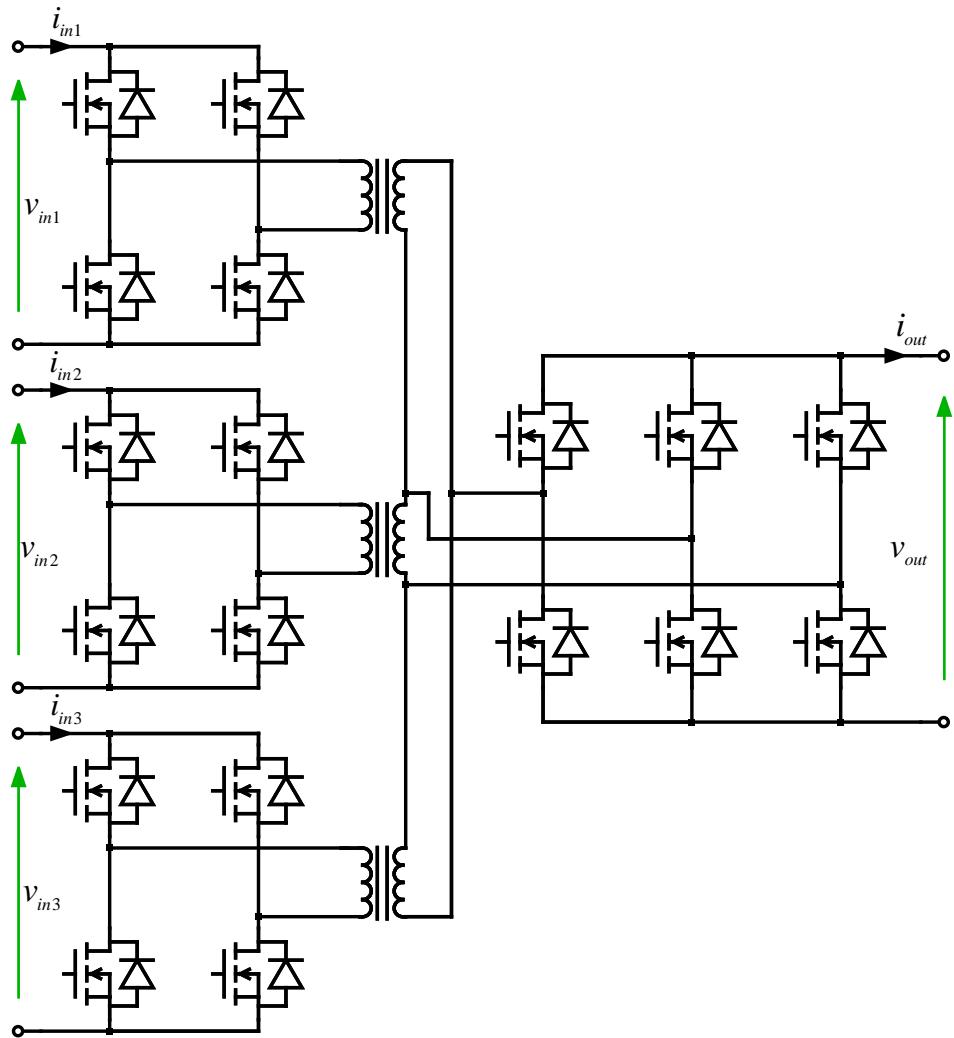


Figure 2.6: One module (One H-bridge for each phase) of the DC-MV/DC-LV part of ST

Due to the fact that the considered structure of an isolated DC/DC converter is not typical, therefore firstly there a typical Dual Active Bridge (DAB) converter (Figure 2.7) is averaged because the process of its averag-

ing is widely described in the literature. Then, based on the average model of typical DAB, the process of averaging one module and then the whole converter is carried out.

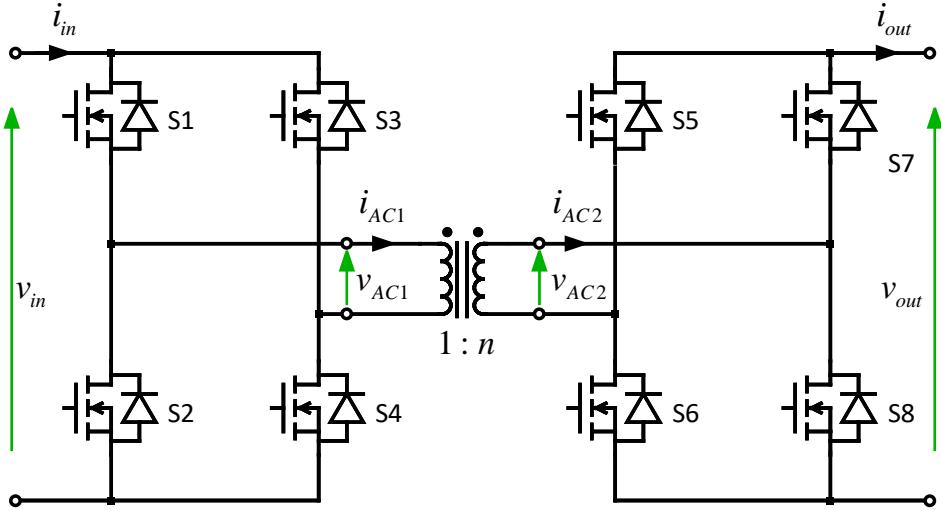


Figure 2.7: Topology of DAB converter

The control algorithm of DC-MV/DC-LV part of ST described in Section 3.2 considered the Phase Shift Modulation (PSM) which is the most popular modulation method in isolated DC/DC converters with high-frequency transformer [10]. In the basic form of the modulation, the rectangular voltage waveforms are applied for the secondary and primary windings of the high-frequency transformer, with a 50% duty cycle and the same frequency.

To illustrate DAB operation with PSM in a more clear way, each of the H-bridges can be replaced with a rectangular voltage source with amplitude successively v_{in} , v_{out} and 50% duty cycle and also representing the transformer as a linear inductance taking into account transformers n-ratio what is presented in Figure 2.8 [10].

The considered model is lossless and also the transformer is linear and its magnetizing inductance and parasitic capacitances are neglected.

Based on the lossless DAB model (Figure 2.8) it is possible to determine the power flow by the equation [11]:

$$P = \frac{v_{in}v_{out}}{2nf_s L_{eq}\pi^2} \phi(\pi - \phi) \quad (2.7)$$

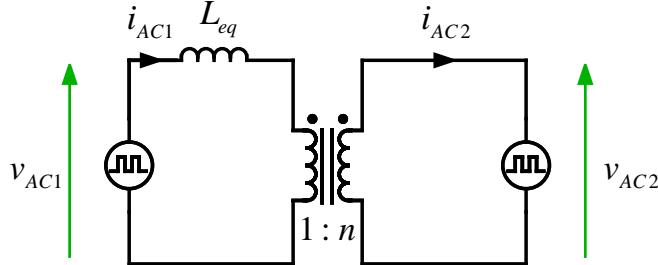


Figure 2.8: Lossless DAB model

where v_{in} , v_{out} are the DAB input and output voltages, ϕ is the phase shift between v_{AC1} and v_{AC2} voltage waveforms, n is the turns ratio of the transformer, f_s is the switching frequency, and L_{eq} is the leakage inductance referred to the input side of the converter.

$$L_{eq} = L_1 + \frac{L_2}{n^2} \quad (2.8)$$

The simple DAB model (Figure 2.8) shows that averaging of these voltage signals for the period T_s is not able to take into account the influence of the phase shift ϕ which has a huge impact on the power flow. Therefore, the averaging method present in Section 2.2 does not give the opportunity to create the correct model.

The used method of the DAB averaging based on literature [11]. It ignores the impact of the magnetizing inductance and core losses of the high-frequency transformer but considers the winding resistances R_{l1} and R_{l2} , leakage inductances L_{l1} and L_{l2} , and the turn-on resistance R_s of the transistors. The averaging process will be carried out with the model presented in Figure 2.9.

The R_{eq} and L_{eq} are the equivalent resistance and inductance respectively referred to the input side of the converter which are described by the equation 2.8 and:

$$R_{eq} = R_1 + 2R_s + \frac{R_1 + 2R_s}{n^2} \quad (2.9)$$

The DAB average model is represented by two current sources related to each other with appropriate equations to simulate the DAB's dynamics but only from the point of view its input and output (Figure 2.10) [11]. Moreover, the average model allows influencing its behaviour by providing a phase shift

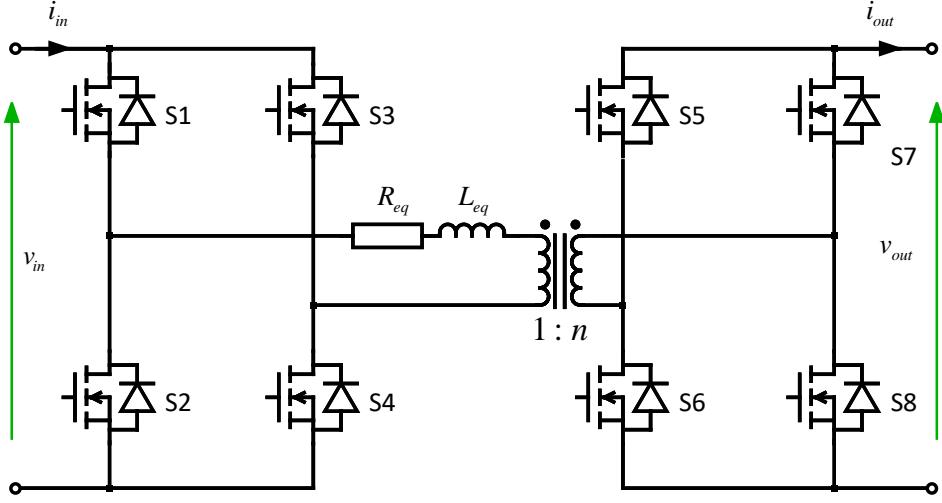


Figure 2.9: Considered DAB model

signal to its input (Figure 2.10). The approach does not allow for full insight into the transformer's signals, as in the detailed model, but fortunately, from the control algorithm point of view, this method is sufficient.

Based on the literature the average model of DAB links voltages and currents values of input and output with the possibility of affecting their behaviour with values of phase shifts using equations below [11]:

$$I_{t1} = \frac{v_{in} - v_{out} + 2v_{out}e^{-\frac{R_{eq}}{L_{eq}}(T-dT)} - (v_{in} + v_{out})e^{-\frac{R_{eq}}{L_{eq}}T}}{R_{eq}(1 + e^{-\frac{R_{eq}}{L_{eq}}T})} \quad (2.10)$$

$$I_{t2} = \frac{v_{in} + v_{out} - 2v_{in}e^{-\frac{R_{eq}}{L_{eq}}dT} + (v_{in} + v_{out})e^{-\frac{R_{eq}}{L_{eq}}T}}{R_{eq}(1 + e^{-\frac{R_{eq}}{L_{eq}}T})} \quad (2.11)$$

$$\begin{aligned} i_{in} = & \frac{(v_{in} + v_{out})dT + (v_{in} - v_{out})(1 - d)T}{TR_{eq}} + \\ & + \frac{L_{eq}(I_{t1} + \frac{v_{in}+v_{out}}{R_{eq}})(e^{-\frac{R_{eq}}{L_{eq}}dT} - 1)}{TR_{eq}} + \\ & + \frac{L_{eq}(\frac{v_{in}-v_{out}}{R_{eq}} - I_{t2})(e^{-\frac{R_{eq}}{L_{eq}}(T-dT)} - 1)}{TR_{eq}} \end{aligned} \quad (2.12)$$

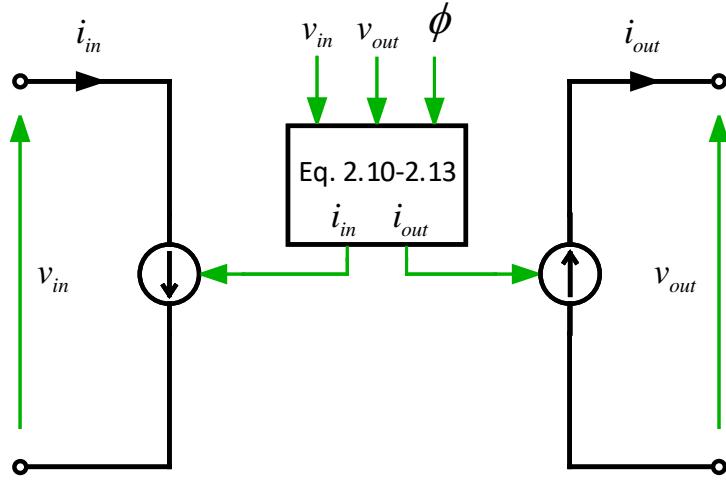


Figure 2.10: Average DAB model

$$\begin{aligned}
 i_{out} = & \frac{-(v_{in} + v_{out})dT + (v_{in} - v_{out})(1 - d)T}{nTR_{eq}} \\
 & - \frac{L_{eq}(I_{t1} + \frac{v_{in} + v_{out}}{R_{eq}})(e^{-\frac{R_{eq}}{L_{eq}}dT} - 1)}{nTR_{eq}} + \\
 & + \frac{L_{eq}(\frac{v_{in} - v_{out}}{R_{eq}} - I_{t2})(e^{-\frac{R_{eq}}{L_{eq}}(T-dT)} - 1)}{nTR_{eq}}
 \end{aligned} \quad (2.13)$$

where the I_{t1} and I_{t2} are the peak values of the transformer current, T is switching period and $dT = \frac{\phi}{2\pi}T$. It means that the model (Figure 2.10) reads the v_{in} , v_{out} and ϕ values in each simulation time step. Then based on them, it determines I_{t1} and I_{t2} . Finally, the model returns currents values i_{in} and i_{out} .

In order to create the average model of the module presented in Figure 2.6 it is enough to connect three modules of the average DAB model as it is shown in Figure 2.11. The final step is to combine three average modules to create the average model of DC-MV/DC-LV part of ST (Figure 2.11).

It is worth adding that in the literature there are also others DAB average models [12], [13]. One of the considered models uses the first harmonic approximation (FHA) method [12]. Its main assumption is to take into

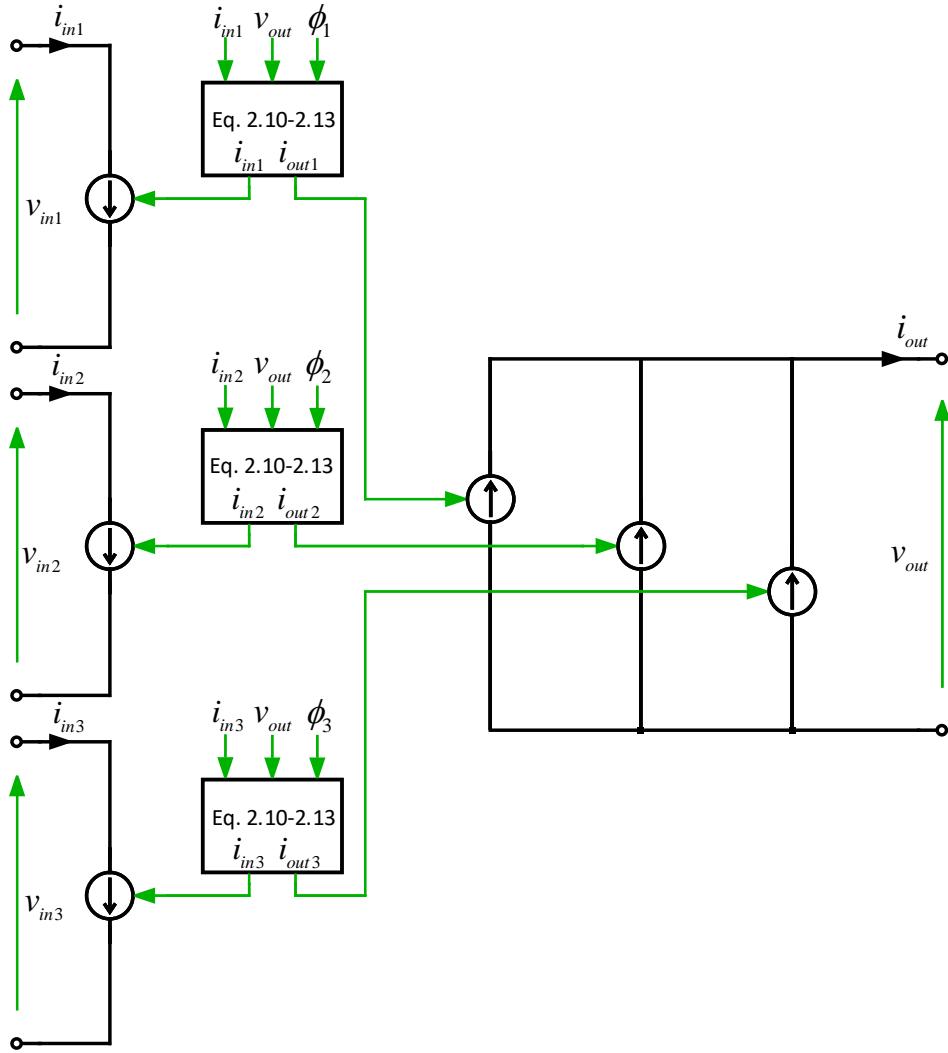


Figure 2.11: Averaged model of one module of the DC-MV/DC-LV converter

account only the first harmonic of these two rectangular signals and then adequately rescale the amplitudes of these signals so that the power flow is the same as for a rectangular signal at a given phase shift. This approach significantly shortened the time of simulation, however, this solution was

finally rejected due to the much different model dynamics compared with detailed model dynamics and the necessity of correcting the value of the first harmonic amplitude to receive the same power flow for the same phase shift value as for the detailed model in the steady state.

2.4 Averaged model of modular 4 leg LV-DC/LV-AC T-Type converter

The considered DC-LV/AC-LV stage of the ST consists of four modules connected in parallel what is shown in Figure 2.12.

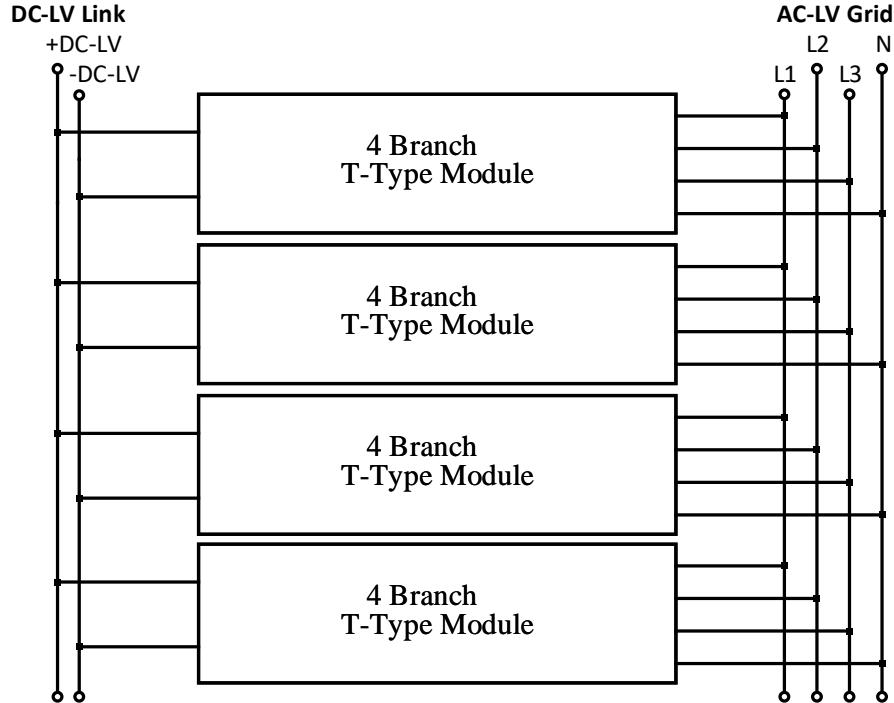


Figure 2.12: DC-LV/AC-LV stage of the ST

The structure of one module is composed of four T-branches the LC-output filter and two capacitors of DC-link (Figure 2.13).

The averaging procedure of DC-LV/AC-LV stage of the ST is very similar to averaging star-connected CHB converter described in Section 2.2. The first

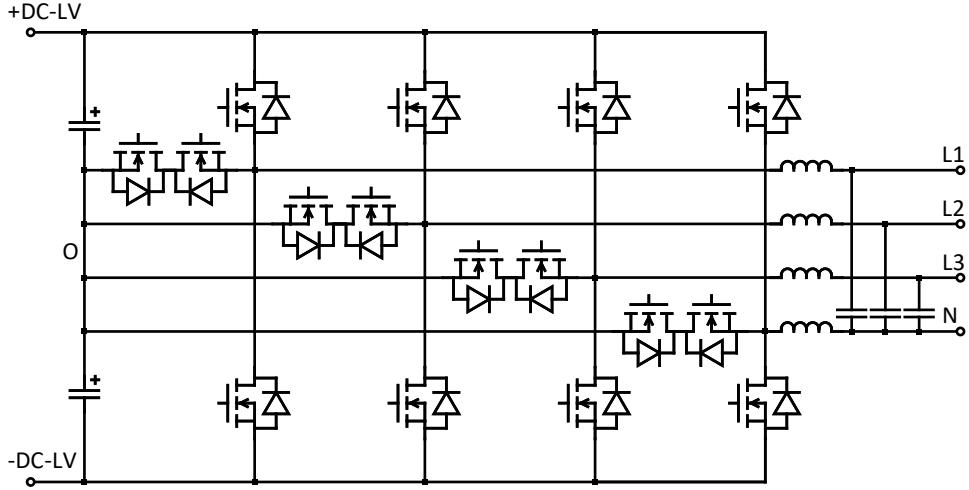


Figure 2.13: Four leg T-Type module

step is to define a basic module from which it is possible to create the whole considered power stage of ST.

The main requirement which the average model should meet is the ability to test the control algorithm of this stage of ST described in Section 3.3. The control strategy returns four control signals as the duty cycle values D for one module. Each of the signal determine the average value of the branch voltage v_{out} between terminals O and A (Figure 2.14) of each T-Type branch for the T_s period. Then an average value of the voltage can be formulated as follows [14], [15], [16]:

$$\begin{cases} v_{out} = Dv_{in1}, & \text{for } D \geq 0 \\ v_{out} = Dv_{in2}, & \text{for } D < 0 \end{cases} \quad (2.14)$$

where v_{in1} and v_{in2} are average voltages across capacitors C1 and C2 , respectively.

Therefore, the basic module in this part of the ST is one T-Type branch (Figure 2.14). From the OA terminals point of view, the average model determine the voltage value described by Eq. 2.15. Therefore from the side of OA terminals the average model can be represented as a controlled voltage source. Due to the fact that for $D > 0$ the output energy is supplied from C1 and for $D < 0$ the output energy is supplied from C2, it causes that the detailed model shows an uneven voltage distribution on the capacitors. To simulate these voltage fluctuations across the capacitors, it is necessary

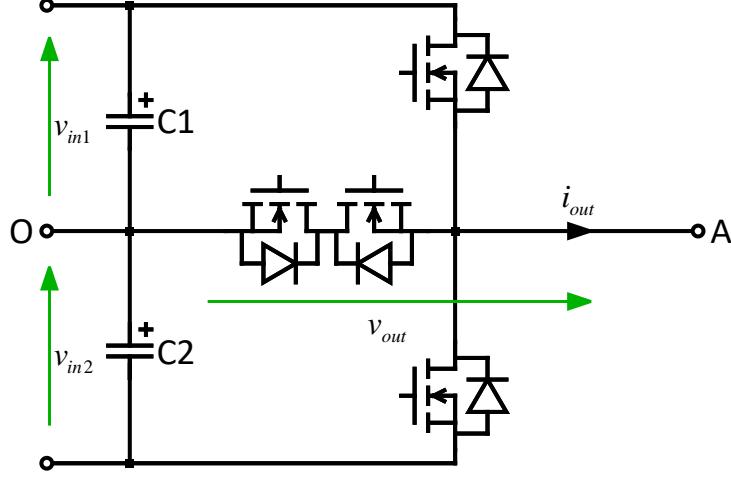


Figure 2.14: Detailed model of T-type branch

to dedicate two controlled current sources for each T-Type branch from the DC-side point of view. The average current value of these controlled current sources is determined based on the power balance equation. For $D > 0$, power is provided by the capacitor C1 and $D < 0$ power is provided by the capacitor C2. The average current value may be calculated by equations:

$$\begin{cases} i_{in1} = Di_{out} \\ i_{in2} = 0 \end{cases}, \text{ for } D \geq 0$$

$$\begin{cases} i_{in1} = 0 \\ i_{in2} = Di_{out} \end{cases}, \text{ for } D < 0 \quad (2.15)$$

The complete model of T-Type branch is presented in Figure 2.15. The construction of the entire average model of this stage consists only in the replacement of each detailed T-Type branch (Figure 2.14) with its average model (Figure 2.15).

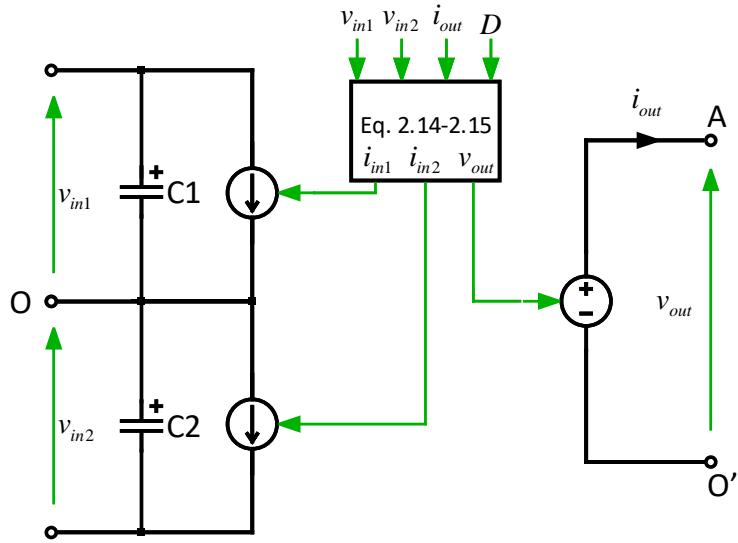


Figure 2.15: Averaged model of T-Type branch

2.5 Conclusions

The considered ST forms a large converter, but thanks to its modular structure it is possible to create its average model by averaging only three modules on which the entire ST power circuit is made while meeting the requirements of the control strategy. Therefore, the process of developing a complete model of average ST can be realized by modelling each stage separately and then combining them in the way presented in the Figure 2.1.

Chapter 3

Basic control methods of ST

3.1 Control algorithm of AC-MV/DC-MV part od ST

One of the most popular AC/DC converter control algorithm is Voltage Oriented Control (VOC) [17]. The VOC is characterized by simplicity due to the use of very common Proportional Integral (PI) controller. The overriding task of the algorithm is to maintain one DC-bus voltage at the reference value.

In contrast to the classical VOC the control algorithm of AC-MV/DC-MV converter must regulate not one but nine separate MV-DC-links each corresponding to one H-bridge as shown in Figure 3.1.

Therefore, it is decided to use the control strategy related to each phase separately which includes three H-bridges connected in series [18], [19]. The control algorithm with cascaded structure regulator is shown in Figure 3.2.

The external control loop is responsible for maintaining the value of three DC-links voltages $v_{MVDC,x}$ (Eq. 3.1) in the considered x phase to the reference voltage level $v_{(MVDC,x)}^*$, where $x \in \{a, b, c\}$.

$$v_{MVDC,x} = \frac{1}{3}(v_{MVDC,x1} + v_{MVDC,x2} + v_{MVDC,x3}) \quad (3.1)$$

The voltage control is based on PI controller whose output determines the reference amplitude value of the MV-AC phase current $I_{MV,x}^*$. The internal loop controls the phase current $i_{MVAC,x}$ with a Proportional-Resonant (PR) controller. The reference value of the current loop $i_{MVAC,x}^*$ is determined by multiplication the reference amplitude of the phase current $I_{MV,x}^*$ and $\cos\alpha_x$, where α_x is an angle of the main harmonic of the phase voltage $v_{MVAC,x}$ waveform. The output of the inner control loop is the duty cycle value d_x . There is no modulator block in Figure 3.2 but for the average model

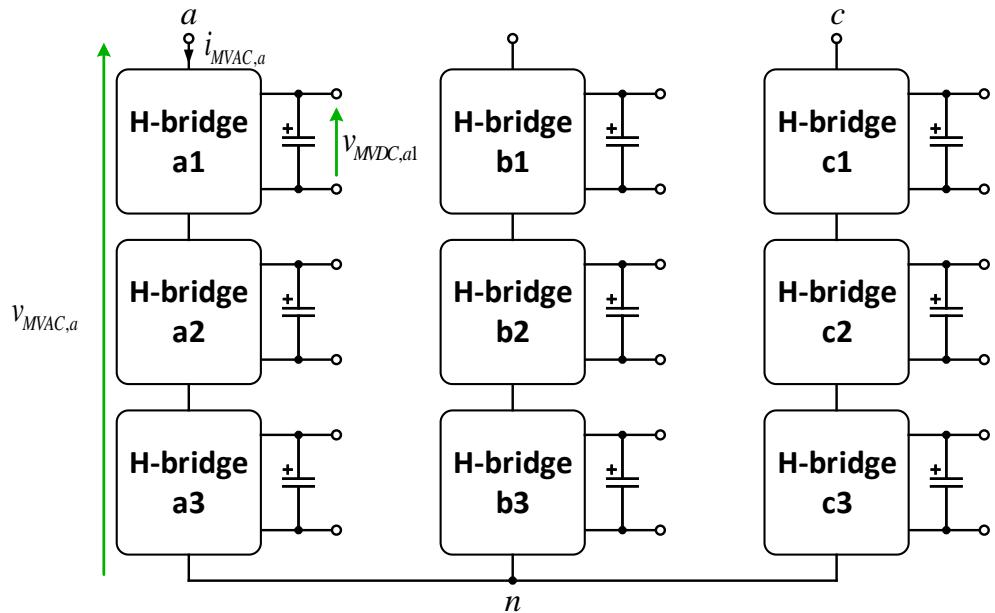


Figure 3.1: Star-connected CHB converter with marked signals

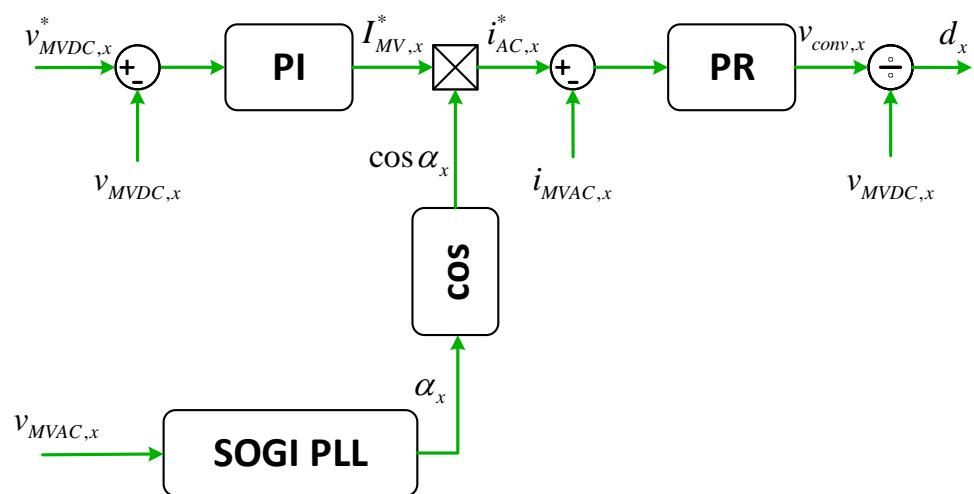


Figure 3.2: The control algorithm of one phase CHB converter

application, the duty cycle value is enough to verify the control algorithm (Section 2.2). Due to the fact that the considered stage of ST model is simplified, the algorithm does not include the problem of balance between voltages $v_{MVDC,x1}$, $v_{MVDC,x2}$ and $v_{MVDC,x3}$. Therefore, each H-bridge per x phase is controlled by the same d_x signal (Eq. 3.2).

$$d_{x1} = d_{x2} = d_{x3} = d_x \quad (3.2)$$

The problem of possible unbalancing of the voltages in the considered model is not visible, because the capacity of each of the nine DC-links is identical.

The angle α_x is determined based on Second-Order Generalized Integrator (SOGI) and Phase-Locked Loop (PLL) algorithms [20]. Their structure is presented in Figure 3.3.

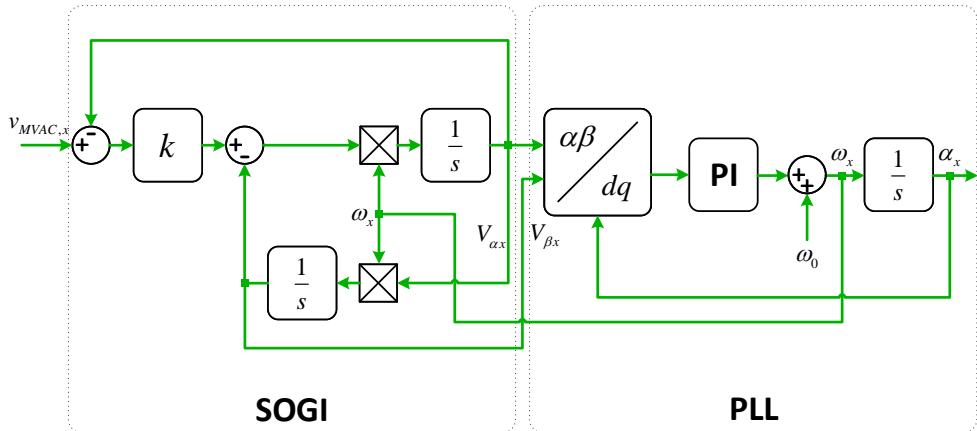


Figure 3.3: SOGI-PLL scheme

It consists of a separate SOGI area which acts as a filter that lets the signal of ω_x pulsation pass returning the first harmonic voltage in $\alpha - \beta$ stationary reference frame. Therefore the SOGI outputs are the first harmonic voltage $V_{\alpha x}$ and a virtual beta voltage $V_{\beta x}$ shifted by 90 degrees relative to the voltage $V_{\alpha x}$ and with the same amplitude as the voltage $V_{\alpha x}$. The k block is a gain coefficient which is used to determine the optimal dynamic and accuracy of SOGI. Then, the signals $V_{\alpha x}$ and $V_{\beta x}$ are the input of the PLL block where at the beginning they are transformed into components in the dq synchronous reference frame (Eq. 3.3) based on the α_x angle which is the feedback signal [20].

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\alpha_x) & \sin(\alpha_x) \\ -\sin(\alpha_x) & \cos(\alpha_x) \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (3.3)$$

After that the V_q component is an input of the PI controller whose task is returned such pulsation value to brought the V_q component to zero in the feedback loop. Moreover, the estimated pulsation value ω_0 is added to the PI regulator output, so that the controller does not have to start from zero value, but it only has to correct the pulsation value. This makes the PLL block achieve a steady state much faster with milder transient states. Finally, the ω_x pulsation is integrated in order to obtain α_x angle which is used to determine the $i_{MVAC,x}^*$ current value.

To sum up, the control algorithm presented in Figure 3.2 involves controlling three bridges within one phase. This means that the entire control strategy of this part of ST returns nine duty cycle values which are the input of the average model of star-connected CHB converter described in Section 2.2.

3.2 Control algorithm of DC-MV/DC-LV part od ST

This section deals with the control strategy of DC-MV/DC-LV part of ST description. The full structure of the considered part of ST contains three DC/DC modules. The construction of one module is presented in Figure 2.6. This part of ST let to transfer energy between nine MV-DC-links and one LV-DC-link which is shown in Figure 3.4 [9], [21].

The main goal of the control algorithm is maintaining the v_{LVDC} voltage value to the v_{LVDC}^* reference voltage level. In order to fulfil this aim, the control structure shown in the Figure 3.5 is used. This control includes one outer loop which maintains the LV-DC voltage value to the reference level using the PI controller. Then the output signal from that loop is the reference current value of the MV-DC-links (Figure 3.4) for each of the nine internal control loops. Finally, the all of the inner loops return the nine phase shift value, three per each module.

In the detailed model, the values of phase shifts are the inputs of the modulator block which on the LV-DC side controls the two-level converter with three branches by fixed PWM signal with 50% duty cycle. Whereas each bridge on the MV-DC side is controlled with a 50% fill but the phase shift value is changed in the time in relation to the signals controlling the inverter on the LVDC side. In the case of the average model, three phase shifts are assigned to each of the three modules, without a modulator.

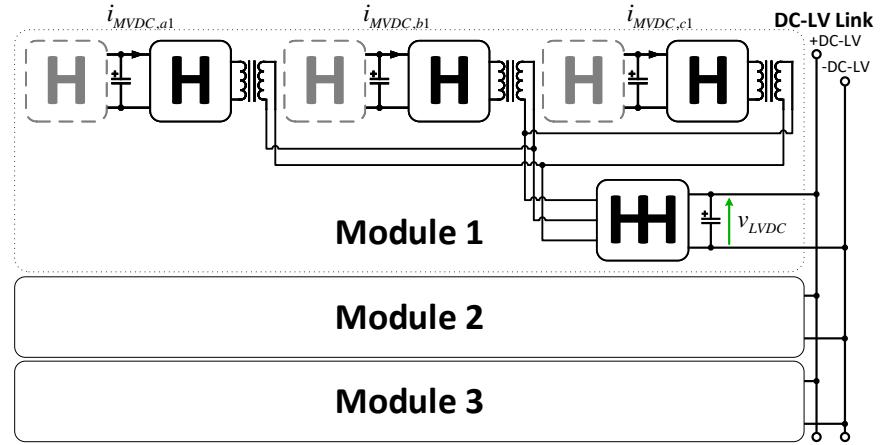


Figure 3.4: Isolated DC-MV/DC-LV converter with marked signals

To sum up, for both models, a conventional PSM is applied with the difference that the impact of this modulation on the average model is taken into account in the construction of the model itself (Section 2.3) [11].

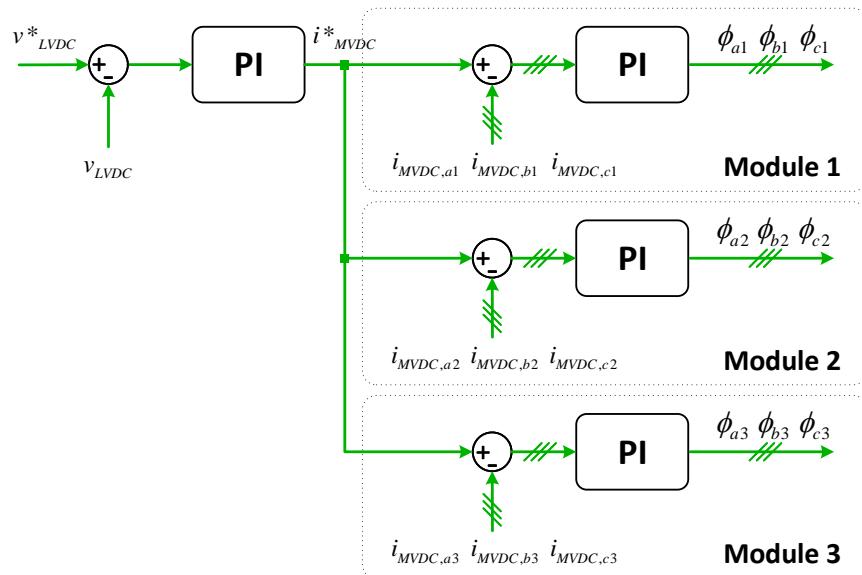


Figure 3.5: DAB control strategy scheme

3.3 Control algorithm of DC-LV/AC-LV stage

Considered control strategy of DC-LV/AC-LV stage (Figure 3.6) assumes that the first T-Type module is responsible for the voltage control in the LV-AC grid, while the other three modules are controlling the current to distribute the active power to all four modules.

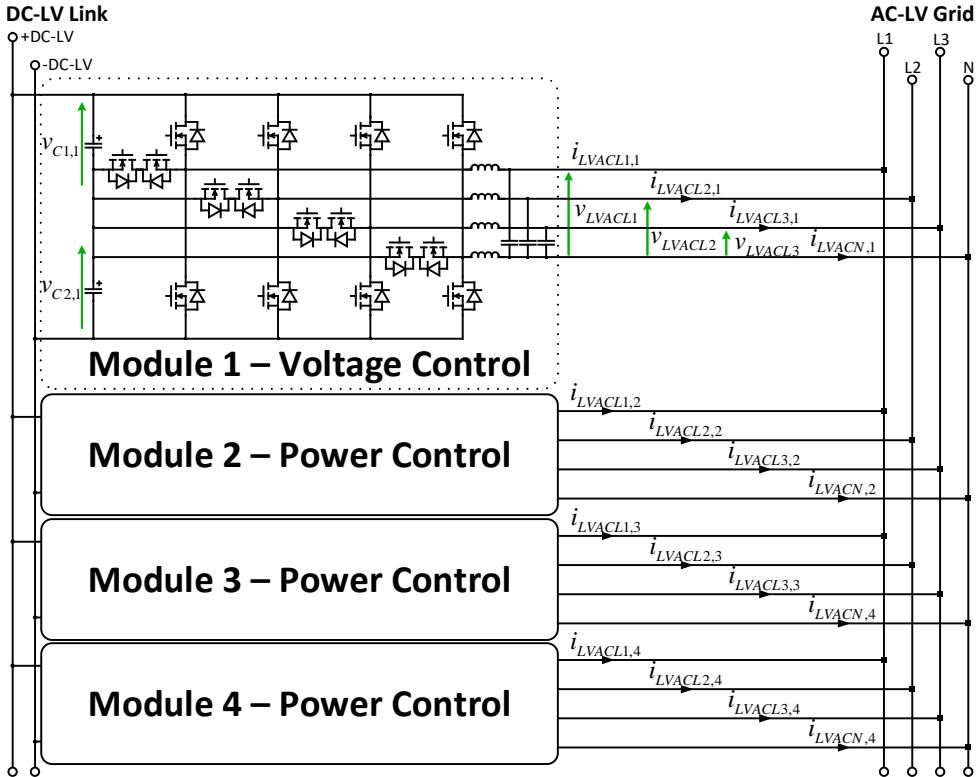


Figure 3.6: DC-LV/AC-LV stage with marked signals

The control algorithm of the first T-Type module with cascaded structure is presented in Figure 3.7 [22]. Due to the fact that the reference voltages and currents have a sinusoidal waveform the PR controllers are used.

The outer loop of the control is responsible for maintaining the voltage $v_{LVACz,1}$ at the reference value $v_{LVACz,1}^*$, where $z \in \{L1, L2, L3\}$. The outputs of the voltage control are the three reference currents values $i_{LVACz,1}^*$ being an input of inner loop responsible for current control. Seeing that each T-Type module is a four-leg converter, the reference current in the module the fourth N-wire is determined by Kirchhoff's law based on three reference

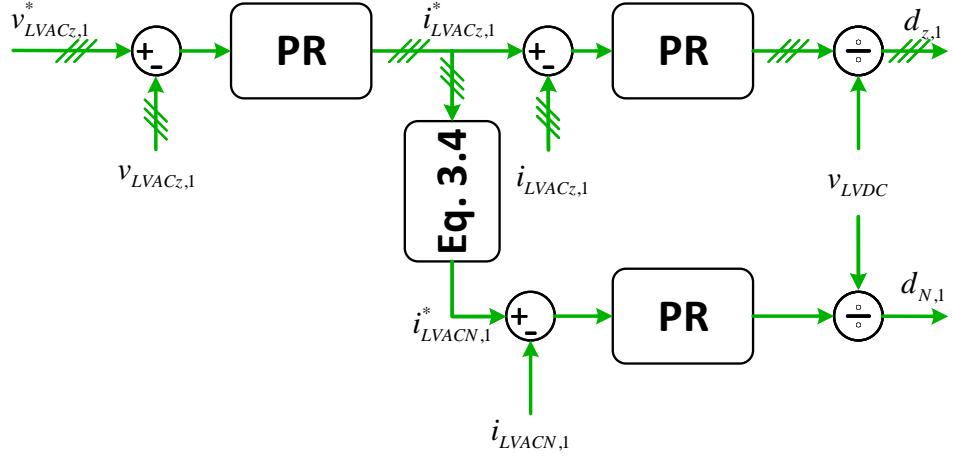


Figure 3.7: The voltage control scheme of first T-Type module

currents:

$$i_{LVACN,m}^* = -(i_{LVACL1,m}^* + i_{LVACL2,m}^* + i_{LVACL3,m}^*) \quad (3.4)$$

where m is the number of module. Finally, the current control returns the duty cycle values which are the inputs of the average model described in Section 2.2.

The control strategy of the other modules is shown in Figure 3.8. The control is very similar to the control of first module but instead of the external voltage loop there is a block of reference current value $i_{LVACz,m}^*$ estimation.

In the first step of the control the active power of each phase in each T-Type module is calculated based on equation [23]:

$$P = \frac{v_\alpha i_\alpha + v_\beta i_\beta}{2} \quad (3.5)$$

where the v_α, i_α are the main harmonic value of the voltage and current signals, and v_β, i_β are the v_α, i_α signals shifted by 90 degrees. The $v_\alpha, v_\beta, i_\alpha, i_\beta$ signals in each phase in each T-Type module are generated based on SOGI algorithm (Section 3.1). After that the average value of the active power $P_{avg,z}$ in each phase is determined. Finally, the average active power $P_{avg,z}$ is divided by the reference voltage amplitude V_{LVACz}^* and then multiply by $\cos\alpha_z^*$ of the reference voltage $v_{LVACz,1}^*$ which returns the reference current value $i_{LVACz,m}^*$. The rest of the algorithm is the same as in the case control of the first module.

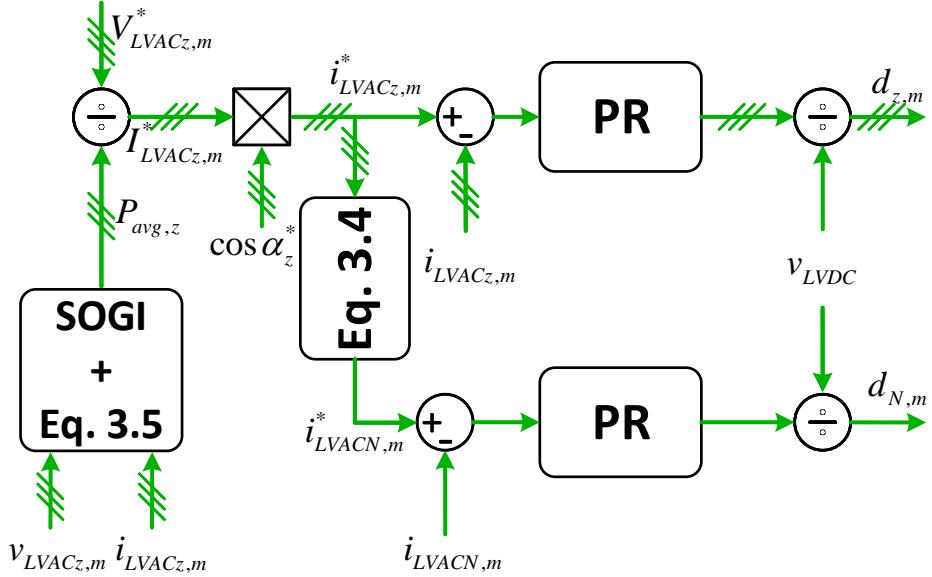


Figure 3.8: The current control scheme of other T-Type module

The presented algorithm is in its basic form without the harmonic compensation.

3.4 Load Identification Algorithms for LV side of ST

The way in which voltage amplitude and frequency of LV grid affect power and current drawn from the ST strictly depends on the type of loads connected to the ST. Therefore, an important issue from the ST power management point of view is the load identification algorithms.

3.4.1 Load models

In the literature, two load models are usually presented [24]. The first based on the description of the active and reactive power of the load as a quadratic voltage function. The powers are expressed by the equations:

$$P = P_1 \left(\frac{V}{V_0} \right)^0 + P_2 \left(\frac{V}{V_0} \right)^1 + P_3 \left(\frac{V}{V_0} \right)^2 \quad (3.6)$$

$$Q = Q_1 \left(\frac{V}{V_0} \right)^0 + Q_2 \left(\frac{V}{V_0} \right)^1 + Q_3 \left(\frac{V}{V_0} \right)^2 \quad (3.7)$$

where P_1 and Q_1 are the sums of active and reactive power of loads which are independent to voltage amplitude (constant power), P_2 and Q_2 are the sums of active and reactive power of constant current loads, P_3 and Q_3 are sums of active and reactive power of loads which have a feature of linear impedance. All the power values P_1 , P_2 , P_3 , Q_1 , Q_2 and Q_3 are determined for the nominal voltage amplitude V_0 .

The second common load model is the description of the load active and reactive power by the equations:

$$P = P_0 \left(\frac{V}{V_0} \right)^{K_p} \quad (3.8)$$

$$Q = Q_0 \left(\frac{V}{V_0} \right)^{K_q} \quad (3.9)$$

where

$$P_0 = P_1 + P_2 + P_3 \quad (3.10)$$

$$Q_0 = Q_1 + Q_2 + Q_3 \quad (3.11)$$

whereas K_p and K_q are the sensitivities of active and reactive power to voltage.

In the literature an approximate values of K_p and K_q are determined based on (3.6), (3.7) and they take the following forms [24]:

$$K_p \approx \frac{P_1 \times 0 + P_2 \times 1 + P_3 \times 2}{P_1 + P_2 + P_3} \quad (3.12)$$

$$K_q \approx \frac{Q_1 \times 0 + Q_2 \times 1 + Q_3 \times 2}{Q_1 + Q_2 + Q_3} \quad (3.13)$$

The approximations (3.12) and (3.13) are correct, assuming that the effective value of the voltage applied to the loads is very close to V_0 value. Based on the above simplification, it could be concluded that when the direction of power flow of each type of load is the same to ST then sensitivity value $K_p \in <0; 2>$. The same applies to reactive power based on the simplification (3.13). When the signs of Q_1 , Q_2 and Q_3 are the same then $K_q \in <0; 2>$.

In addition, in the literature, the load model described by (3.6) and (3.7) can be extended by the sensitivities of active and reactive power to frequency K_{fp} and K_{fq} [25]:

$$P = P_1 \left(\frac{V}{V_0} \right)^{K_p} \left(1 + K_{fp} \frac{(f - f_0)}{f_0} \right), \quad (3.14)$$

$$Q = Q_1 \left(\frac{V}{V_0} \right)^{K_q} \left(1 + K_{fq} \frac{(f - f_0)}{f_0} \right), \quad (3.15)$$

where f_0 is the nominal frequency value. The model described by the equation above is more complete because the power of the real load is dependent on both voltage and frequency. Therefore, the algorithm used to Load Sensitivity Identification presented in this article is based on the model determined by (3.14) and (3.15).

All models have to be applied separately for each phase, because when the load is asymmetrical, the P_1 , P_2 , P_3 , Q_1 , Q_2 , Q_3 , K_p , K_{fp} , K_q and K_{fq} coefficients for the respective phases are different and they can change independently.

3.4.2 Accurate Load Identification

The proposed algorithm of Accurate Load Identification (ALI) assumes that the active and reactive power of the load is described by equations (3.6) and (3.7).

The concept of the ALI is based on a calculation of the first and second power derivative with respect to the voltage amplitude by intentionally changing the reference value. These calculations are based on the measurements of phase voltages and currents.

Calculating the value of the second derivative from below equations, the value of active and reactive powers P_3 , Q_3 can be determined:

$$\frac{d^2P}{dV^2} = P_3 \frac{2}{V_0^2} \quad (3.16)$$

$$P_3 = \frac{1}{2} \frac{d^2P}{dV^2} V_0^2 \quad (3.17)$$

$$\frac{d^2Q}{dV^2} = Q_3 \frac{2}{V_0^2} \quad (3.18)$$

$$Q_3 = \frac{1}{2} \frac{d^2Q}{dV^2} V_0^2 \quad (3.19)$$

Then, having information about the value of the first derivative (3.20) and taking into account the calculated values of P_3 and Q_3 , the active and reactive powers P_2 , Q_2 can be calculated:

$$\frac{dP}{dV} = \frac{P_2}{V_0} + P_3 \frac{2V}{V_0^2} \quad (3.20)$$

$$P_2 = \frac{dP}{dV} V_0 - 2P_3 \quad (3.21)$$

$$\frac{dQ}{dV} = \frac{Q_2}{V_0} + Q_3 \frac{2V}{V_0^2} \quad (3.22)$$

$$Q_2 = \frac{dQ}{dV} V_0 - 2Q_3 \quad (3.23)$$

The last stage of identification is the calculation of the active and reactive powers P_1 , Q_1 which values are obtained from the power balance equations:

$$P_1 = P_0 - P_1 - P_2 \quad (3.24)$$

$$Q_1 = Q_0 - Q_2 - Q_3 \quad (3.25)$$

The described method has to be implemented numerically determining the first and second derivative of the measured power at the output of the converter relative to the output voltage amplitude and then calculating all powers in accordance with the above equations.

In order to determine derivatives, when the identification is initialized, the power value and the voltage amplitude values are averaged based on n samples. Then the referenced voltage amplitude value is reduced by ΔU and at the moment when the measured value reaches the steady state, the power and voltage amplitude are averaged again. This process is one more time repeated by changing the voltage amplitude reference value to $U_0 + \Delta U$. The voltage changes ΔU cannot exceed the grid standards. An example of the referenced voltage amplitude with the averaging intervals is shown in Figure 3.9.

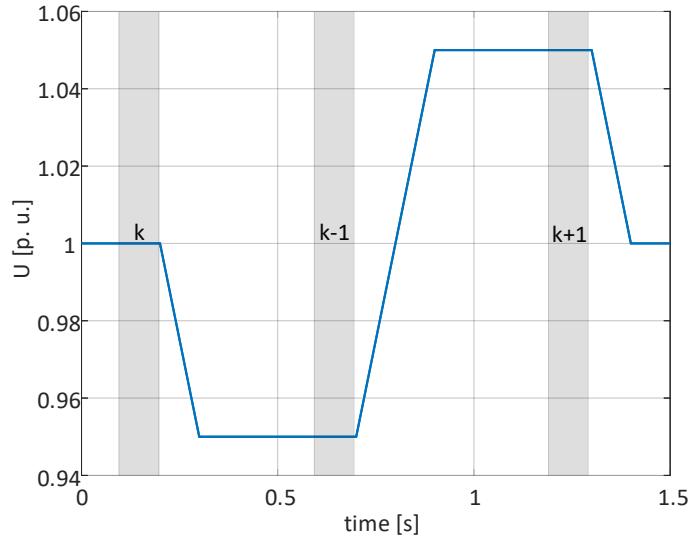


Figure 3.9: An example of the referenced voltage amplitude with marked averaging intervals of measured values.

When all powers and voltage amplitude values have been measured and averaged in moments k , $k-1$, $k+1$, the first and second derivatives of active power P and reactive Q are determined:

$$\frac{dP}{dV} \approx \frac{P_{k+1} - P_{k-1}}{V_{k+1} - V_{k-1}} \quad (3.26)$$

$$\frac{d^2P}{dV^2} \approx \frac{P_{k-1} - 2P_k + P_{k+1}}{(V_{k+1} - V_k)(V_k - V_{k-1})} \quad (3.27)$$

$$\frac{dQ}{dV} \approx \frac{Q_{k+1} - Q_{k-1}}{V_{k+1} - V_{k-1}} \quad (3.28)$$

$$\frac{d^2Q}{dV^2} \approx \frac{Q_{k-1} - 2Q_k + Q_{k+1}}{(V_{k+1} - V_k)(V_k - V_{k-1})} \quad (3.29)$$

Finally, active powers P_1 , P_2 , P_3 and reactive powers Q_1 , Q_2 , Q_3 are calculated specifying which type of loads are connected to the power electronics converter. Taking into account the real dynamic of load changes in the power grid, the described identification method can be repeated at intervals of ten of seconds.

3.4.3 Load Sensitivity Identification

The considered algorithm for Load Sensitivity Identification assumes that the active and reactive power of the loads is described by (3.14) and (3.15). The idea has been presented in [25], [26]. To determine, the K_p , K_{fp} , K_q and K_{fq} coefficients the algorithm makes a controlled voltage or frequency dip and then it measurements the active and reactive power response to this dip. The reference voltage waveform is presented in Figure 3.10.

In contrast to the algorithms described in [25], [26], the sensitivity was determined based on measurements of currents and voltages in steady-state before and after the dip, not in dynamic states when the reference voltage value is changing linearly in time. The sensitivity of K_p , K_{fp} , K_q and K_{fq} are described by the formulas [25]:

$$K_p = \frac{\frac{\Delta P}{P}}{\frac{\Delta V}{V}} \quad K_q = \frac{\frac{\Delta Q}{Q}}{\frac{\Delta V}{V}} \quad K_{pf} = \frac{\frac{\Delta P}{P}}{\frac{\Delta f}{f}} \quad K_{qf} = \frac{\frac{\Delta Q}{Q}}{\frac{\Delta f}{f}}. \quad (3.30)$$

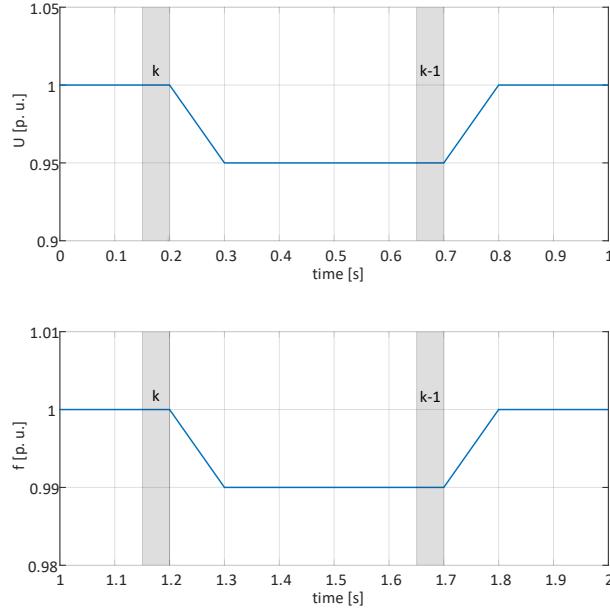


Figure 3.10: An example of the reference voltage amplitude and frequency with marked averaging intervals of measured values.

The numerical representation of (3.30) are determined by equations [25]:

$$K_p = \frac{\frac{P_{k-1} - P_k}{P_k}}{\frac{V_{k-1} - V_k}{V_k}}, \quad (3.31)$$

$$K_q = \frac{\frac{Q_{k-1} - Q_k}{Q_k}}{\frac{V_{k-1} - V_k}{V_k}}, \quad (3.32)$$

$$K_{pf} = \frac{\frac{P_{k-1} - P_k}{P_k}}{\frac{f_{k-1} - f_k}{f_k}}, \quad (3.33)$$

$$K_{qf} = \frac{\frac{Q_{k-1} - Q_k}{Q_k}}{\frac{f_{k-1} - f_k}{f_k}}, \quad (3.34)$$

where the values with the index $k - 1$ are after the steady-state voltage change, whereas the values with the k index are measured before the voltage dip.

It is worth noting that the application of the ALI algorithm may also have additional benefits allowing for a more accurate determination of the sensitivities K_p and K_q , by means of a central difference quotient and not a one-sided difference quotient. This is possible because ALI requires the determination of powers for two additional voltage levels (Figure 3.9). Then the sensitivities are described by the following equations:

$$K_p = \frac{\frac{P_{k-1}-P_{k+1}}{P_{k+1}}}{\frac{V_{k-1}-V_{k+1}}{V_{k+1}}}, \quad (3.35)$$

$$K_q = \frac{\frac{Q_{k-1}-Q_{k+1}}{Q_{k+1}}}{\frac{V_{k-1}-V_{k+1}}{V_{k+1}}}, \quad (3.36)$$

3.4.4 Overload protection control

One of the applications for identifying load sensitivity to voltage and frequency is to protect ST against overload. Two thresholds for the current amplitude value $I_{security}$ and I_{hard} can be distinguished [26]. The algorithm, at the moment of exceeding the $I_{security}$ current value in at least one phase, changes the frequency of the reference voltage in the range acceptable by the standards. Then if the frequency reaches the limit value and the current value in a phase is still greater than $I_{security}$ the reference voltage will change in the range acceptable by the standards. If the current amplitude in at least one phase exceeds the value of I_{hard} , then the ST stop to operate, depriving the recipients of power. In order to be able to determine how to change the frequency and the voltage, the sensitivity of the current to voltage K_i and the sensitivity of the frequency K_{if} is determined based on the K_p , K_{fp} , K_q and K_{fq} according to the following expressions [26]:

$$K_i = (\cos \varphi_0)^2 K_p + (\sin \varphi_0)^2 K_q - 1, \quad (3.37)$$

$$K_{if} = (\cos \varphi_0)^2 K_{fp} + (\sin \varphi_0)^2 K_{fq}, \quad (3.38)$$

where φ_0 is the phase shift between the first harmonic of current and voltage. When $I_{measure} > I_{security}$, the change of the frequency and the voltage value is determined using the equations below:

$$\Delta V = \frac{V_0}{I_{security} K_i} \Delta I, \quad (3.39)$$

$$\Delta f = \frac{V_0}{I_{security} K_{if}} \Delta I, \quad (3.40)$$

$$\Delta I = I_{security} - I_{measure}, \quad (3.41)$$

where ΔI is the required current change, while V_0 is the rated voltage.

Unfortunately, there may be a situation in which loads of individual phases may differ enormously, which may lead to a situation in which a change in frequency or voltage leads to a reduction the current in one phase and at the same time an increase in current in another. In the case of extremely different K_i and K_{if} values in each phase, this problem can be partially reduced by changing the voltage only in the phase in which the current measurement exceeded the $I_{security}$ value thus introducing the asymmetry of the three-phase voltage on the low voltage side. This solution seems correct only when it is certain that there are connected only single phase loads. Then this solution could solve another negative aspect of this method consisting in the fact that the overload of one phase affects the quality of the voltage of other consumers connected to the other phases, which do not overload their phases.

Therefore, this study considers the cases of symmetrical voltages and asymmetric voltages in the LV grid.

3.4.5 Soft Load Reduction Control

Another application of the load identification sensitivity is a Soft Load Reduction Control. It reduce the active power consumption by the loads on the LV grid on demand by the set value γ , where $0 < \gamma < 1$. The required voltage value is determined based on the previous Load Sensitivity Identification [27]. It is formulated by the following transformations:

$$\Delta P = \Delta P_A + \Delta P_B + \Delta P_C = -\gamma (P_A + P_B + P_C), \quad (3.42)$$

$$\Delta P_A = \frac{P_A}{V_0} K_{pA} (V - V_0), \quad (3.43)$$

$$\Delta P_B = \frac{P_B}{V_0} K_{pB} (V - V_0), \quad (3.44)$$

$$\Delta P_C = \frac{P_C}{V_0} K_{pC} (V - V_0), \quad (3.45)$$

then,

$$V = \left(1 + \frac{\Delta P}{(P_A K_{pA} + P_B K_{pB} + P_C K_{pC})}\right) V_0, \quad (3.46)$$

where, ΔP_A , ΔP_B and ΔP_C is the change in active power consumption by each phase, while V is the voltage value after the reduction of the active power of the loads.

One of the applications of this algorithm is to reduce the power consumption of loads imposed by the electric power system in the event of a fault in order to maintain grid stability [27]. It allows increasing the reliability of power supply to the loads, because it only reduces their power consumption, and does not deprive some of them the power. Moreover, this algorithm can be used in the event of a power failure of the ST from the medium voltage grid side, when the power is taken from the energy storage in the DC microgrid. Then, by monitoring the voltage drop in the DC-link, it is possible to relieve the energy storage by reducing the power consumption of loads in the low voltage grid. It allows extending the time of supply of the receivers by the energy store, which also increases reliability in the energy supply for customers because when the time of supplying customers from the energy store is longer, the greater chance that the failure could be removed at that period of time.

Chapter 4

Simulation study

Due to the fact that the Master's thesis is being carried out as a part of the project titled "Highly efficient and fault tolerant SiC-based smart transformer in distributed energy systems" the rated parameters of the average model are consistent with the parameters of the ST prototype which is going to be built in this project. The ST parameters are shown in Table 4.1.

Considered voltage levels are very low due to the capabilities of the laboratory and also because the main goal of the project is to verify the concept of ST topology and control strategy, especially fault control algorithms. All simulation studies were performed in the PLESC simulation software.

4.1 Comparison of detailed and average models of each ST part

The developed average model of three parts of the ST is verified by comparing the simulation signals waveform with the detailed model. All signals which come from the detailed models are averaged over the T_s period to allow comparison of the detailed model and the average model behaviour. Moreover, it is worth adding that in the detailed models simple Pulse Width Modulation (PWM) have been used.

In order to verify the average model of star-connected CHB converter (Figure 2.5) its detailed model has been made (Figure 2.2). Both models from the MV-DC side contain nine power sources, one for each MV-DC link. The power sources simulate the active power required by LV-AC load, which is distributed over nine MV-DC links. The control strategy used in the models has been described in Section 3.1.

Table 4.1: Simulation parameters of ST average model

Description	Value
MV-AC reference voltage V_{MV}	$3 \times 400 \text{ V}$
Rated power S_n	10 kVA
MV-AC grid resistance R_s	$3 \text{ m}\Omega$
MV-AC grid inductance R_s	1 mH
MV-DC capacitors	$9 \times 1.65 \text{ mF}$
Medium DC voltage reference value	$9 \times 270 \text{ V}$
Transformer leakage inductance L_{tr}	$9 \times 10 \mu\text{H}$
Transformer resistance R_{tr}	$9 \times 10 \text{ m}\Omega$
LV-DC Capacitor	3.96 mF
Low DC voltage reference value	270 V
T-type modules DC capacitors	5.28 mF
LC filter inductance	$4 \times 4 \times 0.5 \text{ mH}$
LC filter capacitance	$4 \times 3 \times 10 \mu\text{F}$
Switching frequency f_s	100 kHz
Low AC voltage reference amplitude value	$3 \times 100 \text{ V}$

The comparison between average and detailed model waveforms of considered part of ST is presented in Figure 4.1. To observe the models behaviour in dynamic states, there is a step change of requested power from 5 kW to 10 kW in 0.25 s .

The MV-AC currents $i_{MVAC,x}$ and MV-DC voltages $v_{MVDC,xy}$ are almost the same for both models for the same conditions. That confirms the correctness of the averaged model.

Similarly, the verification process of the DC-MV/DC-LV part of ST is based on a comparison of the detailed and average model behaviour. For this purpose, the two models of one MV-DC/LV-DC module shown in Figure 2.6 has been built. Both models from MV-DC side contain the voltage sources of 270 V with 100 Hz sinusoidal ripple, whereas from the LV-DC side there is a power source which simulates the active power required by LV-AC load.

The control algorithm, which has been applied, is described in Section 3.2 with the difference that it applies only to one module, so there are only three internal loops of current control.

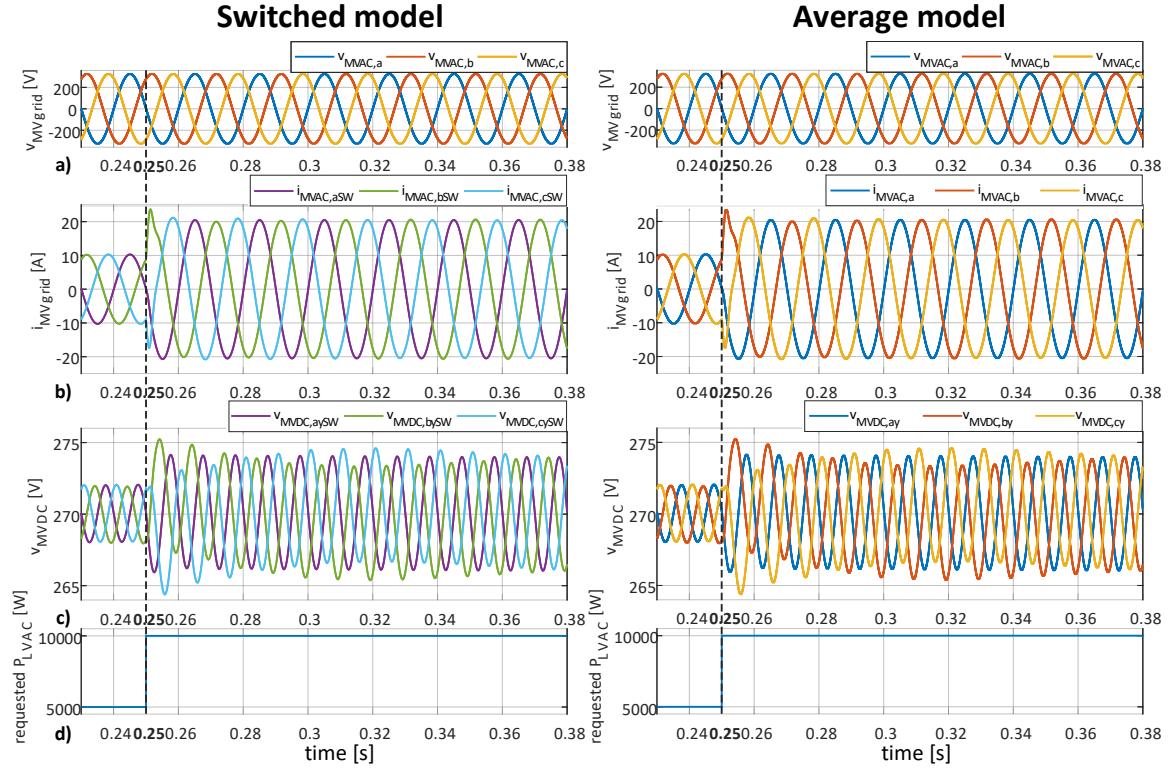


Figure 4.1: Comparison between average and detailed model of star-connected CHB converter

The comparison of results obtained with both models is shown in Figure 4.2. In the 0.25 s there is a step change of required power to show dynamics of both models. There are small differences between the models which are

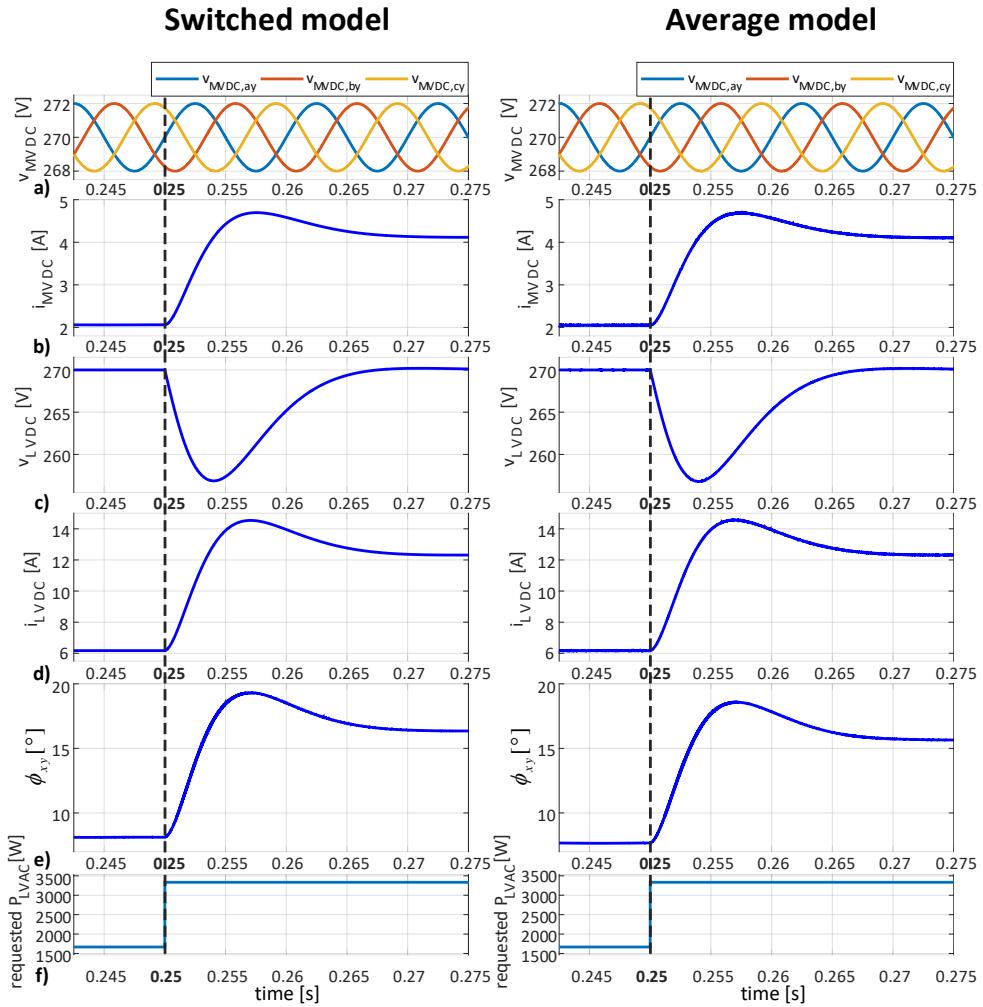


Figure 4.2: Comparison between average and detailed model of one module of the DC-MV/DC-LV part of the ST

mainly visible on the phase shift between square voltages waveform ϕ but the deviation is acceptable.

The third part of the average ST model has been verified only by one T-Type module shown in Figure 2.13. From the LV-DC side, both models have a voltage source of 270 V. The comparison between the average and detailed

model of one T-Type module with voltage control is presented in Figure 4.3. In the 0.25 s there is a load change from symmetrical to asymmetrical conditions. The behaviors of the considered models are almost the same.

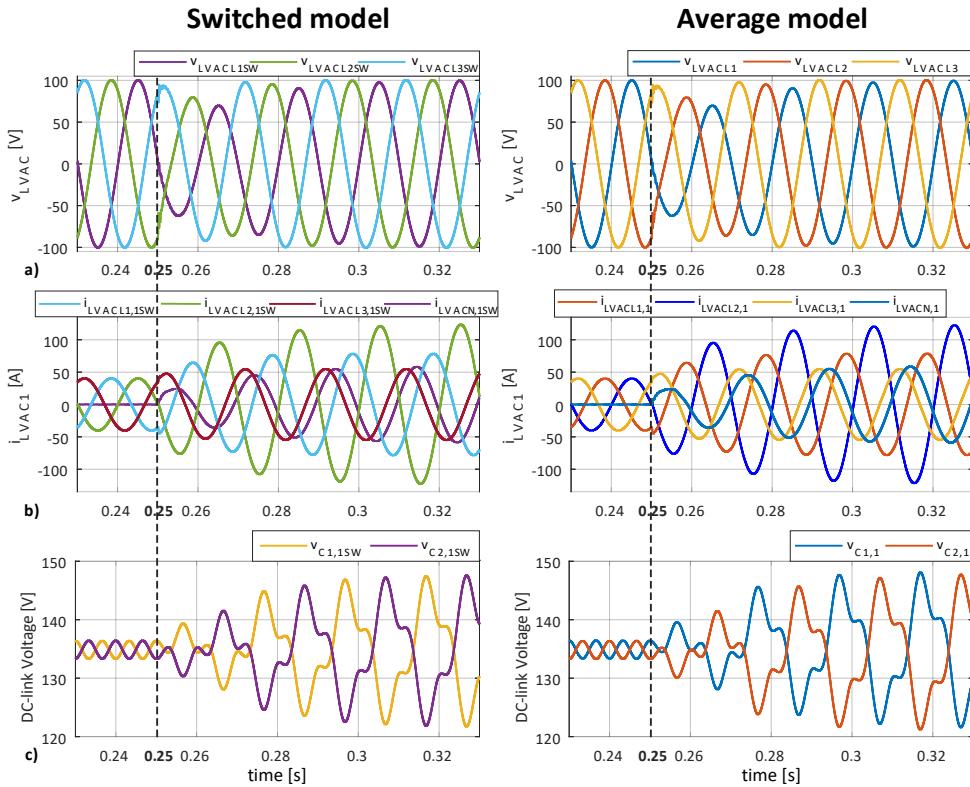


Figure 4.3: Comparison between average and detailed model of one T-Type module

Finally, to show the greatest advantage of the averaged model over the detailed for large converters, the real time of 1 s simulation are compared in Table 4.2. The results confirm the need to build an average model due to the very large simulation time of large converters which is explained in Section 1.3. Thanks to the averaging process there is a huge reduction of simulation time.

Table 4.2: Simulation time comparison

	Simulation time of average model	Simulation time of switched model
AC-MV/DC-MV	6.89 s	100.8 s
DC-MV/DC-LV	12.48 s	400.9 s
DC-LV/AC-LV	19.78 s	723.9 s
Whole ST	139.6 s	—

4.2 The behaviour of the ST average model in specific conditions

Three cases have been carried out to illustrate the behaviour of the hole average model of ST with the control strategy described in Chapter 3. The first of them assumes the symmetrical MV grid and symmetrical LV-AC load, the second one considered symmetrical MV grid and asymmetrical LV-AC load and the last one is related to asymmetrical MV grid and LV-AC load. The applied LV-AC load is linear and resistive. In the case of the asymmetrical load, the active power of $L1$, $L2$, $L3$ phases equals 1, 3, 4 kW respectively. The asymmetry in the MV grid is simulated by a 20% reduction in the nominal voltage amplitude in phase a and an increase of 20% in phase c . The simulation results of the considered conditions are shown in Figure 4.4. In 0.34 s there is a step-change in the symmetrical LV-AC load to asymmetrical conditions. The load change is transferred to the LV-DC link and then to the MV-DC links with a small influence on the MV grid current $i_{MVAC,x}$. Note that the total value of the required active power is constant over time and equals 10 kW. The second step take place in 0.4975 s, changing the symmetrical MV-AC grid into an asymmetrical one but this has a visible influence on the MV-DC links and MV currents. The results show that the developed ST average model works correctly which confirms the ability to verify the developed algorithms according to the assumptions.

Due to the fact that only basic control strategy has been considered, only three cases of the ST operation have been tested.

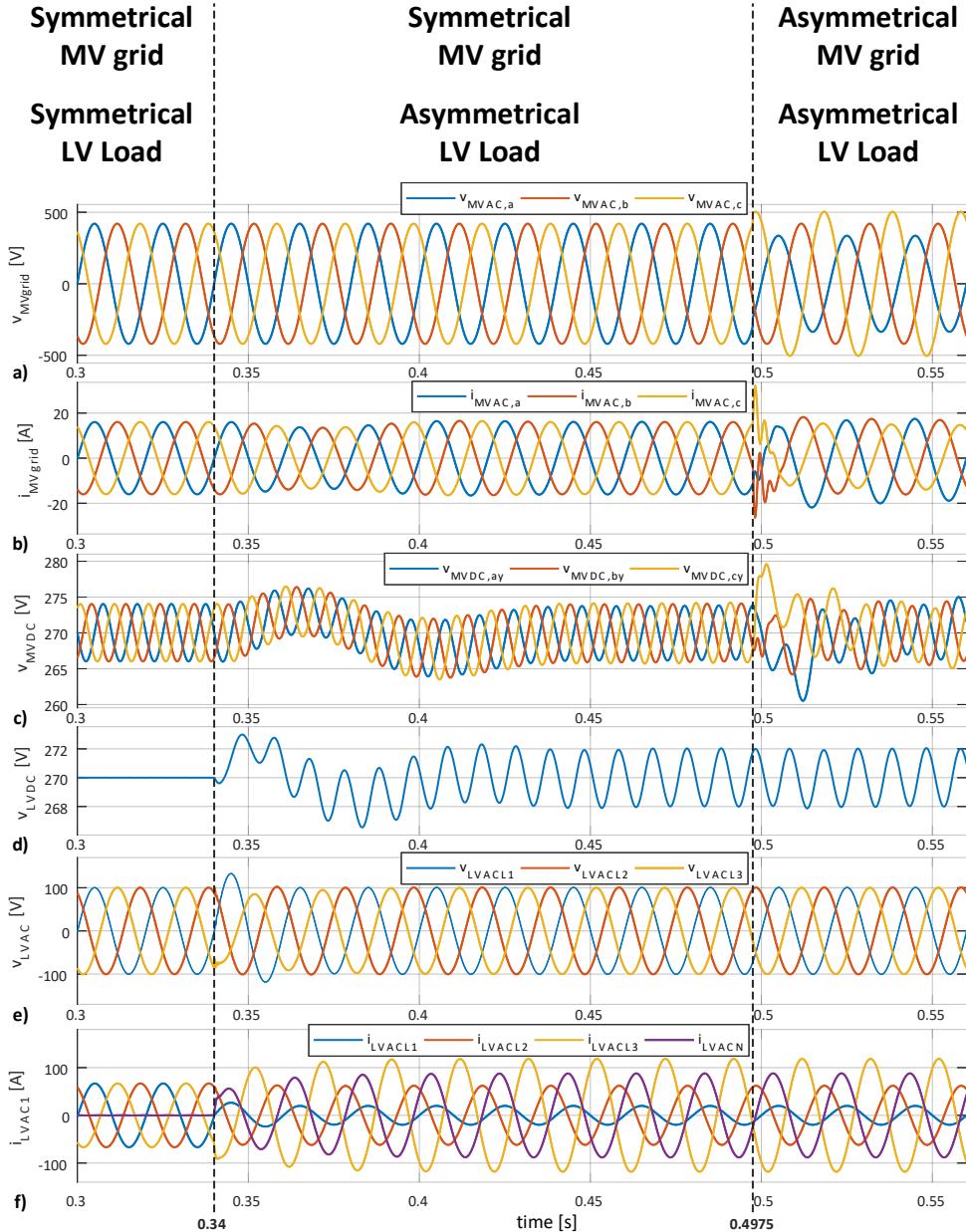


Figure 4.4: Selected ST voltages and currents waveform with symmetrical or asymmetrical MV grid or LV load.

4.3 Load identification algorithm: Simulation results

4.3.1 Converter and load models

Only the DC-LV/AC-LV stage of ST is sufficient to verify the load identification algorithms. The schematic of the used converter model is presented in Figure 4.5.

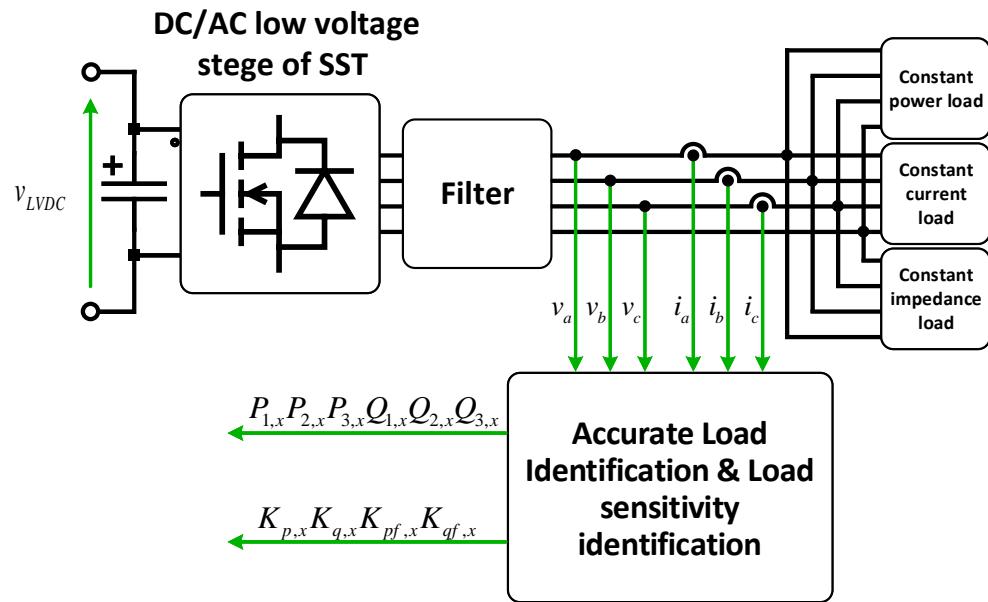


Figure 4.5: Load Identification scheme

The model includes constant current and constant power loads simulated by controlled current sources synchronized with the voltage in Point of Common Coupling (PCC). Therefore only the powers of impedance loads are sensitive to frequency changes.

4.3.2 Accurate Load Identification

In order to verify the correctness of the ALI algorithm, it was tested for various loads in each phase. It is worth emphasizing that all power value and the voltage amplitude values are averaged based on 1000 samples with a sampling step of $0.01\mu s$. The example active power value in the phase A and the reference and real voltage amplitude values with the averaging intervals are presented in Figure 4.6. As it is shown in the figure the dip of active power P_a is delayed in relation to reference voltage amplitude. This delay strongly depends on the ST load type. Therefore, the averaging intervals are in periods of time where a steady state will occur for the majority of real loads.

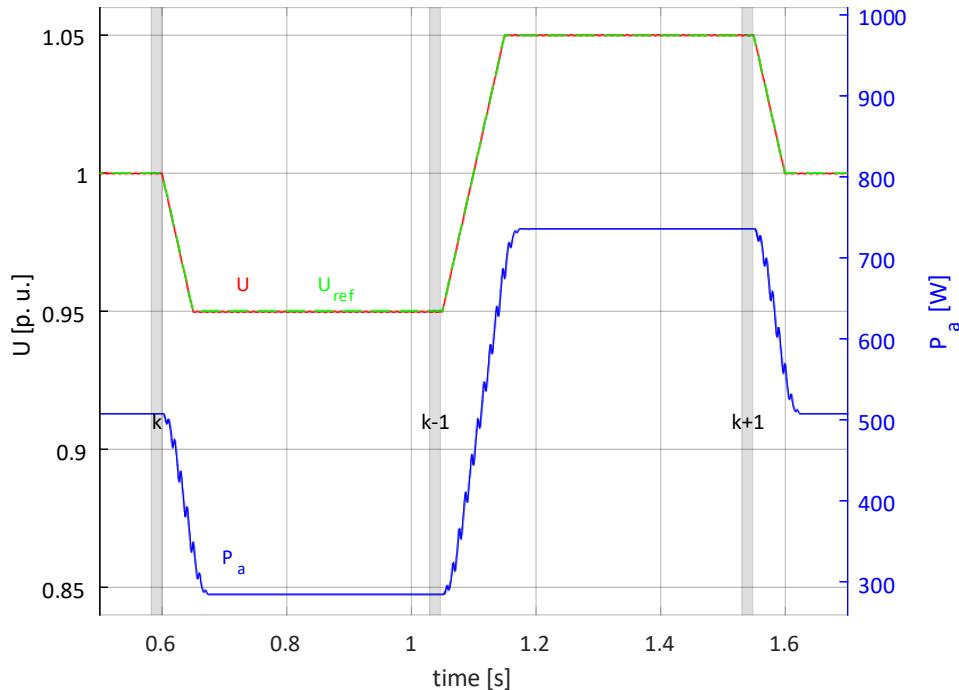


Figure 4.6: The waveforms of reference and real voltage amplitude with active power value in the phase A .

The Table 4.3 and Table 4.4 summarize the estimated power of individual types of loads using the algorithm, the actual values and the relative and absolute error of this method. It can be noticed that there are only small differences between the estimated and actual values of the powers.

Table 4.3: Simulation results of ALI without measurement noise

		Estimated [W]	Actual values[W]	Absolute error [W]	Relative error [%]
P_1	A	-2994.780	-2999.993	5.213	-0.17378
	B	3990.831	4000.001	-9.170	-0.22925
	C	999.816	1000.015	-0.199	-0.01990
P_2	A	2488.558	2499.042	-10.484	-0.41950
	B	4996.771	4978.422	18.349	0.36857
	C	-6003.098	-6003.637	0.539	-0.00898
P_3	A	1012.805	1007.547	5.257	0.52177
	B	1980.163	1989.349	-9.186	-0.46176
	C	3008.285	3008.438	-0.153	-0.00508

Table 4.4: Simulation results of ALI without measurement noise

		Estimated [var]	Actual values[var]	Absolute error [var]	Relative error [%]
Q_1	A	99.790	100.000	-0.209	-0.20936
	B	199.855	199.998	-0.142	-0.07122
	C	-1000.154	-1000.005	-0.148	0.01484
Q_2	A	-99.542	-99.978	0.436	-0.43613
	B	199.429	199.118	0.310	0.15572
	C	-99.729	-100.080	0.351	-0.35109
Q_3	A	99.035	99.273	-0.238	-0.23997
	B	-99.632	-99.382	-0.250	0.25143
	C	-300.543	-300.311	-0.232	0.07721

Furthermore, Table 4.5 and Table 4.6 show ALI results with Gaussian noise at current and voltage measurement, where their standard deviation is 0.01 A and 0.23 V , respectively. Due to the random nature of the results the tables show the standard derivation and the average values of the returned coefficients obtained based on 20 load identifications. Unfortunately, the results show a huge impact of the inaccuracy of measurements of phase currents and voltages on the ALI error.

Table 4.5: Simulation results of ALI with measurement noise

		Estimated mean value [W]	Actual values[W]	Standard deviation σ [W]
P_1	A	752.7	786.4886	135.1
	B	698.1	779.1131	143.3
	C	776.6	776.0024	144.8
P_2	A	4.035	0	274.6
	B	142.6	0	290.9
	C	58.22	0	293.6
P_3	A	695.6	668.5	138.5
	B	646.1	710.3	147.1
	C	724.4	785.9	148.1

Table 4.6: Simulation results of ALI with measurement noise

		Estimated mean value [var]	Actual values[var]	Standard deviation σ [var]
Q_1	A	56.29	0	76.48
	B	51.35	0	109.2
	C	99.15	0	79.29
Q_2	A	-44.31	0	154.2
	B	2.524	0	218.3
	C	-95.24	0	157.5
Q_3	A	181.95	65.5	77.42
	B	84.16	78.1	108.8
	C	131.6	77.3	78.078

4.3.3 Load Sensitivity Identification

Similarly to the ALI algorithm, the sensitivity parameters K_p , K_{fp} , K_q and K_{fq} are determined based on power values, voltage frequency and amplitude which are averaged values from the 1000 samples with a sampling step of $0.01\mu s$. The power value in the phase A and the reference and real voltage amplitude and frequency values with the averaging intervals are presented in Figure 4.7. The figure shows active power response to the voltage amplitude and frequency change.

A Table 4.7 summarizes the estimated sensitivity values using the considered algorithm and the real values by means of Eq. 3.12 and 3.13 which were used to verify the correctness of identification.

Table 4.7: Simulation results of Load sensitivity identification: I - one-sided differential quotient, II - central differential quotient

	Actual values [-]	Estimated I [-]	Absolute error I [-]	Estimated II [-]	Absolute error II [-]
K_p	A 8.9109	8.5927	0.3182	8.9091	0.0018
	B 0.8167	0.8195	0.0028	0.8167	0
	C -0.0067	-0.0219	0.0152	-0.0067	0
K_q	A 0.9926	0.7524	0.2402	0.9922	0.0004
	B 0.0007	-0.0021	0.0028	0.0006	0.0001
	C 0.5004	0.3784	0.1220	0.5003	0.0001

Possible differences between the estimation and real values of load sensitivity to voltage result mainly from the numerical representation of the derivative, which is in the form of a one-sided first order differential quotient.

As it was mentioned in section 3.4.3 it is possible to increase the accuracy of determining K_p and K_q coefficients by calculating them using the first order central differential quotient when the ALI algorithm is implemented. The table Table 4.7 shows a significant central advantage over one-sided differential quotient based on the Figure 4.6

4.3.4 Overload protection control

Overload protection control is aimed at limiting the current flowing on the LV grid by changing the voltage frequency or amplitude. If current value reaches $I_{security}$ level in at least one phase the algorithm will not lead to its further increase. The load of the converter was asymmetrical. In addition,

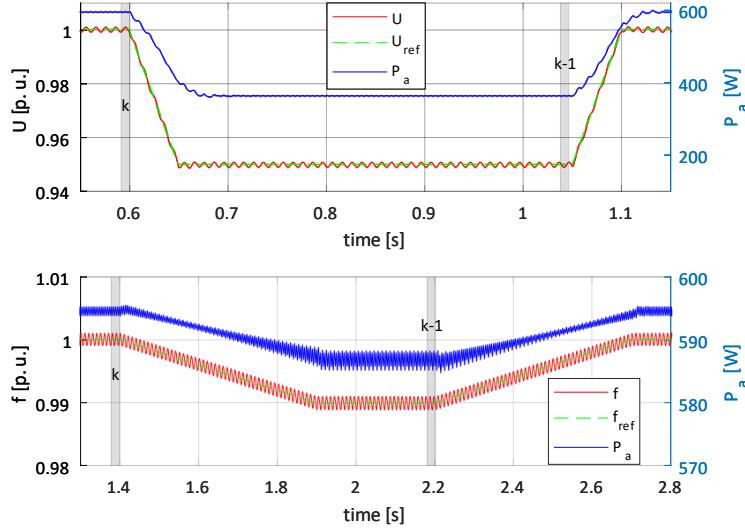


Figure 4.7: The waveforms of reference and real voltage amplitude and frequency with active power value in the phase A .

symmetrical, time-varying, independent of voltage, active power has been added to study the behaviour of this algorithm at time-varying load.

After initial identification of the load sensitivity (Figure 4.8) whose response is visible as almost stepwise changes in active and reactive power as well as currents in all phases between, the voltage frequency starts to change in 4.24s when the current in phase A is greater than $I_{security}$ level. When the frequency value reaches the limit value permitted by the standards ($\pm 1\%$) in 5.12s, then the voltage amplitude changes. Afterwards, when the load of the phase A decrease then the voltage amplitude return to the nominal value in 9.84s, and then the frequency also return to the nominal value in 11.27s. Moreover, to illustrate the changes introduced by the considered algorithm, active and reactive power waveform are added, which would force the load if the considered algorithm would not work. Unfortunately, the overload in one phase also causes a change in the voltage quality in the remaining ones, which is visible on their current waveforms (Figure 4.8a). Therefore, the case in which the voltage was only reduced in one phase was investigated, prompting for voltage asymmetry in PCC. The current is limited in each phase separately by changing voltage value only in the phase in which the current exceeded the dangerous level (Figure 4.8b). Thanks to this, the con-

sumers connected to the other phases do not feel the overloads of another phase. It is worth noting that it is not possible to change the frequency only in one phase so it causes that this solution allows controlling the current to a lesser extent because it is only possible to influence the voltage amplitude in the phase.

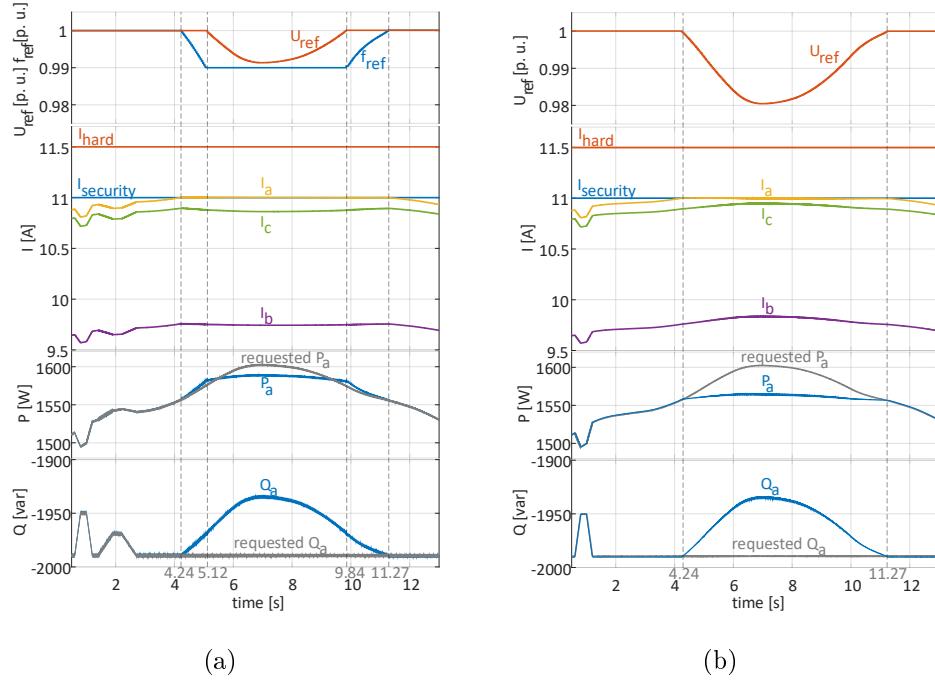


Figure 4.8: Overload Protection Control with symmetrical (4.8a) and asymmetrical (4.8b) voltage in PCC.

4.3.5 Soft load reduction control

The aim of soft load reduction control is to reduce the active power consumption by the loads on the LV grid on demand by the set value γ . The load on the inverter has been asymmetrical. Moreover, symmetrical active power has been added which was time-varying, but independent of voltage to verify the algorithm under these conditions.

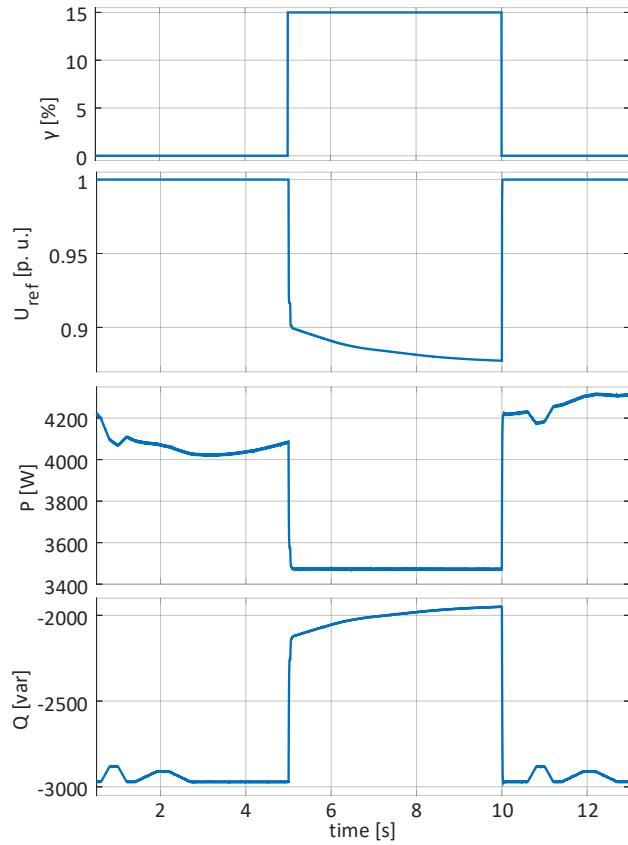


Figure 4.9: Simulation results of Soft Load Reduction

In contrast to the algorithm described in [27], when the ST receive the power reduction request the algorithm stores the power value at this moment and then relative to this stored power value it is reduced by γ and is kept constant until the time in which the power reduction request will be interrupted. This means that the voltage value is constantly changed so as to maintain a constant active power value at the request time, which is shown in Figure 4.9. The way in which the voltage value is changed to maintain constant power is determined on the earlier periodical identification of the load sensitivity to the voltage.

Chapter 5

Final Conclusions

The main goal of the thesis has been developing the ST averaged model to verify the considered topology of the ST from the control point of view. Due to the large size of ST, the construction of its average model have been proposed instead of a detailed one. In the thesis, the whole ST averaging process and the basic ST control strategy are described. Within control strategy load identification algorithms, along with their two applications have been distinguished. Moreover, the ST averaged model has been built and its correctness has been verified by comparing the behaviour of its parts with their detailed models. Finally, the simulation study of the whole ST model with its basic control strategy has been carried out.

The proposed ST model fulfilled its task, offering the possibility of testing the entire ST with its complete control in relatively high accuracy and high speed of simulation. Thus, the average model of ST is effective to perform power system dynamic studies and interaction between all three part of ST. Thanks to the relatively fast simulation of the average model, it significantly speeds up the process of tuning the control of ST. Moreover, the ST model can be useful for external fault management studies like a voltage sag at the MV grid.

It is worth noting that there is possibility to implement more complicated control algorithms under the proviso that these algorithms return exact control signals as algorithms presented in Chapter 3 and also their operation is not an indispensable part of the modulation method.

The thesis also presents the algorithms used to load identification, along with its two applications. The first of these is the ST overload protection, which is aimed at limiting the current flowing on the LV grid by changing the voltage frequency or amplitude. It is worth emphasizing that how much the ST overload ability could increase due to the application of overload protection control is strongly influenced by the type of load. The second

one is the soft load reduction. The application of this algorithm is to reduce the power consumption of loads imposed by the electric power system in the event of a fault in order to maintain grid stability. It allows increasing the reliability of power supply to the loads, because it only reduces their power consumption, without depriving some of them the power. Moreover, this algorithm can be used in the event of a power failure of the ST from the medium voltage grid side, when the power is taken from the energy storage in the DC microgrid. Then, by monitoring the voltage drop in the DC-link, it is possible to relieve the energy storage by reducing the power consumption of loads in the low voltage grid. In addition, the research also presents the proposed algorithm used to accurate load identification called ALI. The algorithm, in theory, allows determining the value of the resultant power of individual types of loads, with the preservation of the sign which allows determining the direction of the power flow of each type of loads. It could allow to better use the energy storage attached to the DC circuit of the power electronics converter. The obtained information determines if it is possible to reduce the power of the converter and how much the power can be reduced so that the electricity can provide to local loads in the long-term. Another application of the ALI is to provide detailed information on loads in order to monitor and supervise the grid-connected to the power electronic converter working as a voltage source. Unfortunately, the simulation study also shows that the ALI is very sensitive to the inaccuracy of the calculation of active and reactive power determined based on measurements of currents and voltages. Therefore, this method is difficult to implement because it requires very accurate and advanced measuring devices.

To sum up, a properly functioning ST model has been built that allows testing the control strategy of the entire ST. Therefore, the purpose of the thesis has been realized.

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