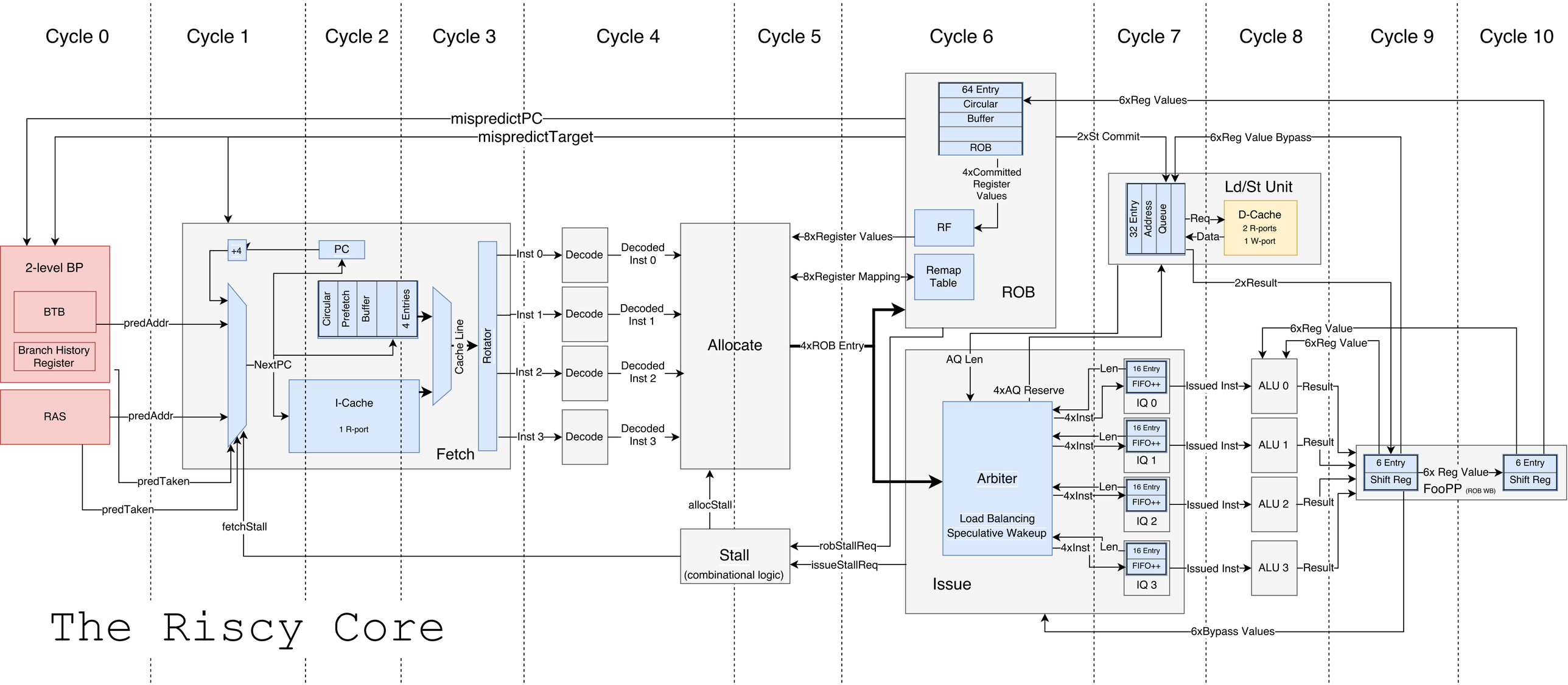
Cycle 0
Cycle 1
Cycle 2
Cycle 3
Cycle 4
Cycle 5
Cycle 6
Cycle 7
Cycle 8
Cycle 9
Cycle 10
mispredictPC
mispredictTarget
2-level BP
BTB
Branch History Register
RAS
predAddr
predAddr
predTaken
predTaken
fetchStall
+4
PC
NextPC
Circular
Prefetch
Buffer
4 Entries
I-Cache
1 R-port
Cache Line
Rotator
Fetch
Inst 0
Inst 1
Inst 2
Inst 3
Decode
Decode
Decode
Decode
Decoded Inst 0
Decoded Inst 1
Decoded Inst 2
Decoded Inst 3
Allocate
allocStall
Stall
(combinational logic)
robStallReq
issueStallReq
8xRegister Values
8xRegister Mapping
4xROB Entry
64 Entry
Circular
Buffer
ROB
4xCommitted Register Values
RF
Remap Table
ROB
6xReg Values
2xSt Commit
6xReg Value Bypass
Ld/St Unit
32 Entry
Address
Queue
Req
Data
D-Cache
2 R-ports
1 W-port
2xResult
AQ Len
4xAQ Reserve
Arbiter
Load Balancing
Speculative Wakeup
Issue
Len
4xInst
16 Entry
FIFO++
IQ 0
IQ 1
IQ 2
IQ 3
Issued Inst
ALU 0
ALU 1
ALU 2
ALU 3
Result
6xReg Value
6xReg Value
6 Entry
Shift Reg
6x Reg Value
FooPP (ROB WB)
6 Entry
Shift Reg
6xBypass Values
The Riscy Core