channel nodes have sent their packets so it is safe them to switch back to configuration one in preparation for the next packet period. Once again, reference to a global sample counter allows safe, predictable deterministic system behavior.

V. Mixing

Mixing is achieved by the scaling and accumulating of each channel packet in the mix node to form a mix packet. The realtime host keeps track of fader and pan positions and on/off information. Whenever a change to any of these parameters occurs a new mix scaler is calculated for the appropriate channel and written to the mix nodes via parallel DMA. A packet sent to a mix node is received in the input FIFO, and each of the 70 samples is multiplied by the current mix scaler for that channel and accumulated in a mix buffer.

The nodes assigned to the task of mixing include those mixing the master left and right outputs, the monitor left and right outputs and the auxiliary mix outputs. The number of nodes assigned to mixing is based on the ratio of the time to send a packet on the bus to the time taken unloading the current channel packet from the FIFO. This ratio is approximately 0.5 to 1, i.e., the packet sends are twice as fast as the FIFO unloads. Thus, in order to fully utilize the bus time segment two mix nodes are used to perform each single channel mix. Odd numbered channel nodes send their packets to the "odd" mix nodes, and even numbered channel nodes send their packets to the "even" mix nodes. In this manner, the bus is fully utilized. Channel node packet sends occur at each sample count whereas mix node FIFO unloads are overlapped by one sample count, odd mix node FIFO unloads starting on odd sample counts and even mix node FIFO unloads starting on even sample counts. The alternation of FIFO unloads between odd and even mix nodes allows sufficient mix processing time since each FIFO unload, scaling and accumulation of a packet requires almost two sample counts to complete. Also, as mentioned before, the order of the channel packets received is always 1, 3, 5, 7, etc. in the odd mix nodes and 2, 4, 6, 8, etc. in the even mix nodes. Therefore, scalers for each distinct channel packet can be read from an incrementing pointer.

Odd and even mix nodes are adjacent to one another, the even node one position further "to the right" in the linear array than the odd node. The mix nodes for a 60 channel system include the following, in order left to right: auxiliary mix one odd, auxiliary mix one even, auxiliary mix two odd, auxiliary mix two even . . . auxiliary mix six odd, auxiliary mix six even, monitor left odd, monitor left even, monitor right odd, monitor right even, master mix left odd, master mix left even, master mix right odd, master mix right even.

After all channel nodes have sent their packets, i.e., sample count 8, the odd mix nodes switch to configuration two, i.e., connect their output FIFOs, and send their accumulated "odd channel mix" to the respective even mix node "mate" which is adjacent. No blocking results since the send is to a nearest right neighbor. The even mix nodes accumulate the full channel mix, left, right or auxiliary as the case may be, and leave it in a buffer to be removed by DMA in the next packet period. After sending the accumulated odd channel mix to its even neighbor, the odd mix node switches back to configuration one, receive or pass-through, to be ready for the next packet period sends. This switch is completed well before the sample counter reaches zero and hence, once again, no blocking ever occurs.

Each odd or even channel node is able to broadcast to all odd or even mix nodes because each node is allowed to have up to three logical bus addresses. Thus each node can be assigned its ordinal number in the linear array, and all odd mix nodes can be assigned one "group ID" while all even mix nodes can be assigned a second group ID. These ID numbers are written to a specific location in the packet header when the packet is built. The ID is used by the communications ASICs to determine whether a packet is to be loaded, loaded and passed on, or simply passed on.

A summary of the sequence of events within each packet period can now be specified for an example 60 channel system. First, channel node one switches to configuration two and broadcasts its packet to all odd mix nodes at sample counter 68. Next, channel node two switches to configuration two and broadcasts its packet to all even mix nodes at sample counter 67. This procedure continues until finally, channel 60 switches to configuration two and broadcasts its packet to all even mix nodes at sample counter 9. Then at sample counter 8 all channel nodes switch back to configuration one, and all odd mix nodes switch to configuration two and send their odd channel mix accumulations to their corresponding right neighbor even mix nodes which accumulate the final mix packets to be sent by serial DMA during the next packet period. Next, all odd mix nodes switch back to configuration one. Finally, when the sample counter reaches zero (or the DMA pointer reaches its barrier address) all node states are incremented and all buffer pointers are set according to the new state, and the sample counter is reset to 70 for the next packet period. The overall mix and monitor system delay is