



5.79 inch E-paper Display Series



GDEY0579Z93

Dalian Good Display Co., Ltd.

Product Specifications



Customer	Standard
Description	5.79" E-PAPER DISPLAY
Model Name	GDEY0579Z93
Date	2022/08/01
Revision	1.0

	Design Engineering		
	Approval	Check	Design

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1. Overview

GDEY0579Z93 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black and red full display capabilities. The 5.79 inch active area contains 272×792 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

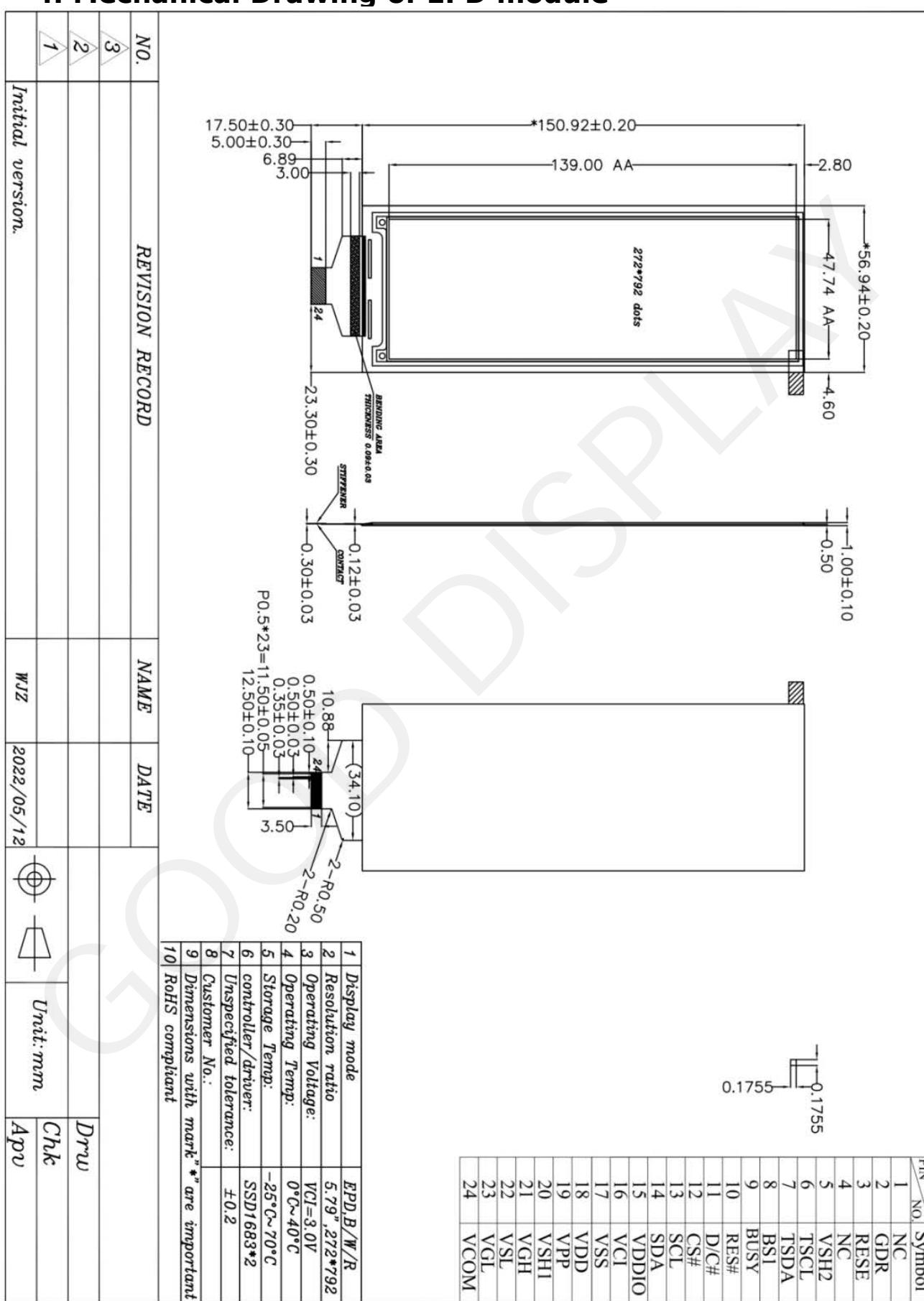
2. Features

- 272×792 pixels display
- High contrast High reflectance
- Ultra wide viewing angle Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform can stored in On-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I²C signal master interface to read external temperature sensor
- Support partial update mode
- Built-in temperature sensor

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	5.79	Inch	
Display Resolution	272(H)×792(V)	Pixel	Dpi:144
Active Area	47.74×139.00	mm	
Pixel Pitch	0.1755×0.1755	mm	
Pixel Configuration	Rectangle		
Outline Dimension	56.94(H)×150.92(V) ×1.0(D)	mm	
Weight	16.5±0.5	g	

4. Mechanical Drawing of EPD module



5. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I ² C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I ² C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 54
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C =Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode.

When the pin is pulled HIGH, the data at SDA will be interpreted as data.
When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when

- Outputting display waveform
- Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Command Table

Command Table																																																																			
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																							
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]= 12Bh [POR], 300 MUX MUX Gate lines setting as (A[8:0] + 1).																																																							
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		B [2:0] = 000 [POR]. Gate scanning sequence and direction																																																							
0	1		0	0	0	0	0	0	0	A ₈		B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, ... GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ...																																																							
0	1		0	0	0	0	0	B ₂	B ₁	B ₀		B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3...299 (left and right gate interlaced) SM=1, G0, G2, G4 ...G294, G1, G3, ...G299																																																							
												B[0]: TB TB = 0 [POR], scan from G0 to G299 TB = 1, scan from G299 to G0.																																																							
<hr/>																																																																			
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage A[4:0] = 00h [POR] VGH setting from 10V to 20V																																																							
0	1		0	0	0	A ₄	A ₃	A ₂	A ₁	A ₀		<table border="1"> <thead> <tr> <th>A[4:0]</th> <th>VGH</th> <th>A[4:0]</th> <th>VGH</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>20</td> <td>0Dh</td> <td>15</td> </tr> <tr> <td>03h</td> <td>10</td> <td>0Eh</td> <td>15.5</td> </tr> <tr> <td>04h</td> <td>10.5</td> <td>0Fh</td> <td>16</td> </tr> <tr> <td>05h</td> <td>11</td> <td>10h</td> <td>16.5</td> </tr> <tr> <td>06h</td> <td>11.5</td> <td>11h</td> <td>17</td> </tr> <tr> <td>07h</td> <td>12</td> <td>12h</td> <td>17.5</td> </tr> <tr> <td>08h</td> <td>12.5</td> <td>13h</td> <td>18</td> </tr> <tr> <td>07h</td> <td>12</td> <td>14h</td> <td>18.5</td> </tr> <tr> <td>08h</td> <td>12.5</td> <td>15h</td> <td>19</td> </tr> <tr> <td>09h</td> <td>13</td> <td>16h</td> <td>19.5</td> </tr> <tr> <td>0Ah</td> <td>13.5</td> <td>17h</td> <td>20</td> </tr> <tr> <td>0Bh</td> <td>14</td> <td>Other</td> <td>NA</td> </tr> <tr> <td>0Ch</td> <td>14.5</td> <td></td> <td></td> </tr> </tbody> </table>	A[4:0]	VGH	A[4:0]	VGH	00h	20	0Dh	15	03h	10	0Eh	15.5	04h	10.5	0Fh	16	05h	11	10h	16.5	06h	11.5	11h	17	07h	12	12h	17.5	08h	12.5	13h	18	07h	12	14h	18.5	08h	12.5	15h	19	09h	13	16h	19.5	0Ah	13.5	17h	20	0Bh	14	Other	NA	0Ch	14.5	
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0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B [7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V Remark: VSH1>=VSH2																																																																																																																																																																																																																																																																																													
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98h	3.4	B8h	6.6																																																																																																																																																																																																																																																																																																						
99h	3.5	B9h	6.7																																																																																																																																																																																																																																																																																																						
9Ah	3.6	BAh	6.8																																																																																																																																																																																																																																																																																																						
9Bh	3.7	BBh	6.9																																																																																																																																																																																																																																																																																																						
9Ch	3.8	BCh	7																																																																																																																																																																																																																																																																																																						
9Dh	3.9	BDh	7.1																																																																																																																																																																																																																																																																																																						
9Eh	4	BEh	7.2																																																																																																																																																																																																																																																																																																						
9Fh	4.1	BFh	7.3																																																																																																																																																																																																																																																																																																						
A0h	4.2	C0h	7.4																																																																																																																																																																																																																																																																																																						
A1h	4.3	C1h	7.5																																																																																																																																																																																																																																																																																																						
A2h	4.4	C2h	7.6																																																																																																																																																																																																																																																																																																						
A3h	4.5	C3h	7.7																																																																																																																																																																																																																																																																																																						
A4h	4.6	C4h	7.8																																																																																																																																																																																																																																																																																																						
A5h	4.7	C5h	7.9																																																																																																																																																																																																																																																																																																						
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A7h	4.9	C7h	8.1																																																																																																																																																																																																																																																																																																						
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ADh	5.5	Other	NA																																																																																																																																																																																																																																																																																																						
A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2																																																																																																																																																																																																																																																																																																						
21h	8.8	37h	13																																																																																																																																																																																																																																																																																																						
23h	9	38h	13.2																																																																																																																																																																																																																																																																																																						
24h	9.2	39h	13.4																																																																																																																																																																																																																																																																																																						
25h	9.4	3Ah	13.6																																																																																																																																																																																																																																																																																																						
26h	9.6	3Bh	13.8																																																																																																																																																																																																																																																																																																						
27h	9.8	3Ch	14																																																																																																																																																																																																																																																																																																						
28h	10	3Dh	14.2																																																																																																																																																																																																																																																																																																						
29h	10.2	3Eh	14.4																																																																																																																																																																																																																																																																																																						
2Ah	10.4	3Fh	14.6																																																																																																																																																																																																																																																																																																						
2Bh	10.6	40h	14.8																																																																																																																																																																																																																																																																																																						
2Ch	10.8	41h	15																																																																																																																																																																																																																																																																																																						
2Dh	11	42h	15.2																																																																																																																																																																																																																																																																																																						
2Eh	11.2	43h	15.4																																																																																																																																																																																																																																																																																																						
2Fh	11.4	44h	15.6																																																																																																																																																																																																																																																																																																						
30h	11.6	45h	15.8																																																																																																																																																																																																																																																																																																						
31h	11.8	46h	16																																																																																																																																																																																																																																																																																																						
32h	12	47h	16.2																																																																																																																																																																																																																																																																																																						
33h	12.2	48h	16.4																																																																																																																																																																																																																																																																																																						
34h	12.4	49h	16.6																																																																																																																																																																																																																																																																																																						
35h	12.6	4Ah	16.8																																																																																																																																																																																																																																																																																																						
36h	12.8	4Bh	17																																																																																																																																																																																																																																																																																																						
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C[7:0]	VSL																																																																																																																																																																																																																																																																																																								
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Other	NA																																																																																																																																																																																																																																																																																																								
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												The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.																																																																																																																																																																																																																																																																																													
0	0	09	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write Register for Initial Code Setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of Initial Code Setting																																																																																																																																																																																																																																																																																													
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																																																																																																																																																																																																																																																																															
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																																																																																																																																																																																																																																																																															
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0	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀																																																																																																																																																																																																																																																																																															
0	0	0A	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting																																																																																																																																																																																																																																																																																													

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																												
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting.																												
0	1		1	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[7:0] -> Soft start setting for Phase1 = 8Bh [POR]																												
0	1		1	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		B[7:0] -> Soft start setting for Phase2 = 9Ch [POR]																												
0	1		1	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		C[7:0] -> Soft start setting for Phase3 = 96h [POR]																												
0	1		0	0	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D[7:0] -> Duration setting = 0Fh [POR]																												
												Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]:																												
												<table border="1"> <thead> <tr> <th>Bit[6:4]</th> <th>Driving Strength Selection</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>1(Weakest)</td> </tr> <tr> <td>001</td> <td>2</td> </tr> <tr> <td>010</td> <td>3</td> </tr> <tr> <td>011</td> <td>4</td> </tr> <tr> <td>100</td> <td>5</td> </tr> <tr> <td>101</td> <td>6</td> </tr> <tr> <td>110</td> <td>7</td> </tr> <tr> <td>111</td> <td>8(Strongest)</td> </tr> </tbody> </table>	Bit[6:4]	Driving Strength Selection	000	1(Weakest)	001	2	010	3	011	4	100	5	101	6	110	7	111	8(Strongest)										
Bit[6:4]	Driving Strength Selection																																							
000	1(Weakest)																																							
001	2																																							
010	3																																							
011	4																																							
100	5																																							
101	6																																							
110	7																																							
111	8(Strongest)																																							
												<table border="1"> <thead> <tr> <th>Bit[3:0]</th> <th>Min Off Time Setting of GDR [Time unit]</th> </tr> </thead> <tbody> <tr> <td>0000 ~ 0011</td> <td>NA</td> </tr> <tr> <td>0100</td> <td>2.6</td> </tr> <tr> <td>0101</td> <td>3.2</td> </tr> <tr> <td>0110</td> <td>3.9</td> </tr> <tr> <td>0111</td> <td>4.6</td> </tr> <tr> <td>1000</td> <td>5.4</td> </tr> <tr> <td>1001</td> <td>6.3</td> </tr> <tr> <td>1010</td> <td>7.3</td> </tr> <tr> <td>1011</td> <td>8.4</td> </tr> <tr> <td>1100</td> <td>9.8</td> </tr> <tr> <td>1101</td> <td>11.5</td> </tr> <tr> <td>1110</td> <td>13.8</td> </tr> <tr> <td>1111</td> <td>16.5</td> </tr> </tbody> </table>	Bit[3:0]	Min Off Time Setting of GDR [Time unit]	0000 ~ 0011	NA	0100	2.6	0101	3.2	0110	3.9	0111	4.6	1000	5.4	1001	6.3	1010	7.3	1011	8.4	1100	9.8	1101	11.5	1110	13.8	1111	16.5
Bit[3:0]	Min Off Time Setting of GDR [Time unit]																																							
0000 ~ 0011	NA																																							
0100	2.6																																							
0101	3.2																																							
0110	3.9																																							
0111	4.6																																							
1000	5.4																																							
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1011	8.4																																							
1100	9.8																																							
1101	11.5																																							
1110	13.8																																							
1111	16.5																																							
												D[5:0]: duration setting of phase D[5:4]: duration setting of phase 3 D[3:2]: duration setting of phase 2 D[1:0]: duration setting of phase 1																												
												<table border="1"> <thead> <tr> <th>Bit[1:0]</th> <th>Duration of Phase [Approximation]</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>10ms</td> </tr> <tr> <td>01</td> <td>20ms</td> </tr> <tr> <td>10</td> <td>30ms</td> </tr> <tr> <td>11</td> <td>40ms</td> </tr> </tbody> </table>	Bit[1:0]	Duration of Phase [Approximation]	00	10ms	01	20ms	10	30ms	11	40ms																		
Bit[1:0]	Duration of Phase [Approximation]																																							
00	10ms																																							
01	20ms																																							
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11	40ms																																							

Command Table																							
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description											
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode												
0	1		0	0	0	0	0	0	A ₁	A ₀													
										Deep Sleep mode Control: A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2			After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver										
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting										Define data entry sequence A[2:0] = 011 [POR]		
0	1		0	0	0	0	0	0	A ₂	A ₁	A ₀											A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR]	
										A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.													
0	0	12	0	0	0	1	0	0	1	0	SW RESET										It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description														
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[7:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).														
0	1		0	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.														
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect														
0	1		0	0	0	0	0	A ₂	A ₁	A ₀		<table border="1" data-bbox="1079 977 1333 1179"> <tr><th>A[2:0]</th><th>VCI level</th></tr> <tr><td>011</td><td>2.2V</td></tr> <tr><td>100</td><td>2.3V</td></tr> <tr><td>101</td><td>2.4V</td></tr> <tr><td>110</td><td>2.5V</td></tr> <tr><td>111</td><td>2.6V</td></tr> <tr><td>Other</td><td>NA</td></tr> </table> <p>The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).</p>	A[2:0]	VCI level	011	2.2V	100	2.3V	101	2.4V	110	2.5V	111	2.6V	Other	NA
A[2:0]	VCI level																									
011	2.2V																									
100	2.3V																									
101	2.4V																									
110	2.5V																									
111	2.6V																									
Other	NA																									
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor														
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] = 7Fh [POR]														
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.														
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6]
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[7:6] 00 Address + pointer 01 Address + pointer + 1st parameter 10 Address + pointer + 1st parameter + 2nd pointer 11 Address A[5:0] – Pointer Setting B[7:0] – 1 st parameter C[7:0] – 2 nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail.
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] B[7:0] = 00h [POR] A[7:4] Red RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content A[3:0] BW RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	0	0	0	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFH (POR)
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
											Operating sequence	Parameter (in Hex)
											Enable clock signal	80
											Disable clock signal	01
											Enable clock signal → Enable Analog	C0
											Disable Analog → Disable clock signal	03
											Enable clock signal → Load LUT with DISPLAY Mode 1 → Disable clock signal	91
											Enable clock signal → Load LUT with DISPLAY Mode 2 → Disable clock signal	99
											Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 1 → Disable clock signal	B1
											Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 2 → Disable clock signal	B9
											Enable clock signal → Enable Analog → Display with DISPLAY Mode 1 → Disable Analog → Disable OSC	C7
											Enable clock signal → Enable Analog → Display with DISPLAY Mode 2 → Disable Analog → Disable OSC	CF
											Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 1 → Disable Analog → Disable OSC	F7
											Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 2 → Disable Analog → Disable OSC	FF
0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0

Command Table													Description													
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command															
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26															
													After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly.													
													For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0													
													Read RAM													
													After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly.													
													The 1 st byte of data read is dummy data.													
													VCOM Sense													
													Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.													
													VCOM Sense Duration													
													Stabiling time between entering VCOM sensing mode and reading acquired. A[3:0] = 9h, duration = 10s. VCOM sense duration = (A[3:0]+1) sec													
													Program VCOM OTP													
													Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.													

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description			
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]			
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[7:0]	VCOM	A[7:0]	VCOM
												08h	-0.2	44h	-1.7
												0Ch	-0.3	48h	-1.8
												10h	-0.4	4Ch	-1.9
												14h	-0.5	50h	-2
												18h	-0.6	54h	-2.1
												1Ch	-0.7	58h	-2.2
												20h	-0.8	5Ch	-2.3
												24h	-0.9	60h	-2.4
												28h	-1	64h	-2.5
												30h	-1.2	6Ch	-2.7
												34h	-1.3	70h	-2.8
												38h	-1.4	74h	-2.9
												3Ch	-1.5	78h	-3
												40h	-1.6	Other	NA
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option:			
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[7:0]: VCOM OTP Selection (Command 0x37, Byte A)			
1	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		B[7:0]: VCOM Register (Command 0x2C)			
1	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes]			
1	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]			
1	1		E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀					
1	1		F ₇	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀					
1	1		G ₇	G ₆	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀					
1	1		H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀					
1	1		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀					
1	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀					
1	1		K ₇	K ₆	K ₅	K ₄	K ₃	K ₂	K ₁	K ₀					
0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]			
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀					
1	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀					
1	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀					
1	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀					
1	1		E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀					
1	1		F ₇	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀					
1	1		G ₇	G ₆	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀					
1	1		H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀					
1	1		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀					
1	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀					

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01]
1	1		0	0	A ₅	A ₄	0	0	A ₁	A ₀		Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [227 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR and XON[nXY] Refer to Session 6.7 WAVEFORM SETTING
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1	:	:	:	:	:	:	:	:	:		
0	1			
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command For details, please refer to SSD1683 application note. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈		
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option A[7] Spare VCOM OTP selection 0: Default [POR] 1: Spare B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] 0: Display Mode 1 1: Display Mode 2 F[6]: Ping-Pong for Display Mode 2 0: RAM Ping-Pong disable [POR] 1: RAM Ping-Pong enable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]~J[7:0] can be stored in OTP 2) RAM Ping-Pong function is not support for Display Mode 1
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored in OTP
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY follow the reference code sequences

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HiZ. A [7:6] :Select VBD option
0	1		A ₇	A ₆	A ₅	A ₄	0	0	A ₁	A ₀		A[7:6] Select VBD as 00 GS Transition, Defined in A[2] and A[1:0] 01 Fix Level, Defined in A[5:4] 10 VCOM 11[POR] HiZ
												A [5:4] Fix Level Setting for VBD
												A[5:4] VBD level 00 VSS 01 VSH1 10 VSL 11 VSH2
												A [1:0] GS Transition setting for VBD VBD Level Selection: 00b: VCOM ; 01b: VSH1; 10b: VSL; 11b: VSH2
												A[1:0] VBD Transition 00 LUT0 01 LUT1 10 LUT2 11 LUT3
0	0	3F	0	0	1	1	1	1	1	1	End Option (EOPT)	Option for LUT end
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		Set this byte to 22h
0	0	41	0	1	0	0	0	0	0	0	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26
0	1		0	0	0	0	0	0	0	A ₀		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address	Specify the start/end positions of the window address in the X direction by an address unit for RAM
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Start / End position	A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 31h
0	1		0	0	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address	Specify the start/end positions of the window address in the Y direction by an address unit for RAM
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Start / End position	A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 12Bh
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	0	46	0	1	0	0	0	1	1	0	Auto Write RED RAM for Regular Pattern	Auto Write RED RAM for Regular Pattern
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		A[7:0] = 00h [POR]

Command Table																																
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																				
												A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate <table border="1"><tr><td>A[6:4]</td><td>Height</td><td>A[6:4]</td><td>Height</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>256</td></tr><tr><td>010</td><td>32</td><td>110</td><td>300</td></tr><tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr></table>	A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	256	010	32	110	300	011	64	111	NA
A[6:4]	Height	A[6:4]	Height																													
000	8	100	128																													
001	16	101	256																													
010	32	110	300																													
011	64	111	NA																													
												A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source <table border="1"><tr><td>A[2:0]</td><td>Width</td><td>A[2:0]</td><td>Width</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>256</td></tr><tr><td>010</td><td>32</td><td>110</td><td>400</td></tr><tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr></table>	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	256	010	32	110	400	011	64	111	NA
A[2:0]	Width	A[2:0]	Width																													
000	8	100	128																													
001	16	101	256																													
010	32	110	400																													
011	64	111	NA																													
												BUSY pad will output high during operation.																				
0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR]	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate <table border="1"><tr><td>A[6:4]</td><td>Height</td><td>A[6:4]</td><td>Height</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>256</td></tr><tr><td>010</td><td>32</td><td>110</td><td>300</td></tr><tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr></table>	A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	256	010	32	110	300	011	64	111	NA
A[6:4]	Height	A[6:4]	Height																													
000	8	100	128																													
001	16	101	256																													
010	32	110	300																													
011	64	111	NA																													
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source <table border="1"><tr><td>A[2:0]</td><td>Width</td><td>A[2:0]</td><td>Width</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>256</td></tr><tr><td>010</td><td>32</td><td>110</td><td>400</td></tr><tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr></table>	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	256	010	32	110	400	011	64	111	NA
A[2:0]	Width	A[2:0]	Width																													
000	8	100	128																													
001	16	101	256																													
010	32	110	400																													
011	64	111	NA																													
												During operation, BUSY pad will output high.																				
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC)																				
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																						

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	
												A[5:0]: 00h [POR].	
0	0	4F	0	1	0	0	1	1	1	1		Set RAM Y address counter	
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].	
0	1		0	0	0	0	0	0	0	0	A ₈		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.	

7. Electrical Characteristics

7.1. Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V _{CI}	-0.5 to +6.0	V
Logic Input voltage	V _{IN}	-0.5 to V _{CI} +0.5	V
Logic Output voltage	V _{OUT}	0.5 to V _{CI} +0.5	V
Operating Temp range	TOPR	0 to +40	°C
Storage Temp range	T _{STG}	-25 to+70	°C
Optimal Storage Temp	T _{STG0}	23±2	°C
Optimal Storage Humidity	H _{STG0}	55±10	%RH

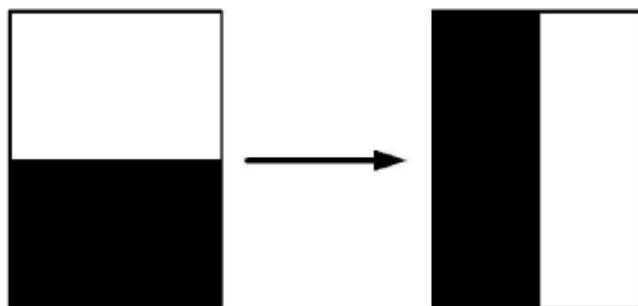
Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

7.2. Panel DC Characteristics

The following specifications apply for: V_{SS}=0V, V_{CI}=3.0V, TOPR =25°C

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V _{SS}	-		-	0	-	V
Logic supply voltage	V _{CI}	-	V _{CI}	2.2	3.0	3.7	V
Core logic voltage	V _{DD}		V _{DD}	1.7	1.8	1.9	V
High level input voltage	V _{IH}	-	-	0.8 V _{CI}	-	-	V
Low level input voltage	V _{IL}	-	-	-	-	0.2 V _{CI}	V
High level output voltage	V _{OH}	IOH = -100uA	-	0.9 V _{CI}	-	-	V
Low level output voltage	V _{OL}	IOL = 100uA	-	-	-	0.1 V _{CI}	V
Typical power	P _{TYP}	V _{CI} =3.0V	-	-	27	-	mW
Deep sleep mode	P _{STPY}	V _{CI} =3.0V	-	-	0.006	-	mW
Typical operating current	Iopr_V _{CI}	V _{CI} =3.0V	-	-	9	-	mA
Image update time	-	25 °C	-	-	20	-	sec
Sleep mode current	Islp_V _{CI}	DC/DC off No clock No input load Ram data retain	-	-	20	-	uA
Deep sleep mode current	Idslp_V _{CI}	DC/DC off No clock No input load Ram data not retain	-	-	2	-	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.

7.3. AC Characteristics

7.3.1. MCU Interface

The IC can support 3-wire/4-wire serial peripheral. MCU interface is pin selectable by BS1 shown in Table bellow.

	Pin Name					
MCU Interface	BS1	RES#	CS#	D/C#	SCL	SDA
4-wire serial peripheral interface (SPI)	L	RES#	CS#	DC#	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	RES#	CS#	L	SCL	SDA

Note : (1) L is connected to VSS and H is connected to VDDIO

7.3.2. MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table bellow and the write procedure 4-wire SPI is shown in Table bellow

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:(1) L is connected to VSS and H is connected to VDDIO

(2)↑ stands for rising edge of signal

(3)SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

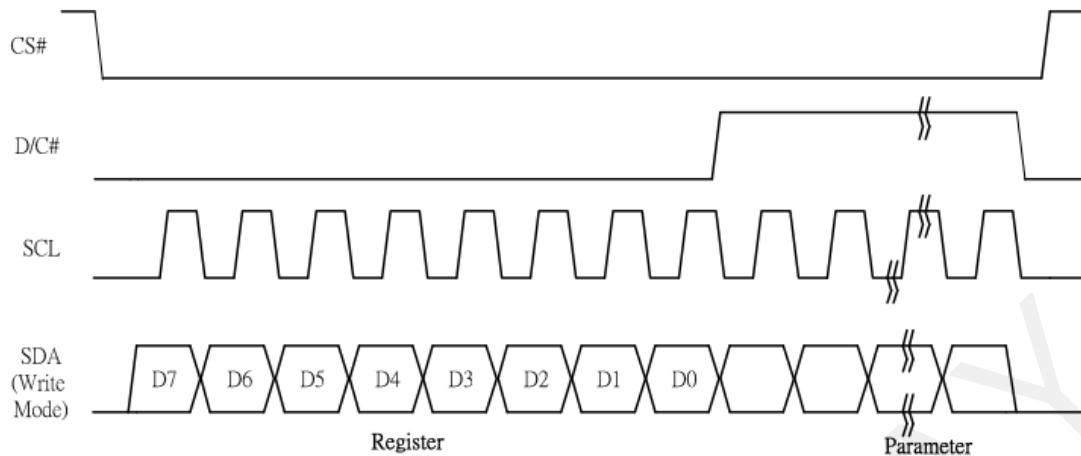


Figure 7-1 : Write procedure in 4-wire SPI mode

7.3.3. MCU Serial Interface (3-wire SPI)

MCU Serial Peripheral Interface (3-wire SPI) The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table bellow.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 7-3 shows the write procedure in 3-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note: (1) L is connected to VSS and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

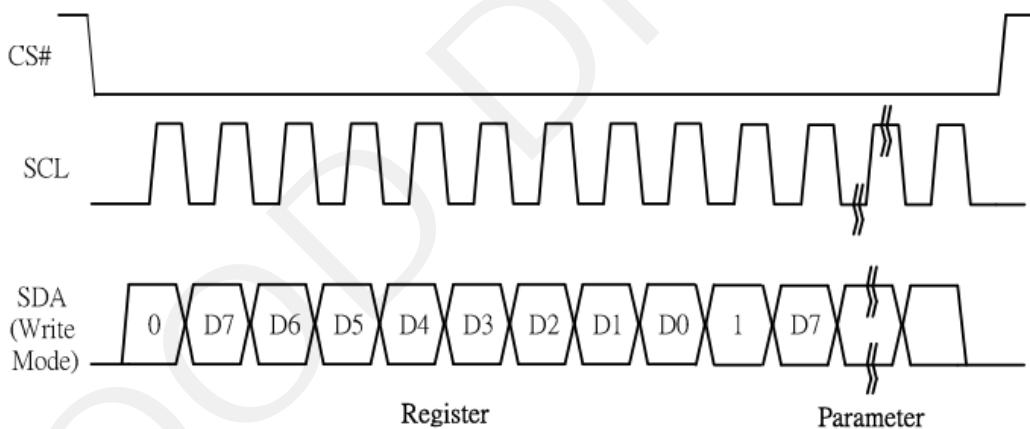
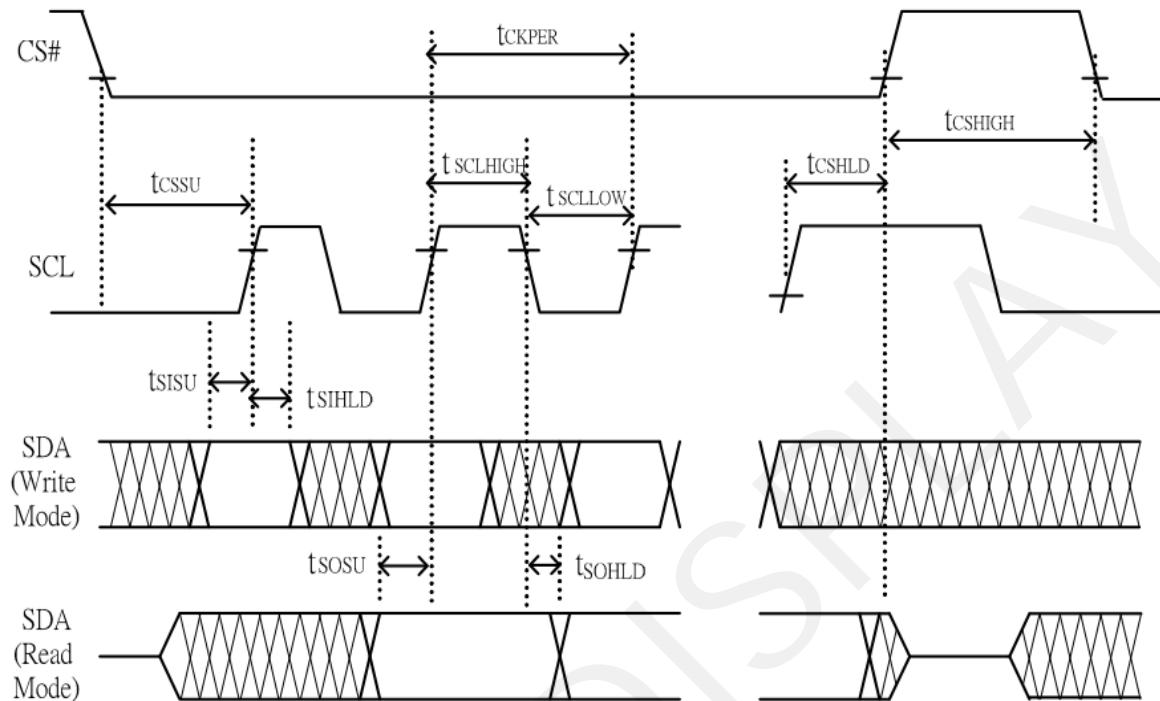


Figure 7-3 Write procedure in 3-wire SPI

7.4. Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25°C.



Write mode

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL frequency (Write Mode)	-	-	20	MHz
t _{CSSU}	Time CS# has to be low before the first rising edge of SCLK	TBD	-	-	ns
t _{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	TBD	-	-	ns
t _{CSSHLD}	Time CS# has to remain high between two transfers	TBD	-	-	ns
t _{SCLHIGH}	Part of the clock period where SCL has to remain high	TBD	-	-	ns
t _{SCLLOW}	Part of the clock period where SCL has to remain low	TBD	-	-	ns
t _{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	TBD	-	-	ns
t _{TSISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	TBD	-	-	ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL frequency (Read Mode)	-	-	2.5	MHz
t _{CSSU}	Time CS# has to be low before the first rising edge of SCLK	TBD	-	-	ns
t _{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	TBD	-	-	ns
t _{CSSHLD}	Time CS# has to remain high between two transfers	TBD	-	-	ns
t _{SCLHIGH}	Part of the clock period where SCL has to remain high	TBD	-	-	ns
t _{SCLLOW}	Part of the clock period where SCL has to remain low	TBD	-	-	ns
t _{TSOSU}	Time SO (SDA Read Mode) will be stable before the next rising edge of SCL	TBD	TBD	-	ns
t _{TOSHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL	TBD	TBD	-	ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

8. Optical Specifications

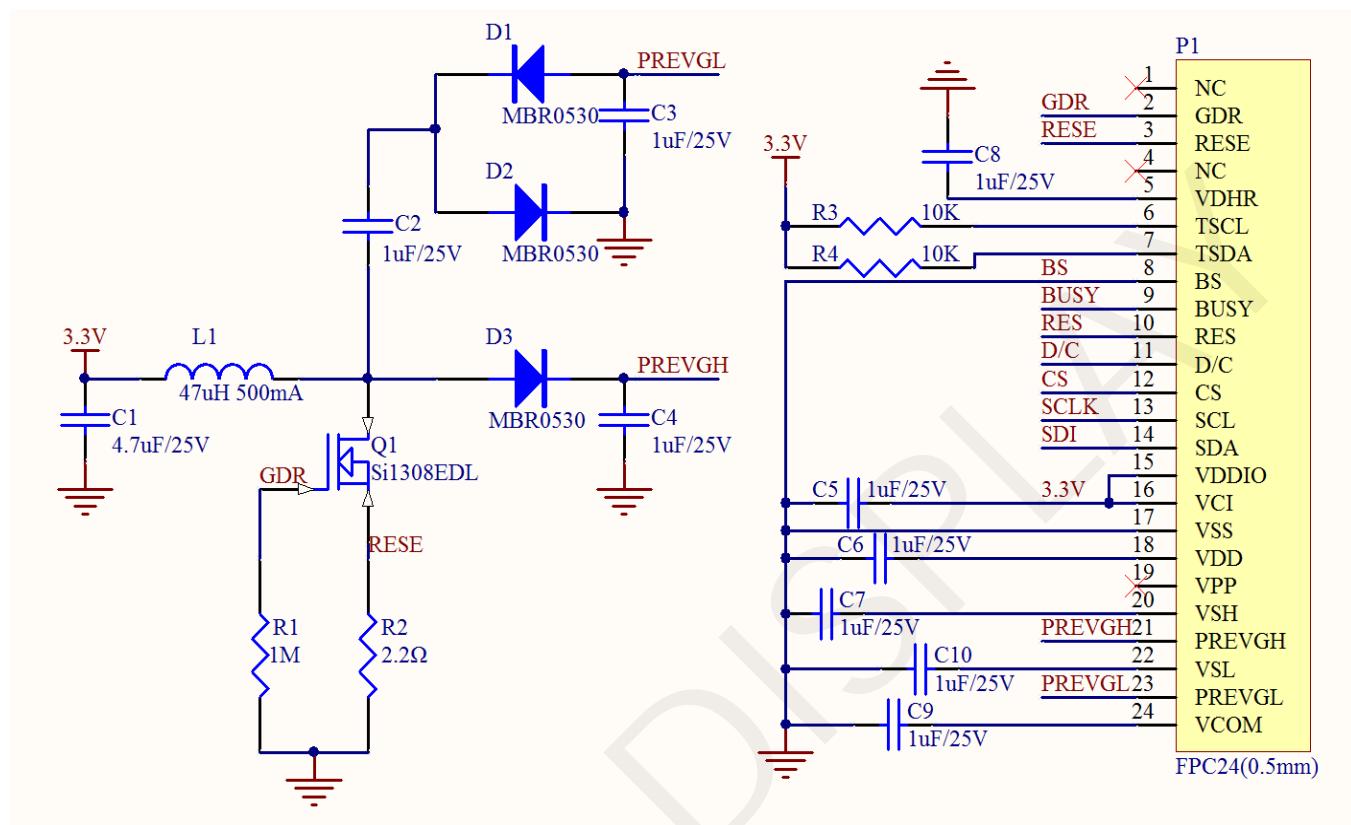
Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
GN	2Grey Level	-		DS+(WS-DS)*n(m-1)			8-3
T update	Image update time	at 25 °C		20	-	sec	
Life		Topr		1000000times or 5years			

Notes:

- 8-1. Luminance meter: Eye-One Pro Spectrophotometer.
- 8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.
- 8-3. WS: White state, DS: Dark state

9. Reference Circuit



10. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display and three-color (black, white and red/Yellow) Good Display 's E-paper Display. And it is also added the functions of USB serial port, Raspberry Pi and LED indicator light ect.

DESPI Development Kit consists of the development board and the pinboard.

More details about the Development Kit, please click to the following link:

<https://www.good-display.com/product/53/>

11. Handling, Safety and Environmental Requirements

WARNING

The display glass may break when it is dropped or bumped on a hard surface. Handle with care.

Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.

Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status

Product specification	The data sheet contains final product specifications.
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Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).

Stress above one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Product Environmental certification

RoHS

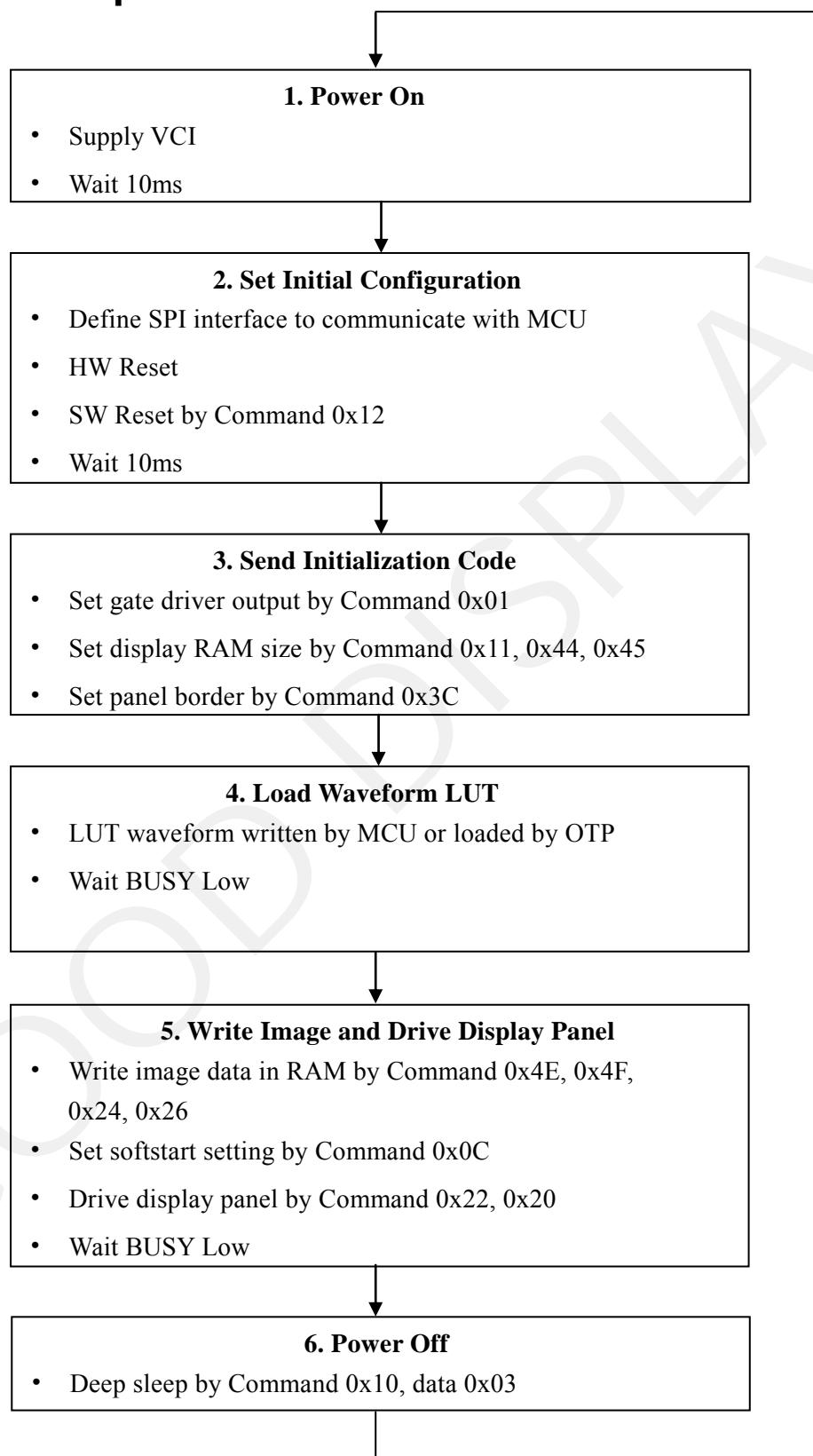
12.Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=70° C, RH=40%, 240h Test in white pattern
3	High-Temperature Operation	T=40° C, RH=35%, 240h
4	Low-Temperature Operation	T=0° C, 240h
5	High-Temperature, High-Humidity Operation	T=40° C, RH=80%, 240h
6	High Temperature, High Humidity Storage	T=50° C, RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25° C 30min]→[+70° C 30 min] : 50cycles Test in white pattern
8	UV exposure Resistance	765W/m ² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

13. Typical Operating Sequence

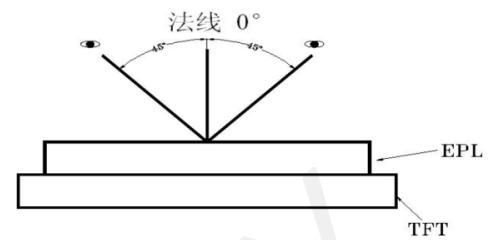
13.1 Normal Operation Flow



14. Inspection method and condition

14.1 Inspection condition

Item	Condition
Illuminance	800~1500 lux
Temperature	22°C ± 3 °C
Humidity	55±10 %RH
Distance	30±10cm
Angle	Vertical fore and aft 45
Inspection method	By eyes



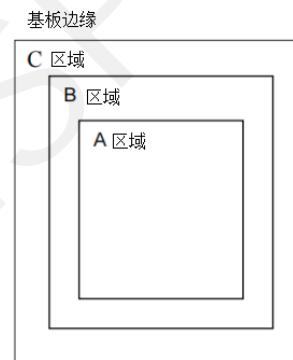
14.2 Display area

14.2.1 Zone definition:

A Zone: Active area

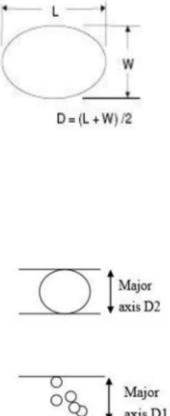
B Zone: Border zone

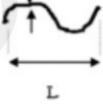
C Zone: From B zone edge to panel edge

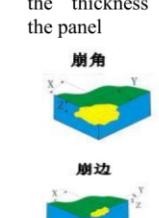


14.3 General inspection standards for products

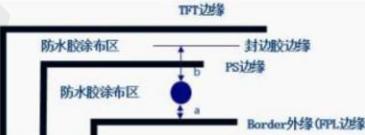
14.3.1 Appearance inspection standard

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/MIN
Spot defects	Spot defects such as dot, foreign matter, air bubble, and dent etc.	Diameter $D=(L+W)/2$ (L-length, W-width) Measuring method shown in the figure below		<p>A spec module</p> <p>The distance between the two spots should not be less than 10mm</p> <p>7.5"-13.3"Module (Not include 7.5") : $D > 1\text{mm}$ N=0 $0.5 < D \leq 0.8$ $N \leq 4$ $D \leq 0.5$ Ignore $0.8 < D \leq 1$ $N \leq 2$</p> <p>4.2"-7.5"Module (Not include 4.2") : $D > 0.5$ N=0 $0.4 < D \leq 0.5$ $N \leq 2$ $D \leq 0.25$ Ignore $0.25 < D \leq 0.4$ $N \leq 4$</p> <p>Module below 4.2" : $D > 0.5$ N=0 $0.4 < D \leq 0.5$ $N \leq 1$ $D \leq 0.25$ Ignore $0.25 < D \leq 0.4$ $N \leq 4$ $0.1\text{mm} < D \leq 0.25$ $N \leq 3/\text{cm}^2$</p> <p>B spec module</p> <p>The distance between the two spots should not be less than 5mm (Outside the AA area, ignore if not serious when checking by eyes)</p> <p>No affect on display</p>	Foreign matter $D \leq 1\text{mm}$ Pass	Check by eyes Film gauge	MIN

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/MIN
Line defects	Line defects such as scratch, hair etc.	L-Length, W-Width, $(W/L) < 1/4$ Judged by line, $(W/L) \geq 1/4$ Judged by dot		<p>A spec module</p> <p>The distance between the two lines should not be less than 5mm</p> <p>7.5"-13.3"Module (Not include 7.5") : $L > 10\text{mm}, N=0$ $W > 0.8\text{mm}$, $N=0$ $5\text{mm} \leq L \leq 10\text{mm}$, $0.5\text{mm} \leq W \leq 0.8\text{mm}$ $N \leq 2$ $L \leq 5\text{mm}$, $W \leq 0.5\text{mm}$ Ignore</p> <p>4.2"-7.5"Module (Not include 4.2") : $L > 8\text{mm}, N=0$ $W > 0.2\text{mm}$, $N=0$ $2\text{mm} \leq L \leq 8\text{mm}$, $0.1\text{mm} \leq W \leq 0.2\text{mm}$ $N \leq 4$ $L \leq 2\text{mm}$, $W \leq 0.1\text{mm}$ Ignore</p> <p>Module below 4.2" : $L > 5\text{mm}, N=0$ $W > 0.2\text{mm}$, $N=0$ $2\text{mm} \leq L \leq 5\text{mm}$, $0.1\text{mm} \leq W \leq 0.2\text{mm}$ $N \leq 4$ $L \leq 2\text{mm}$, $W \leq 0.1\text{mm}$ Ignore</p> <p>B spec module</p> <p>The distance between the two lines should not be less than 5mm (Outside the AA area, ignore if not serious when checking by eyes)</p> <p>No affect on display</p>	Ignore	Check by eyes Film gauge	MIN

Inspection item	Figure	Inspection standard	Inspection method	MAJ/ MIN
Panel chipping and crack defects	TFT panel chipping	<p>X the length, Y the width, Z the chipping height, T the thickness of the panel</p>  <p>Chipping at the edge: Module over 7.5" (Include 7.5") : $X \leq 6\text{mm}, Y \leq 1\text{mm}, Z \leq T, N=3$ Allowed</p> <p>Module below 7.5" (Not include 7.5"): $X \leq 3\text{mm}, Y \leq 1\text{mm}, Z \leq T, N=3$ Allowed</p> <p>Chipping on the corner: IC side $X \leq 2\text{mm}, Y \leq 2\text{mm}$, Non-IC side $X \leq 1\text{mm}, Y \leq 1\text{mm}$. Allowed</p> <p>Note:</p> <ol style="list-style-type: none"> 1、 Chipping should not damage the edge wiring. If it does not affect the display, allowed 2、 The size of the chipping is larger than the above conditions but the display is normal, it can be taken as the B spec. 	Check by eyes, Film gauge	MIN
	Crack	Crack at any zone of glass , Not allowed	Check by eyes, Film gauge	MIN
	Burr edge	No exceed the positive and negative deviation of the outline dimensions $X+Y \leq 0.2\text{mm}$ Allowed	Calliper	MIN
	Curl of panel	Curl height $H \leq \text{Total panel length } 1\%$ Allowed	Check by eyes	MIN

Remarks: The total number of defects in a single piece of A-spec glass is not allowed to exceed 4.

Inspection item	Figure	Inspection standard	Inspection method	MAJ / MIN
PS defect	Water proof film	 <ol style="list-style-type: none"> 1. Waterproof film damage, wrinkled, open edge, not allowed 2. Exceeding the edge of module(according to the lamination drawing) Not allowed 3. Edge warped exceeds height of technical file, not allowed 	Check by eyes	MIN
RTV defect	Adhesive effect	Adhesive height exceeds the display surface, not allowed	Check by eyes	MIN
		<ol style="list-style-type: none"> 1. Overflow, exceeds the panel side edge, affecting the size, not allowed 2. No adhesive at panel edge $\leq 1\text{mm}$, no exposure of wiring, allowed 3. No adhesive at edge and corner $1*1\text{mm}$, no exposure of wiring, allowed 		
	Adhesive re-fill	Protection adhesive, coverage width within $W \leq 1.5\text{mm}$, no break of adhesive, allowed	Check by eyes	MIN
EC defect	Adhesive bubble	 <ol style="list-style-type: none"> 1、 Effective edge sealing area of hot melt products $\geq 1/2$ edge sealing area; 2、 Bubble $a+b/2 \geq 1/2$ effective width, $N \leq 3$, spacing $\geq 5\text{mm}$, allowed <p>No exposure of wiring, allowed</p>	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/MIN
EC defect	Adhesive effect		1. Overflow, exceeds the panel side edge, affecting the size, not allowed 2. No adhesive at panel edge $\leq 1\text{mm}$, no exposure of wiring, allowed 3. No adhesive at edge and corner $1*1\text{mm}$, no exposure of wiring, allowed 4. Adhesive height exceeds the display surface, not allowed	Visual, caliper	MIN
Silver dot adhesive defect	Silver dot adhesive		1. Single silver dot dispensing amount $\geq 1\text{mm}$, allowed 2. One of the double silver dot dispensing amount is $\geq 1\text{mm}$ and the other has adhesive (no reference to 1mm) Allowed	Visual	MIN
			Silver dot dispensing residue on the panel $\leq 0.2\text{mm}$, allowed	Film gauge	MIN
FPC defect	FPC wiring		FPC, TCP damage / gold finger peroxidation, adhesive residue, not allowed	Visual	MIJ
	FPC golden finger		The height of burr edge of TCP punching surface $\geq 0.4\text{mm}$, not allowed	Caliper	MIN
	FPC damage/cr ease		Damage and breaking, not allowed Crease does not affect the electrical performance display, allowed	Check by eyes	MIN

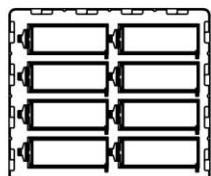
Inspection item		Figure	Inspection standard	Inspection method	MAJ/MIN
Protective film defect	Protective film	Scratch and crease on the surface but no affect to protection function, allowed		Check by eyes	MIN
		Adhesive at edge $L \leq 5\text{mm}$, $W \leq 0.5\text{mm}$, $N=2$, no entering into viewing area		Check by eyes	MIN
Stain defect	Stain	If stain can be normally wiped clean by > 99% alcohol, allowed		Visual	MIN
Pull tab defect	Pull tab	The position and direction meet the document requirements, and ensure that the protective film can be pulled off.		Check by eyes/ Manual pulling	MIN
Shading tape defect	Shading tape	Tilt $\leq 10^\circ$, flat without warping, completely covering the IC.		Check by eyes/ Film gauge	MIN
Stiffener	Stiffener	Flat without warping. Exceeding the left and right edges of the FPC is not allowed. Left and right can be less than 0.5mm from FPC edge		Check by eyes	MIN
Label	Label/ Spraying code	The content meets the requirements of the work sheet. The attaching position meets the requirements of the technical documents.		Check by eyes	MIN

Remarks: The definition of other appearance B spec products, no affect to the display, and no entering into the viewing area.

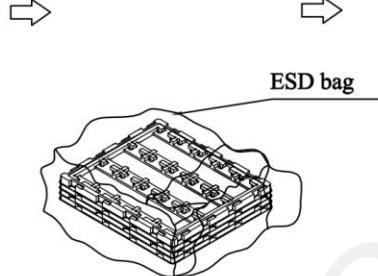
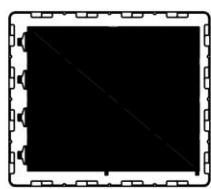
15. Packing

PACKLING ORDER:

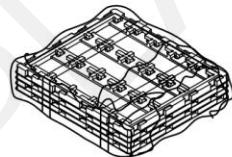
1) Putting 8 pcs Modules on each PET tray. And cover a dedicated EPE film.



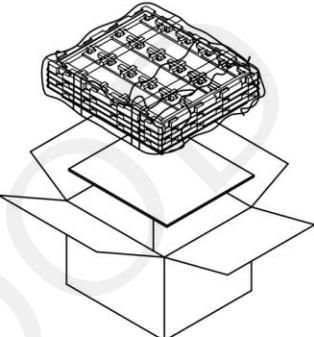
2) Putting 13 pcs PET trays together with 1 empty tray on the top of PET tray. Insert in the ESD bag, add desiccant in the ESD bag.



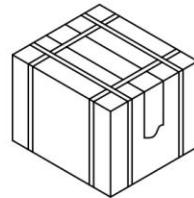
3) the tray together with adhesive tape



4) Putting into one outcarton



5) Packing finished



Note: 8 pcs in a tray, 13 trays in a out carton, so $8 \times (14 - 1) = 104$ pcs/Outcarton

Dimension (Out carton): 394*344*138mm

16. Precautions

- (1) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
- (4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue
- (6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.