



# 11.6 inch E-paper Display Series



**GDEY116Z91**

Dalian Good Display Co., Ltd.

# Product Specifications

Customer	Standard
Description	11.6" E-PAPER DISPLAY
Model Name	GDEY116Z91
Date	2022/06/20
Revision	1.0

	Design Engineering		
	Approval	Check	Design

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## 1. Over View

GDEY116Z91 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black and red full display capabilities. The 11.60 inch active area contains  $960 \times 640$  pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

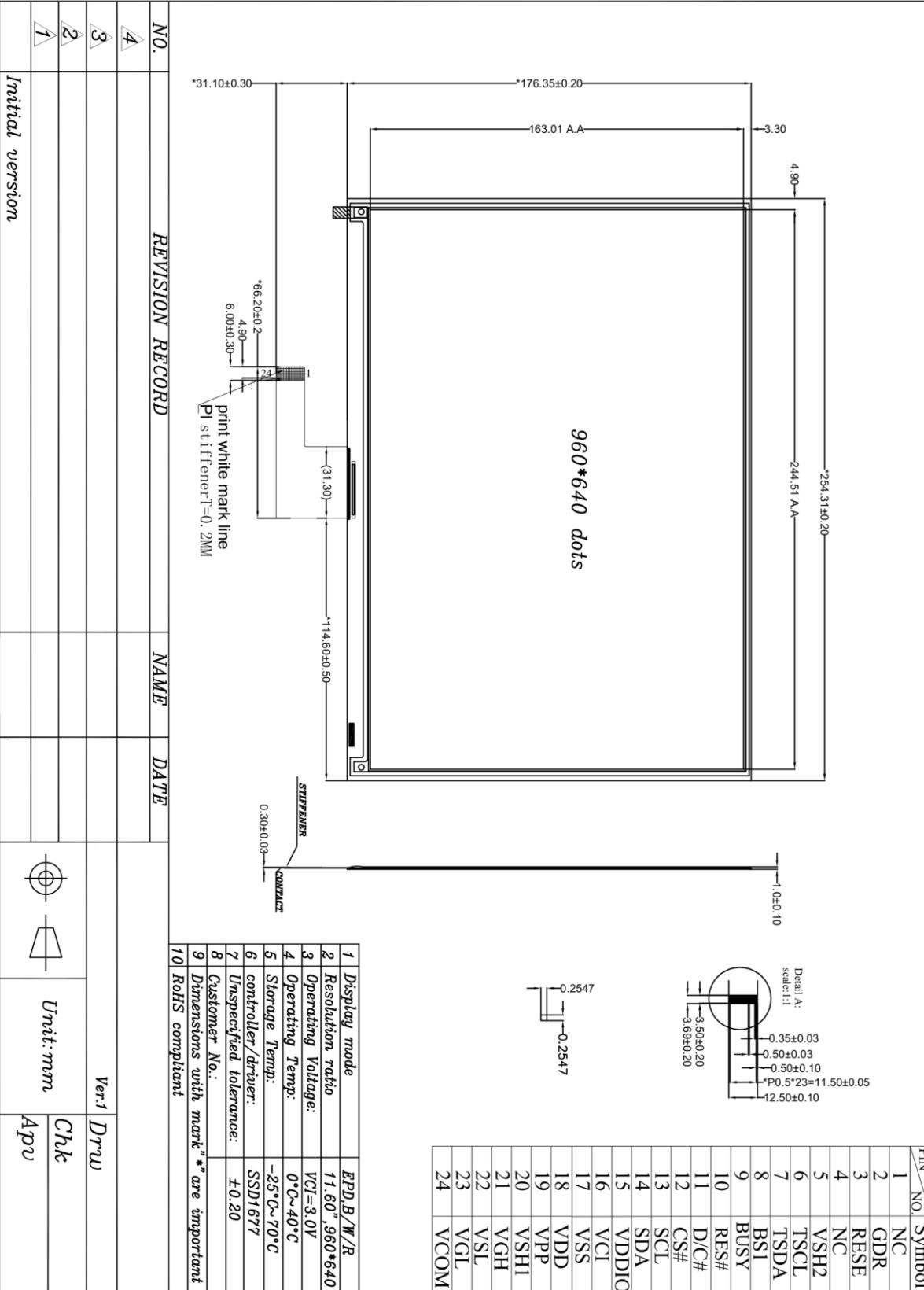
## 2. Features

- $960 \times 640$  pixels display
- High contrast High reflectance
- Ultra wide viewing angle Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform can stored in On-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I<sup>2</sup>C signal master interface to read external temperature sensor
- Built-in temperature sensor

## 3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	11.6	Inch	
Display Resolution	$960(H) \times 640(V)$	Pixel	Dpi:99
Active Area	$244.51 \times 163.01$	mm	
Pixel Pitch	$0.2547 \times 0.2547$	mm	
Pixel Configuration	Rectangle		
Outline Dimension	$254.31(H) \times 176.35(V) \times 1.0(D)$	mm	
Weight	TBD	g	

#### 4. Mechanical Drawing of EPD module

<b>CUSTOMER'S APPROVED:</b>			<b>DATE:</b>	<b>PAGE: 1 / 1</b>																																																																	
 <p><b>Front View Dimensions:</b></p> <ul style="list-style-type: none"> <li>Total width: 176.35 ± 0.20 mm</li> <li>Total height: 254.31 ± 0.20 mm</li> <li>Panel area width: 163.01 A.A.</li> <li>Panel area height: 244.51 A.A.</li> <li>Panel thickness: 3.30 mm</li> <li>Panel side gap: 4.90 mm</li> <li>Panel top/bottom gap: 1.0 ± 0.10 mm</li> <li>Panel center gap: 0.35 ± 0.03 mm</li> <li>Panel side gap: 0.50 ± 0.03 mm</li> <li>Panel side gap: 0.50 ± 0.10 mm</li> <li>Panel side gap: P0.5'23 = 11.50 ± 0.05 mm</li> <li>Panel side gap: 12.50 ± 0.10 mm</li> </ul> <p><b>Pinout and Dimensions:</b></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>PIN NO.</th> <th>Symbol</th> </tr> </thead> <tbody> <tr><td>1</td><td>NC</td></tr> <tr><td>2</td><td>GDR</td></tr> <tr><td>3</td><td>RESE</td></tr> <tr><td>4</td><td>NC</td></tr> <tr><td>5</td><td>VSH2</td></tr> <tr><td>6</td><td>TSCL</td></tr> <tr><td>7</td><td>TSDA</td></tr> <tr><td>8</td><td>BS1</td></tr> <tr><td>9</td><td>BUSY</td></tr> <tr><td>10</td><td>RES#</td></tr> <tr><td>11</td><td>D/C#</td></tr> <tr><td>12</td><td>CS#</td></tr> <tr><td>13</td><td>SCL</td></tr> <tr><td>14</td><td>SDA</td></tr> <tr><td>15</td><td>VDDIO</td></tr> <tr><td>16</td><td>VCI</td></tr> <tr><td>17</td><td>VSS</td></tr> <tr><td>18</td><td>VDD</td></tr> <tr><td>19</td><td>VPP</td></tr> <tr><td>20</td><td>VSH1</td></tr> <tr><td>21</td><td>VGH</td></tr> <tr><td>22</td><td>VSL</td></tr> <tr><td>23</td><td>VGL</td></tr> <tr><td>24</td><td>VCOM</td></tr> </tbody> </table> <p><b>REVISION RECORD</b></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>NO.</th> <th>NAME</th> <th>DATE</th> </tr> </thead> <tbody> <tr><td>4</td><td></td><td>Ver. 1 DrvU</td></tr> <tr><td>3</td><td></td><td>Chk</td></tr> <tr><td>2</td><td></td><td>Apv</td></tr> <tr><td>1</td><td>Initial version</td><td></td></tr> </tbody> </table>					PIN NO.	Symbol	1	NC	2	GDR	3	RESE	4	NC	5	VSH2	6	TSCL	7	TSDA	8	BS1	9	BUSY	10	RES#	11	D/C#	12	CS#	13	SCL	14	SDA	15	VDDIO	16	VCI	17	VSS	18	VDD	19	VPP	20	VSH1	21	VGH	22	VSL	23	VGL	24	VCOM	NO.	NAME	DATE	4		Ver. 1 DrvU	3		Chk	2		Apv	1	Initial version	
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## 5. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, /O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when  
–Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

<b>BS1 State</b>	<b>MCU Interface</b>
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

## 6. Electrical Characteristics

### 6.1 Absolute Maximum Rating

<b>Parameter</b>	<b>Symbol</b>	<b>Rating</b>	<b>Unit</b>
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to V <sub>DDIO</sub> +0.5	V
Logic Output voltage	VOUT	-0.5 to V <sub>DDIO</sub> +0.5	V
Operating Temp range	TOPR	0 to +40	°C
Storage Temp range	TSTG	-25 to +70	°C
Optimal Storage Temp	TSTG <sub>O</sub>	23±2	°C
Optimal Storage Humidity	HSTG <sub>O</sub>	55±10	%RH

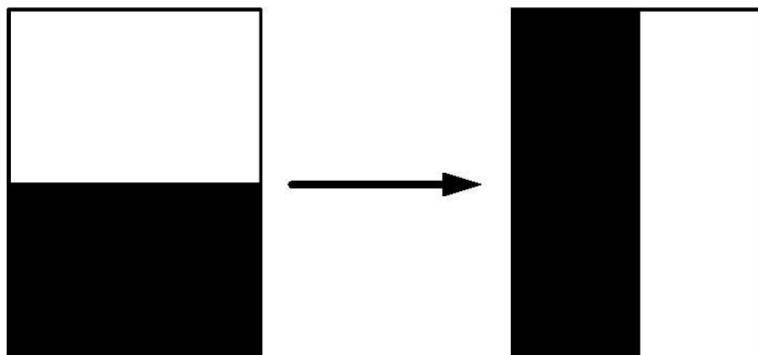
Note:Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

## 6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25 °C

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V <sub>SS</sub>	-		-	0	-	V
Logic supply voltage	V <sub>CI</sub>	-	VCI	2.2	3.0	3.3	V
Core logic voltage	V <sub>DD</sub>		VDD	1.7	1.8	1.9	V
High level input voltage	V <sub>IH</sub>	-	-	0.8 V <sub>DDIO</sub>	-	-	V
Low level input voltage	V <sub>IL</sub>	-	-	-	-	0.2 V <sub>DDIO</sub>	V
High level output voltage	V <sub>OH</sub>	IOH = -100uA	-	0.9 V <sub>DDIO</sub>	-	-	V
Low level output voltage	V <sub>OL</sub>	IOL = 100uA	-	-	-	0.1V <sub>DDIO</sub>	V
Typical power	P <sub>TYP</sub>	V <sub>CI</sub> =3.0V	-	-	TBD	-	mW
Deep sleep mode	P <sub>STPY</sub>	V <sub>CI</sub> =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_V <sub>CI</sub>	V <sub>CI</sub> =3.0V	-	-	TBD	-	mA
Image update time	-	25 °C	-	-	25	-	sec
Sleep mode current	Islp_V <sub>CI</sub>	DC/DC off No clock No input load Ram data retain	-	-	25	-	uA
Deep sleep mode current	Idslp_V <sub>CI</sub>	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by NEWFACE.

## 6.3 Panel AC Characteristics

### 6.3.1 MCU Interface selection

It support 4-wire or 3-wire serial peripheral MCU interface, which is pin selectable by BS1 pin. The interface pin assignment for different MCU interfaces is shown in Table 6-1.

**Table 6-1: Interface pin assignment for different MCU interfaces**

MCU Interface	Pin Name						
	BS1	RES#	CS#	D/C#	SCL	SDI	SDO
4-wire serial peripheral interface (SPI)	L	RES#	CS#	DC#	SCL	SDA	
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	RES#	CS#	L	SCL	SDA	

**Note:**

- (1) L is connected to V<sub>SS</sub> and H is connected to V<sub>DDIO</sub>
- (2) SDI and SDO are connected to be SDA pin for bi-directional data access

### 6.3.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data input SDI, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 6-2 and the write procedure in 4-wire SPI is shown in Figure 6-1.

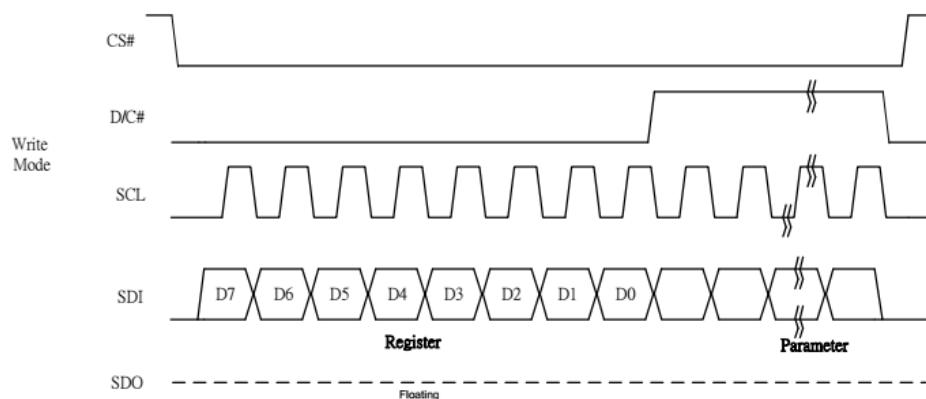
**Table 6-2 : Control pins status of 4-wire SPI**

Function	SCL pin	SDI pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

**Note:**

- (1) L is connected to V<sub>SS</sub> and H is connected to V<sub>DDIO</sub>
- (2) ↑ stands for rising edge of signal

SDI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.



**Figure 6-1 : Write procedure in 4-wire SPI mode**

In the read operation, after CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data output SDO bit shifting sequence is D7, D6, to D0 bit. Figure 6-2 shows the read procedure in 4-wire SPI.

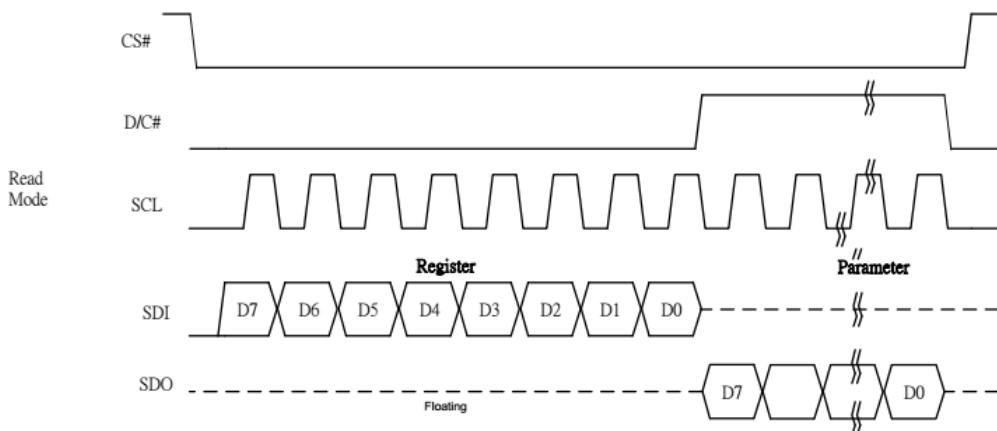


Figure 6-2 : Read procedure in 4-wire SPI mode

### 6.3.3 MCU Serial Interface(3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data input SDI, and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3. In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 6-3 shows the write procedure in 3-wire SPI

Table 6-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDI pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

**Note:**

- (1) L is connected to V<sub>SS</sub> and H is connected to V<sub>DDIO</sub>
- (2) ↑ stands for rising edge of signal

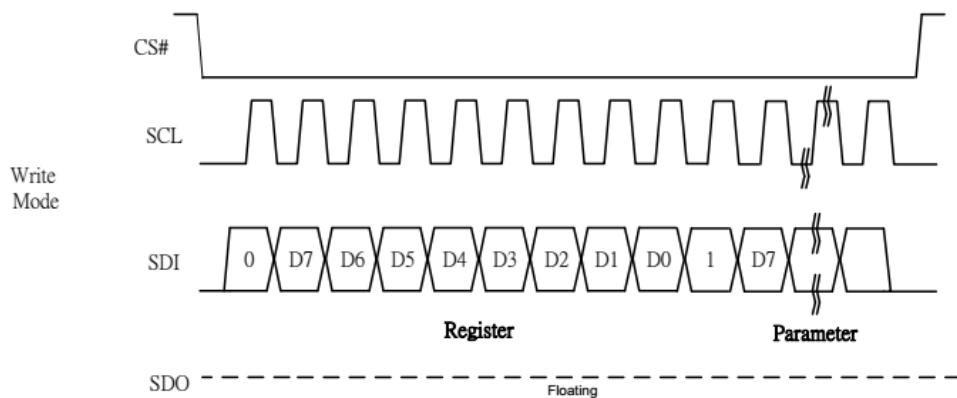


Figure 6-3 : Write procedure in 3-wire SPI

In the read operation, serial data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data output SDO bit shifting sequence is D7, D6, to D0 bit. Figure 6-4 shows the read procedure in 3-wire SPI.

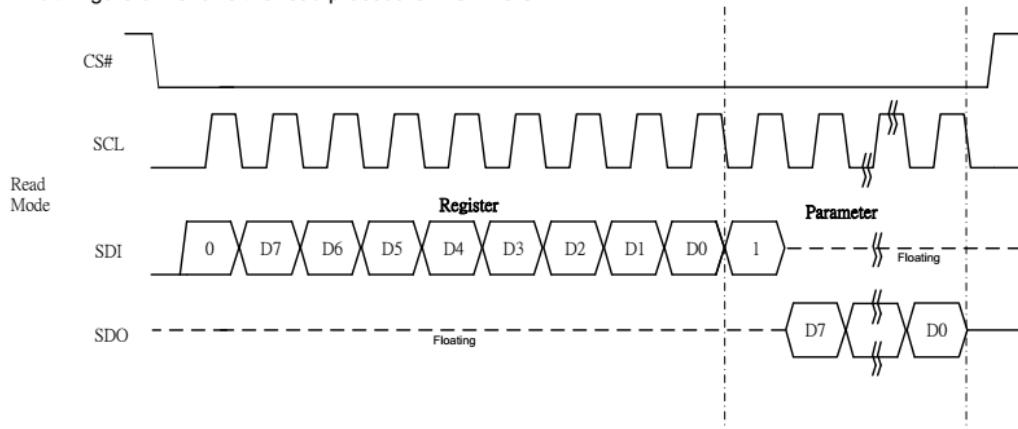


Figure 6-4 : Read procedure in 3-wire SPI mode

### 6.3.4 Interface Timing

The following specifications apply for: VDDIO - VSS = 2.2V to 3.7V, CL=30pF

Table 12-1 : Serial Peripheral Interface Timing Characteristics

#### Write mode

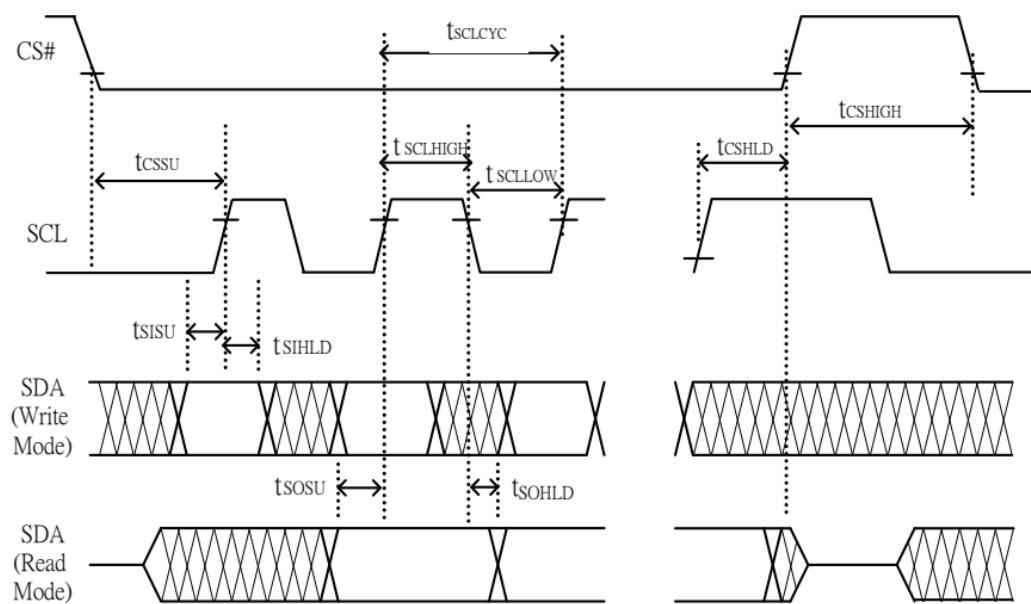
Symbol	Parameter	Min	Typ	Max	Unit
$f_{SCL}$	SCL frequency (Write Mode)			20	MHz
$t_{CSSU}$	Time CS# has to be low before the first rising edge of SCLK	20			ns
$t_{CSHLD}$	Time CS# has to remain low after the last falling edge of SCLK	20			ns
$t_{CSHIGH}$	Time CS# has to remain high between two transfers	100			ns
$t_{SCLCYC}$	SCL cycle time	50			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	25			ns
$t_{SCLLOW}$	Part of the clock period where SCL has to remain low	25			ns
$t_{SISU}$	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
$t_{SIHLD}$	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

#### Read mode

Symbol	Parameter	Min	Typ	Max	Unit
$f_{SCL}$	SCL frequency (Read Mode)			2.5	MHz
$t_{CSSU}$	Time CS# has to be low before the first rising edge of SCLK	100			ns
$t_{CSHLD}$	Time CS# has to remain low after the last falling edge of SCLK	50			ns
$t_{CSHIGH}$	Time CS# has to remain high between two transfers	250			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	180			ns
$t_{SCLLOW}$	Part of the clock period where SCL has to remain low	180			ns
$t_{SO SU}$	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
$t_{SO HLD}$	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

**Figure 12-1: SPI timing diagram**



## 7. Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting Set A[9:0]=2A7h[POR] ,680MUX Set B[2:0]=000[POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		
0	1		0	0	0	0	0	B2	B1	B0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage control	SetGate Driving voltage A[4:0]=17h[POR], VGH at 20V[POR] VGH setting from 12V to 20V
0	1		0	0	0	A4	A3	A2	A1	A0		
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage control	SetSource Driving voltage A[7:0]= 41h[POR], VSH1 at 15V B[7:0]=A8h[POR], VSH2 at 5.0V C[7:0]= 32h[POR], VSL at -15V
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control
0	1		0	0	0	0	0	0	A <sub>1</sub>	A <sub>0</sub>		A[1:0] : Description 00 Normal Mode [POR] 11 Enter Deep Sleep Mode
												After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high.
0	0	11	0	0	0	1	0	0	0	1		Define data entry sequence A [1:0] = ID[1:0]Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Data Entry mode setting	
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation ,BUSY pad will output high. Note: RAM are unaffected by this command.

0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0]=7FFh[POR]
0	1		A11	A10	A9	A8	A7	A6	A5	A4		
0	1		A3	A2	A1	A0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.
0	0	20	0	0	1	0	0	0	0	0	Display Update Control 1	RAM content option for Display Update A[7:0]=00h[POR] A[7:4] Red RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content
0	1		A7	A6	A5	A4	A3	A2	A1	A0		A[3:0] BW RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content
0	0	21	0	0	1	0	0	0	0	1		Display Update Sequence Option: Enable the stage for Master Activation
1			A7	A6	A5	A4	A3	A2	A1	A0		<b>Setting for LUT from MCU</b> Enable Clock Signal, Then Enable Analog Then PATTERN DISPLAY C7 Then Disable Analog Then Disable OSC
												<b>Setting for LUT from OTP according to external Temperature Sensor operation</b> Then Enable Analog Then Load LUT 90
												Then Enable Analog Then PATTERN DISPLAY 47 Then Disable Analog Then Disable OSC
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	After this command, data entries will be written into the 1RAM until another command is written. Address pointers will advance accordingly. For Write pixel: Content of write RAM(BW)=1 For Black pixel: Content of write RAM(BW)=0
1			A7	A6	A5	A4	A3	A2	A1	A0		
0	0	24	0	0	1	0	0	1	0	0	Write RAM (BW)	

0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the 2 RAM until another command is written. Address pointers will advance accordingly. For RED pixel: Content of write RAM(RED)=1 For White/Black pixel: Content of write RAM(RED)=0
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Set A[7:0]=50h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read	Read Register stored in OTP: 1. A[7:0]~B[7:0]: VCOM Information 2. C[7:0]~G[7:0]: Display mode 3. H[7:0]~K[7:0]: Waveform Version [4bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	J0		
1	1		K7	K6	K5	K4	K3	K2	K1	K0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x21] A[5]: HV Ready Detection flag [POR=1] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A5	A4	0	0	A1	A0		
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [105 bytes].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		

0	0	3A	0	0	1	1	1	0	1	0	Reserved	Reserved
0	0	3B	0	0	1	1	1	0	1	1	Reserved	Reserved
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0]=C0h[POR], set VBD as HIZ A[7:6] Select VBD option
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	0	0	A <sub>1</sub>	A <sub>0</sub>		A[7:6] Select VBD as 00 GS Transition Define A[1:0] 01 Fix Level Define A [5:4] 10 VCOM 11[POR] HIZ
												A [5:4] Fix Level Setting for VBD A[5:4] VBD level 00[POR] VSS 01 VSH1 10 VSL 11 VSH2
												A[1:0]) BW Transition setting for VBD A[1:0] VBD Transition 00 [POR] LUT0 01 LUT1 10 LUT2 11 LUT3
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[9:0]: XSA[9:0], X Start, POR = 000h B[9:0]: XEA[9:0], X End, POR = 3BFh
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	1		-	-	-	-	-	-	A <sub>9</sub>	A <sub>8</sub>		
0	1		B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	1		-	-	-	-	-	-	B <sub>9</sub>	B <sub>8</sub>		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[9:0]: YSA[9:0], Y Start, POR = 000h B[9:0]: YEA[9:0], Y End, POR = 2A7h
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	1		-	-	-	-	-	-	A <sub>9</sub>	A <sub>8</sub>		
0	1		B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	1		-	-	-	-	-	-	B <sub>9</sub>	B <sub>8</sub>		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[9:0]: 000h[POR]
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	1		-	-	-	-	-	-	A <sub>9</sub>	A <sub>8</sub>		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[9:0]: 000h[POR]
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	1		-	-	-	-	-	-	A <sub>9</sub>	A <sub>8</sub>		
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		

## 8. Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
GN	2Grey Level	-		DS+(WS-DS)*n(m-1)			8-3
T update	Image update time	at 25 °C		25	-	sec	
Life		Topr		1000000times or 5years			

Notes: 8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3. WS: White state, DS: Dark state

## 9. Handling, Safety and Environment Requirements

### Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

### Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

## 10. Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=70°C, RH=40%, 240h Test in white pattern
3	High-Temperature Operation	T=40°C, RH=35%, 240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T=40°C, RH=80%, 168h
6	High Temperature, High Humidity Storage	T=50°C, RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m <sup>2</sup> for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell,not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display,no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display,including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

## 11. Typical Application Circuit

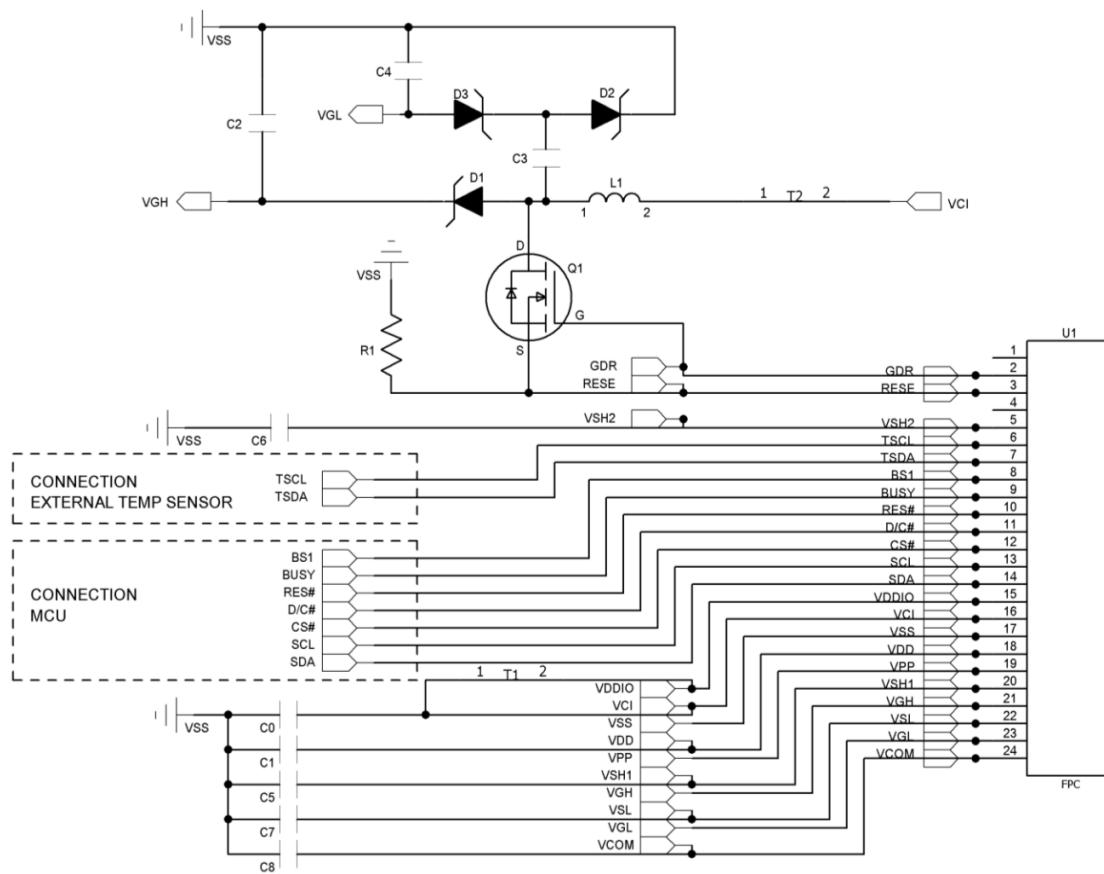


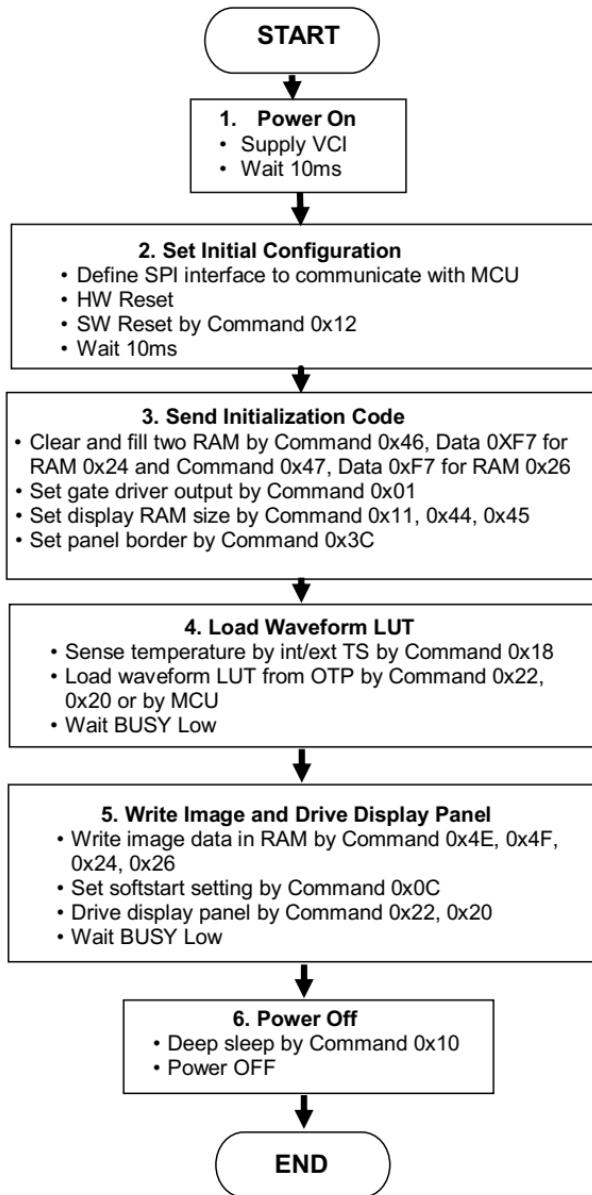
Table 13-1: Component list for SSD1677 application circuit

Part Name	Value	Reference Part/ Requirement
C0-C1	1uF	0603; X5R/X7R; Voltage Rating: 6V
C2-C7	4.7uF	0805; X5R/X7R; Voltage Rating: 25V
C8	1uF	0805; X7R; Voltage Rating: 25V
R1	2.2 Ohm	0805; 1%
D1-D3	Diode	MBR0530
Q1	NMOS	Si1304BDL
L1	47uH	CDRH2D18/ LDNP-470NC
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

Remark: Component value is subjected to change and depends on panel loading.

## 12. Typical Operating Sequence

### 12.1 Normal Operation Flow



## 12.2 Normal Operation Reference Program Code

TBD

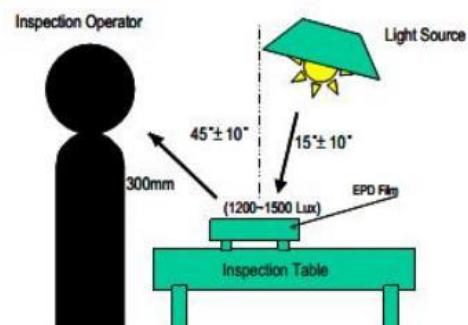
## 13. Part Number Definition

TBD

## 14. Inspection method and condition

### 14.1 Inspection condition

Item	Condition
Illuminance	$\geq 1000$ lux
Temperature	$22^{\circ}\text{C} \pm 3^{\circ}\text{C}$
Humidity	45-65 % RoHS
Distance	$\geq 30\text{cm}$
Angle	$\pm 45^{\circ}$
Inspection method	By eyes



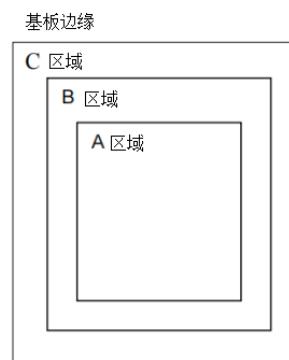
### 14.2 Display area

#### 14.2.1 Zone definition:

A Zone: Active area

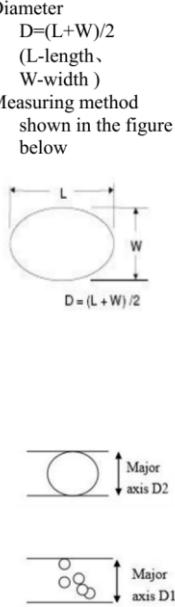
B Zone: Border zone

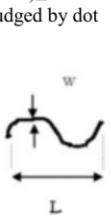
C Zone: From B zone edge to panel edge

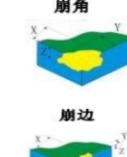


## 14.3 General inspection standards for products

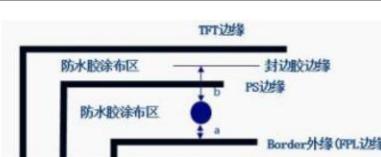
### 14.3.1 Appearance inspection standard

Inspection item	Figure	A zone inspection standard	B/C zone	Inspection method	MAJ/MIN
Spot defects	<p>Diameter <math>D=(L+W)/2</math>  (L-length, W-width)  Measuring method shown in the figure below</p>  <p>The distance between the two spots should not be less than 10mm</p>	<p>7.5"-13.3"Module (Not include 7.5") :  <math>D&gt;1\text{mm}</math> <math>N=0</math> <math>0.5 &lt; D \leq 0.8</math>  <math>N \leq 4</math> <math>D \leq 0.5</math>  Ignore <math>0.8 &lt; D \leq 1</math> <math>N \leq 2</math></p> <p>4.2"-7.5"Module (Not include 4.2") :  <math>D&gt;0.5</math> <math>N=0</math> <math>0.4 &lt; D \leq 0.5</math>  <math>N \leq 2</math> <math>D \leq 0.25</math>  Ignore <math>0.25 &lt; D \leq 0.4</math> <math>N \leq 4</math></p> <p>Module below 4.2" :  <math>D&gt;0.5</math> <math>N=0</math> <math>0.4 &lt; D \leq 0.5</math>  <math>N \leq 1</math>  <math>D \leq 0.25</math> Ignore <math>0.25 &lt; D \leq 0.4</math>  <math>N \leq 4</math>  <math>0.1\text{mm} &lt; D \leq 0.25</math> <math>N \leq 3/\text{cm}^2</math></p>	Foreign matter $D \leq 1\text{mm}$ Pass	Check by eyes Film gauge	MIN

Inspection item	Figure	A zone inspection standard	B/C zone	Inspection method	MAJ/MIN
Line defects	<p>L-Length, W-Width, <math>(W/L) &lt; 1/4</math>  Judged by line,  <math>(W/L) \geq 1/4</math>  Judged by dot</p>  <p>The distance between the two lines should not be less than 5mm</p>	<p>7.5"-13.3"Module (Not include 7.5") :  <math>L &gt; 10\text{mm}, N=0</math> <math>W &gt; 0.8\text{mm}</math>, <math>N=0</math>  <math>5\text{mm} \leq L \leq 10\text{mm}</math>, <math>0.5\text{mm} \leq W \leq 0.8\text{mm}</math>  <math>N \leq 2</math> <math>L \leq 5\text{mm}</math>, <math>W \leq 0.5\text{mm}</math> Ignore</p> <p>4.2"-7.5"Module (Not include 4.2") :  <math>L &gt; 8\text{mm}, N=0</math> <math>W &gt; 0.2\text{mm}</math>, <math>N=0</math>  <math>2\text{mm} \leq L \leq 8\text{mm}</math>, <math>0.1\text{mm} \leq W \leq 0.2\text{mm}</math> <math>N \leq 4</math>  <math>L \leq 2\text{mm}</math>, <math>W \leq 0.1\text{mm}</math> Ignore</p> <p>Module below 4.2" :  <math>L &gt; 5\text{mm}, N=0</math> <math>W &gt; 0.2\text{mm}</math>, <math>N=0</math>  <math>2\text{mm} \leq L \leq 5\text{mm}</math>, <math>0.1\text{mm} \leq W \leq 0.2\text{mm}</math> <math>N \leq 4</math>  <math>L \leq 2\text{mm}</math>, <math>W \leq 0.1\text{mm}</math> Ignore</p>	Ignore	Check by eyes Film gauge	MIN

Inspection item	Figure	Inspection standard	Inspection method	MAJ / MIN
Panel chipping and crack defects	TFT panel chipping	<p>X the length, Y the width, Z the chipping height, T the thickness of the panel</p>  <p>Chipping at the edge: Module over 7.5" (Include 7.5") : <math>X \leq 6\text{mm}, Y \leq 1\text{mm}, Z \leq T, N=3</math> Allowed Module below 7.5"(Not include 7.5"): <math>X \leq 3\text{mm}, Y \leq 1\text{mm}, Z \leq T, N=3</math> Allowed</p> <p>Chipping on the corner: IC side <math>X \leq 2\text{mm}, Y \leq 2\text{mm}</math>, Non-IC side <math>X \leq 1\text{mm}, Y \leq 1\text{mm}</math>. Allowed</p> <p>Note:</p> <ol style="list-style-type: none"> <li>1、 Chipping should not damage the edge wiring. If it does not affect the display, allowed</li> <li>2、 The size of the chipping is larger than the above conditions but the display is normal, it can be taken as the B spec.</li> </ol>	Check by eyes, Film gauge	MIN
	Crack		Crack at any zone of glass , Not allowed	Check by eyes, Film gauge
	Burr edge		No exceed the positive and negative deviation of the outline dimensions $X+Y \leq 0.2\text{mm}$ Allowed	Calliper
	Curl of panel		Curl height $H \leq \text{Total panel length } 1\%$ Allowed	Check by eyes

Remarks: The total number of defects in a single piece of A-spec glass is not allowed to exceed 4.

Inspection item	Figure	Inspection standard	Inspection method	MAJ / MIN	
PS defect	Water proof film		1. Waterproof film damage, wrinkled, open edge, not allowed 2. Exceeding the edge of module(according to the lamination drawing) Not allowed 3. Edge warped exceeds height of technical file, not allowed	Check by eyes	MIN
RTV defect	Adhesive effect		Adhesive height exceeds the display surface, not allowed	Check by eyes	MIN
			1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2 .No adhesive at panel edge $\leq 1\text{mm}$ , no exposure of wiring, allowed 3. No adhesive at edge and corner $1*1\text{mm}$ , no exposure of wiring, allowed		
			Protection adhesive, coverage width within $W \leq 1.5\text{mm}$ , no break of adhesive, allowed		
	Adhesive re-fill		Dispensing is uniform, without obvious concave and breaking, bubbling and swell, not higher than the upper surface of the PS, and the diameter of the adhesive re-filling is not more than 8mm, allowed	Check by eyes	MIN
EC defect	Adhesive bubble		1、 Effective edge sealing area of hot melt products $\geq 1/2$ edge sealing area; 2、 Bubble $a+b/2 \geq 1/2$ effective width, $N \leq 3$ , spacing $\geq 5\text{mm}$ , allowed No exposure of wiring, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/MIN
EC defect	Adhesive effect		1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2.No adhesive at panel edge $\leq$ 1mm, no exposure of wiring, allowed 3.No adhesive at edge and corner 1*1mm, no exposure of wiring, allowed 4. Adhesive height exceeds the display surface, not allowed	Visual, caliper	MIN
Silver dot adhesive defect	Silver dot adhesive		1、 Single silver dot dispensing amount $\geq$ 1mm, allowed 2、 One of the double silver dot dispensing amount is $\geq$ 1mm and the other has adhesive (no reference to 1mm) Allowed	Visual	MIN
			Silver dot dispensing residue on the panel $\leq$ 0.2mm, allowed	Film gauge	MIN
FPC defect	FPC wiring		FPC, TCP damage / gold finger peroxidation, adhesive residue, not allowed	Visual	MIJ
	FPC golden finger		The height of burr edge of TCP punching surface $\geq$ 0.4mm, not allowed	Caliper	MIN
	FPC damage/crase		Damage and breaking, not allowed Crease does not affect the electrical performance display, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/MIN
Protective film defect	Protective film	Scratch and crease on the surface but no affect to protection function, allowed		Check by eyes	MIN
		Adhesive at edge L $\leq$ 5mm, W $\leq$ 0.5mm, N=2, no entering into viewing area		Check by eyes	MIN
Stain defect	Stain	If stain can be normally wiped clean by > 99% alcohol, allowed		Visual	MIN
Pull tab defect	Pull tab	The position and direction meet the document requirements, and ensure that the protective film can be pulled off.		Check by eyes/ Manual pulling	MIN
Shading tape defect	Shading tape	Tilt $\leq$ 10°, flat without warping, completely covering the IC.		Check by eyes/ Film gauge	MIN
Stiffener	Stiffener	Flat without warping, Exceeding the left and right edges of the FPC is not allowed. Left and right can be less than 0.5mm from FPC edge		Check by eyes	MIN
Label	Label/ Spraying code	The content meets the requirements of the work sheet. The attaching position meets the requirements of the technical documents.		Check by eyes	MIN

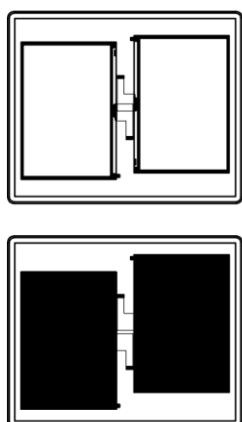
**Remarks:** The definition of other appearance B spec products, no affect to the display, and no entering into the viewing area.

## 15. Packaging

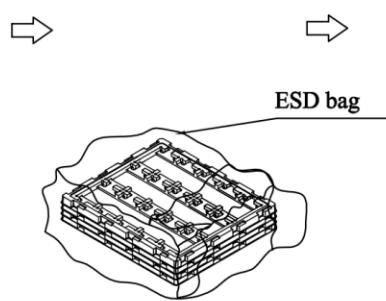
<i>CUSTOMER'S APPROVED:</i>		<i>PAGE: 1/1</i>
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### PACKLING ORDER:

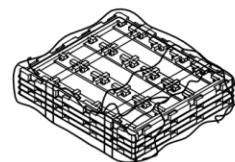
- 1) Putting 2 pcs Modules on each PET tray. And cover a dedicated EPE film.



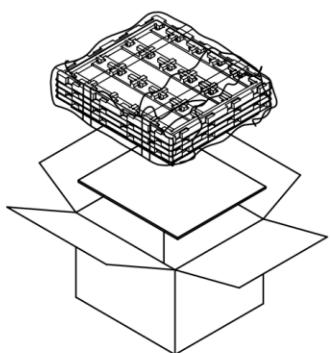
- 2) Putting 18 pcs PET trays together with 1 empty tray on the top of PET tray. Insert in the ESD bag, add desiccant in the ESD bag.



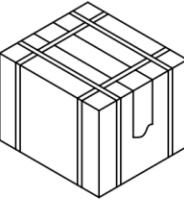
- 3) the tray together with adhesive tape



- 4) Putting into one outcarton



- 5) Packing finished



Note: 2 pcs in a tray, 18 trays in a out carton, so  $2 \times (19-1) = 36$  pcs/Outcarton

Dimension (Out carton): 454\*374\*190mm

Ver. 1	Drw:	Chk:	Apv: