Insert your paper title here

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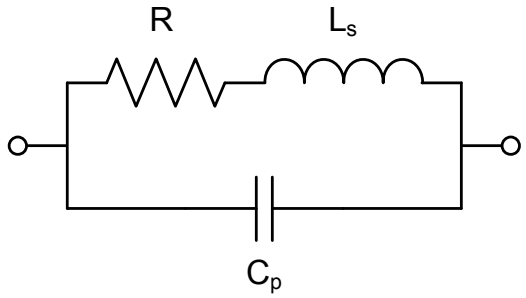

Fig. 1. Lumped circuit model of a non-ideal resistor.

***Abstract*—Abstract goes here.**

I. Introduction

An introduction with some references to [1] and [2].

II. Proposed isolated ADC

III. Coreless PCB transformers

IV. Topology and operating principles

V. Images

Images can be inserted as shown below. We can reference figure 1 like so. Use a starred figure environment for double column floats (see fig. 2).

VI. Math

We can include equations like so.

$$\frac{V(s)}{I(s)} = R + sL_s = R\left(1 + s\frac{L_s}{R}\right) \tag{1}$$

We can also reference equation 1.

A. Unnecessary subsection

This subsection is unnecessary, but serves as an example.

B. Unnecessary subsection

Like section VI-A, this subsection is unnecessary, but *also* serves as an example.

VII. Conclusion

Conclusion goes here.

Acknowledgements

Probably no acknowledgements required. If the HPC is used the line below should be included.

Computational (and/or data visualisation) resources and services used in this work were provided by the HPC and Research Support Group, Queensland University of Technology, Brisbane, Australia.

References

[1] M. A. H. Broadmeadow, G. F. Ledwich, and G. R. Walker, "An improved gate driver for power MOSFETs using a cascode configuration," in *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on*, April 2014, pp. 1–6.

[2] M. A. H. Broadmeadow, G. R. Walker, and G. F. Ledwich, "Comparison of the gate drive parameter space for driving power MOSFETs using conventional and cascode configurations," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, Sept 2014 (in press).

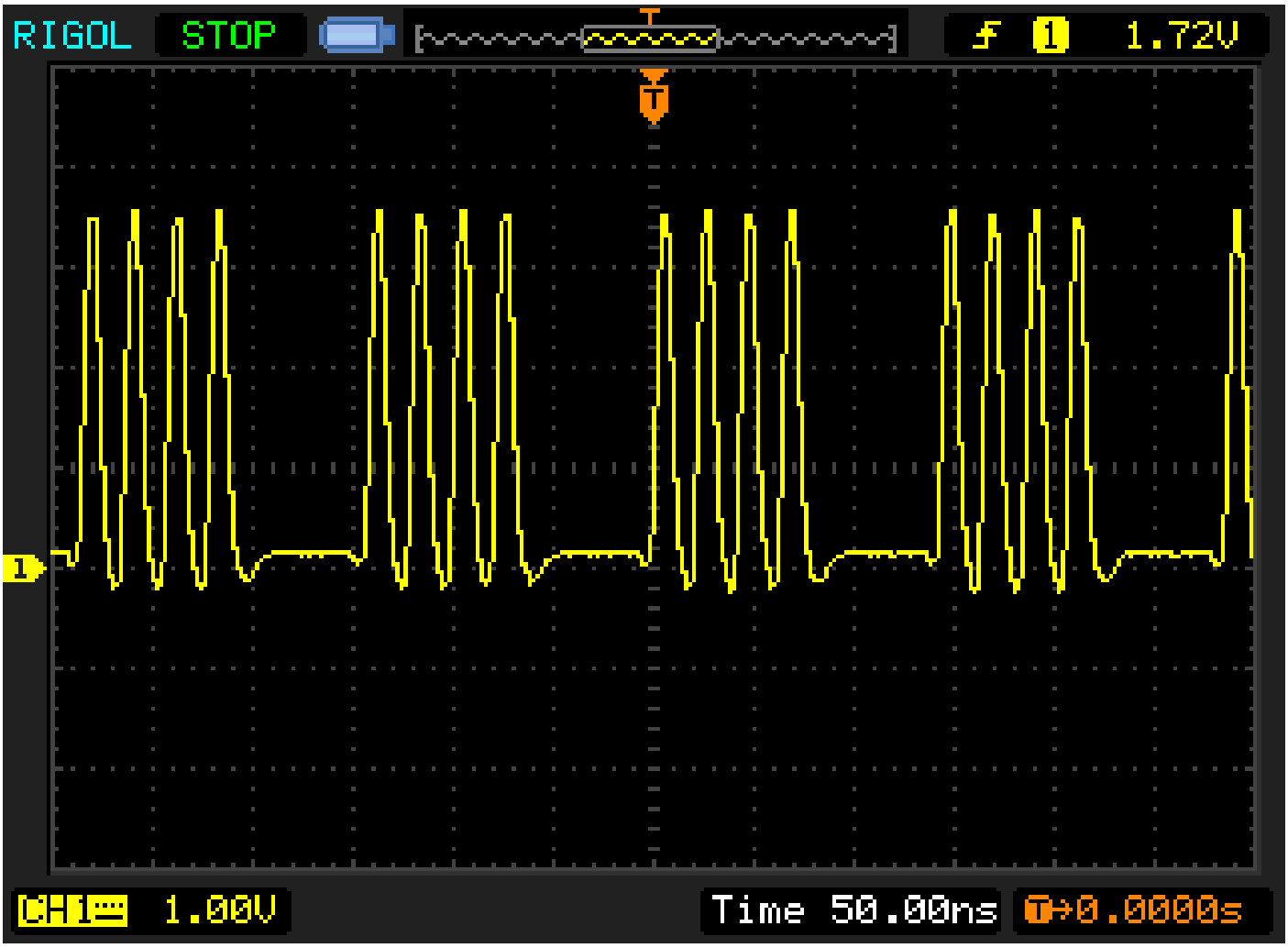

Fig. 2. An example scope capture.