A modular ADC system for power data acquisition utilising coreless PCB transformers for power and signal isolation

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***Abstract*—Energy monitoring and power quality analysis has, and always will be, a necessity in industrial and commercial situations....**

I. Introduction

Currently, industrial energy users are limited to the use of generally expensive and low-bandwidth energy usage data collection devices. Although such metering devices are well suited to high-accuracy, high-energy systems, they are poorly suited to highly modular, multi-sensor data collection schemes. To facilitate industrial process refinement, fault detection and energy usage analysis, the Queensland University of Technology researchers are currently developing a galvanically isolated, low-cost, high-bandwidth data acquisition module.

II. Proposed modular data acquisition system

The complete system (Fig.1) comprises of one or more data acquisition modules (herein referred to as DAQMs), a data consolidation FPGA, and a microcontroller attached to a PC, display or storage device. The DAQM's data conversion device is commercial dual-input sigma-delta IC, with appropriate signal conditioning to facilitate voltage measurement via a resistor divider, and current measurement via a resistive shunt or current transformer (CT). This paper will refer to the data conversion side of the DAQM as the "secondary" side. To power the sigma-delta converter and to transmit data from it to the host, as well as simultaneously providing the converter with a clock signal from the host, a single planar coreless PCB transformer is used. For current sigma-delta converter, the clock is approximately 8MHz, with the data rate of $f_{clock}/4$ (voltage and current share one data stream) with the maximum input sampling rate of $f_{clock}/12$. This transformer, along with the methods used to transfer power, clock and data signals, will be the focus of this paper. The secondary side of the DAQM consists of the coreless transformer driver, clock encoding and data recovery circuitry.

Planar coreless PCB transformers are not a new concept, and considerable work has been presented by Hui, et al [1]. Such papers are primarily focussed on the application of coreless PCB transformers in relatively low-frequency isolated gate drive circuits, and do not discuss high-frequency signal transfer nor bidirectional (clock and data) signal transfer whilst simultaneously extracting power from the PCB transformer's secondary planar winding.

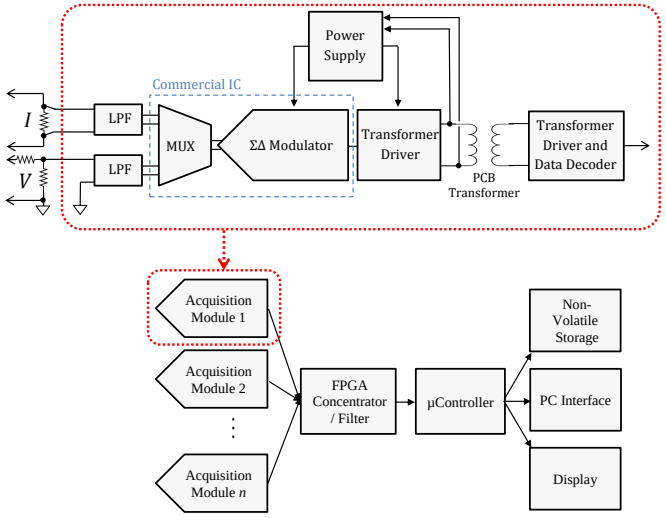

Fig. 1. Modular isolated power measurement system.

III. Planar coreless PCB transformers

The fundamental design of a planar coreless PCB transformer involves two planar copper spirals - one etched onto either side of a regular two-layer PCB. The two windings are thus separated by the PCB's core material, whose material properties and thickness determine, to some extent, the transformer's performance and primary-to-secondary isolation. This transformer's primary winding is then driven at high frequency, usually in the range of 2MHz to 20MHz in order to achieve either the maximum [input] impedance frequency (MIF - useful in low power systems) or the maximum efficiency frequency (MEF - useful for high power systems). Hui, et al [1] have demonstrated that an external secondary load capacitor, in the order of 100pF to 1nF, plays a significant role in the determination of the transformer's resonant frequency. In conventional coreless PCB transformer applications, the output (ie: secondary winding) voltage is then rectified and filtered. Transformer efficiencies exceeding 90%, with power density of up to $24W/cm^2$ have been demonstrated [1].

Planar coreless PCB transformers are very low cost and feature high power densities, no manufacturing restrictions due to core size or shape and are constructed using highly

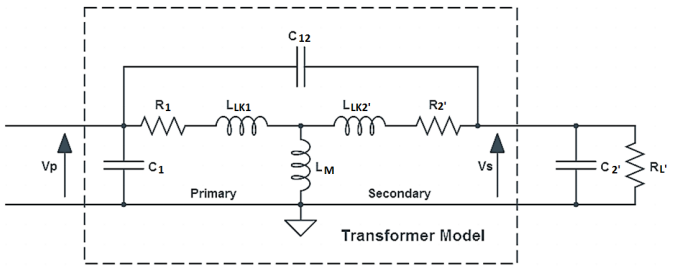

Fig. 2. High-frequency transformer model [1].

repeatable standard PCB manufacturing process.

A two-winding coreless PCB transformer may be described using the high-frequency transformer model in figure 2 [1], where:

R_1 Primary winding resistance;
R_2' Secondary winding resistance, referred to primary;
R_L' Load resistance, referred to primary;
L_{LK1} Primary leakage inductance;
L_{LK2}' Secondary leakage inductance, referred to primary;
L_M Mutual inductance;
C_{12} Primary-to-secondary winding capacitance;
C_1 Sum of primary winding capacitance and primary driver output capacitance;
C_2' Sum of secondary winding capacitance and external load capacitance, referred to primary;
n Turns ratio;

The self inductance of the planar winding is given by

$$L_p = \sum_{j=1}^{N_p} \sum_{i=1}^{N_p} M_{ij} \tag{1}$$

$$L_s = \sum_{j=1}^{N_s} \sum_{i=1}^{N_s} M_{ij} \tag{2}$$

And thus, the mutual inductance between the two planar windings may be represented as

$$M_{ps} = \sum_{j=1}^{N_p} \sum_{i=1}^{N_s} M_{ij} \tag{3}$$

where the mutual inductance, M_{ij}, has been reported in [2]

$$M_{ij} = \frac{\mu_0 \pi}{h_1 \ln(\frac{r_2}{r_1}) h_2 \ln(\frac{a_2}{a_1})} \int_0^\infty S(kr_2, kr_1) S(ka_2, ka_1) Q(kh_1, kh_2) e^{-k|z|} dk \tag{4}$$

where

$$S(kr_2, kr_1) = \frac{J_0(kr_2) - J_0(kr_1)}{k} \tag{5}$$

$$S(ka_2, ka_1) = \frac{J_0(ka_2) - J_0(ka_1)}{k} \tag{6}$$

IV. Implementation of power and signal isolation using PCB transformers

A. Power

The most basic use for a planar coreless PCB transformer is in an isolated power transfer application. Typically, this would be achieved by driving the transformer at its maximum efficiency frequency (MEF) for high power transfer applications, or, where it is desirable to minimise the quiescent power consumption of the transformer, the maximum impedance frequency (MIF). The MEF will tend to approach the MIF as the transformer's secondary load current decreases [1]. Due to the low secondary load current of the DAQM, approximately 6mA at 3.3V (20mW), the MEF of the module's coreless PCB transformer is assumed to be equal to the MIF. In most papers discussing planar coreless PCB transformers, the primary winding is driven in either a single-ended or bipolar manner [FIGURE] with a relatively high supply voltage (12V being a popular choice for isolated gate drive circuits). Since the DAQM is to be a 3.3V supply capable device, the PCB transformer is driven in a bipolar manner to achieve an effective doubling of the primary drive voltage. The primary drive circuit uses a simple relaxation oscillator for the resonant frequency generation, and the transformer's winding is driven directly by the Schmitt-trigger's high-current ($\pm$32mA) push-pull outputs [FIGURE]. On the transformer's secondary side, the output waveform may simply be rectified using an ordinary voltage-doubler rectifier topology [FIGURE]. The figure shows the use of Schottky diodes to minimise voltage loss, however, the effect of the diode's junction capacitance on the transformer's resonant frequency should not be neglected.

B. Clock Generation and Recovery

In order to provide a clock signal of approximately 8MHz to the frontend ADC, a method of transferring this clock signal via the PCB transformer from the DAQM's primary side to the secondary side (where the sigma-delta data converter resides) was required. It is desirable to allow the sigma-delta modulator to be externally clocked as this allows for synchronisation in multi-module systems, thus simplifying the filtering and data consolidation process. Since a coreless PCB transformer's resonant frequency may be adjusted quickly and easily using the external load capacitance, it is possible to drive the transformer at any power-of-two multiple of the desired modulator clock frequency (provided the resulting drive frequency results in sufficient secondary output voltage). The clock signal may then extracted simply by rectifying, filtering and dividing the transformer's secondary voltage waveform. The resulting clock recovery circuit has been highlighted in FIGURE.

C. Data Recovery

The sigma-delta data converter encodes both voltage and current information into a single Manchester-encoded bit-stream at a rate equal to $f_{clock}/4$ (typically 2MHz). To transfer this data back to the primary side of the data acquisition module, a second coreless PCB transformer may be used. Since the data signal is not periodic in the way that a clock signal may be, it is necessary to configure the data transformer for a very high resonant frequency. This ensures that only the high-frequency square wave transitions are sent over the coil.

As the data frequency approaches the transformer's resonant frequency, the transformer's output voltage can be seen to 'ring' after the fundamental edge transition is transmitted - a benefit when maximum power transfer is required, but detrimental to the signal integrity of data transmissions. To achieve a very high resonant frequency, the EQUATIONS imply that either the number of primary and secondary turns (and thus the primary and secondary outer diameter) should be decreased, and/or the external load capacitor may be reduced or removed. FIGURE shows the signal transformer and data recovery circuit. On the signal transformer's secondary side (where the sigma-delta modulator is located), the data output of the modulator is capacitively coupled into the signal transformer, which is driven in a single-ended configuration. On the primary side, the low-amplitude (50mV to 500mV may be expected) positive- and negative-going spikes, which represent the rising and falling edges of the data signal respectively, are first amplified by a bipolar junction transistor (BJT). The amplifier's output is then coupled into two more BJTs with necessary biasing to allow the discrimination of the positive- and negative-going transitions. The output of each of the 'edge transition detectors' is then fed into a set/reset latch constructed from a dual Schmitt-input NAND array. As an added benefit, the outputs of the two NAND gates are complementary and thus allow for differential signal driving back to the host FPGA (which may be located some distance away).

V. Experimental Validation

To validate the use of planar coreless PCB transformers in the data acquisition module design, a test PCB transformer was manufactured on a standard two-layer, 1.6mm PCB. The test transformer had 11 turns with identical primary and secondary windings. The track and spacing width was equal at 203.2μm (8 mil), giving an outer diameter of 13.7mm.

A. Power

To approximate the expected load of the sigma-delta modulator and associated secondary circuitry, a 500Ω load resistor was fitted after the rectifier. By sweeping the primary drive frequency over the range of 500kHz to 25MHz, the coreless PCB test transformer, with primary-side Schmitt trigger driver and secondary side rectifier could be analysed for input impedance- and output voltage- versus frequency (FIGURE). The figure shows a clear distinction between the MIF (13MHz) and MEF (15.5MHz), however the reasonably low quality factor of the MEF peak suggests that driving the transformer at a frequency of compromise between the MIF and MEF may be desirable. The data also demonstrate the effectiveness of driving the transformer in a bipolar manner, which has resulted in an output voltage approximately 1.6 times the 3.3V primary supply voltage - thus increasing the usable voltage range of the data acquisition module and simplifying the secondary voltage supply circuitry. FIGURE shows the coreless PCB test transformer's secondary rectified output power and voltage versus load current. It shows a maximum power point of 47mW, and that for a minimum pre-regulator voltage of 3.5V, the load current may be up to 11mA (about 40mW) - twice the expected power required by the DAQM's secondary circuitry. As a compromise between the MIF (13MHz) and MEF (15.5MHz), the test transformer drive frequency was

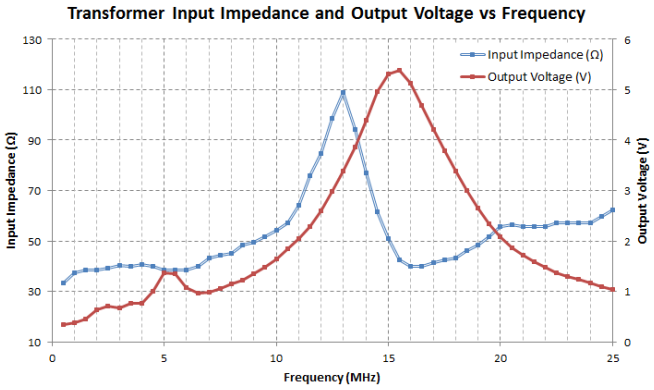

Fig. 3. Input impedance and output voltage versus frequency at 3.3V.

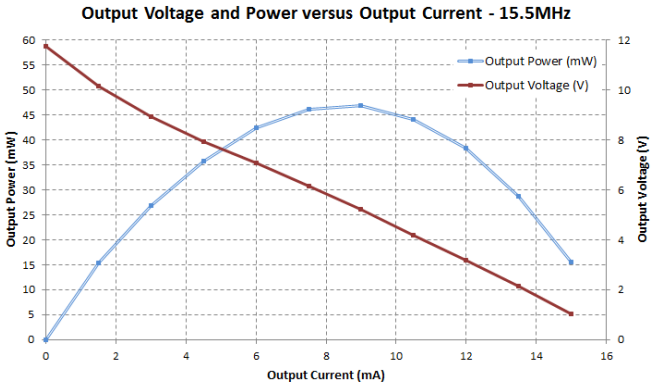

Fig. 4. Secondary output voltage and power versus load current at MEF (15.5MHz).

adjusted to 14MHz (see FIGURE). This data shows improved load regulation and a shift in the maximum power point toward greater load currents, as well as a slight reduction in maximum power (approximately 47mW max versus 40mW max). This suggests that transformer operation at a MEF-MIF compromise frequency (rather than at the MEF exactly) can have benefits for applications with greater secondary loads where the primary is driven by a current-limited source (such as the Schmitt trigger direct-drive circuit used herein). The recommended experimental frequency setting procedure is to configure the secondary circuit for maximum expected load, then adjust the primary driver frequency for maximum secondary output voltage.

B. Clock Generation and Recovery

Since the sigma-delta modulator's clock is derived from the drive frequency of the primary winding, it is necessary for the primary drive frequency to be an exact power-of-two multiple of the desired modulator frequency, which may vary from DC to 8MHz. For the DAQM application, however, the external clock is necessary for multi-module synchronisation, and there is no desire to operate the sigma-delta modulator at a clock frequency other than 8MHz. The test coreless PCB transformer has been designed for a 16MHz resonant frequency, with prior figures showing this to be the case in practice. FIGURE shows the 16MHz clock signal (Reference - white), secondary

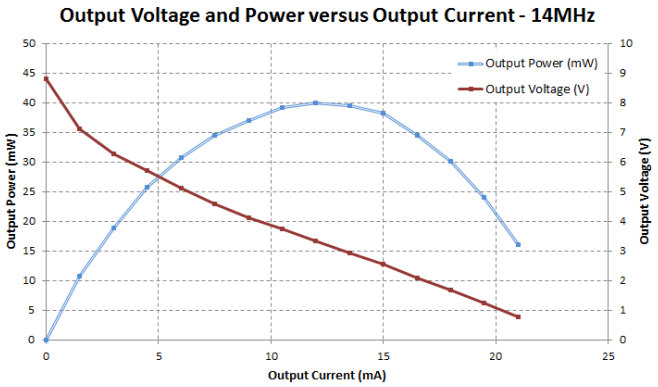

Fig. 5. Secondary output voltage and power versus load current at MIF-MEF compromise (14MHz).

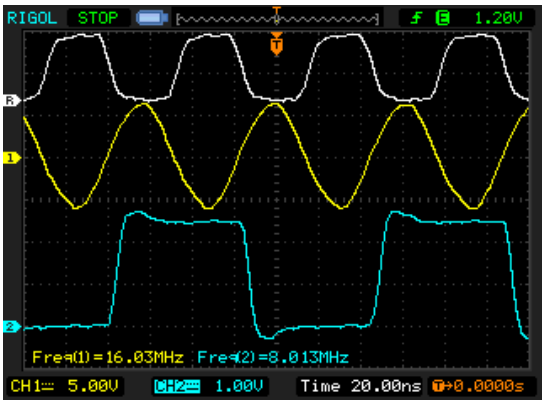

Fig. 6. 16MHz input clock signal (top); secondary output voltage (centre); 8MHz extracted clock signal (bottom).

output voltage (Channel 1 - yellow) and extracted clock signal (Channel 2 - cyan). The divide-by-two clock extraction method appears effective, even with a varying secondary load, and further testing showed the simple circuit was able to accurately output a clock signal over the transformer drive frequency range of 11MHz to 16MHz. The figures show no reason why a higher order division (divide by 4, for example) could not be used if desired.

C. Data Recovery

To test the data recovery circuit, a second PCB transformer was obtained with physical specifications identical to the unit discussed prior. This second test transformer, however, had its load capacitor (which was 100pF in the prior unit) removed, such that its resonant frequency (now estimated to be $>$80MHz) was much greater than the expected data frequency - a key requirement of the data detection circuit. Driving the transformer in a single-ended configuration was achieved by grounding one terminal and connecting the other, via a small capacitor, to a signal generator simulating the sigma-delta modulator's data output. Due to hardware availability issues, the high-speed ($t_d \leq 10ns$) Schmitt NAND gate specified in the circuit was substituted for an ordinary-speed ($t_d \approx 250ns$) Schmitt NAND gate, which resulted in poor performance above about 500kHz (due to the fast impulses generated by the edge detection circuit). FIGURE shows the data recovery

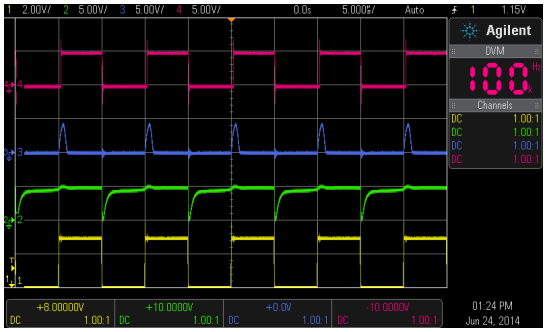

Fig. 7. Data into transformer (CH1, bottom); output of negative edge amplifier (CH2); output of positive edge amplifier (CH3); recovered data signal at output of transformer (CH4, top).

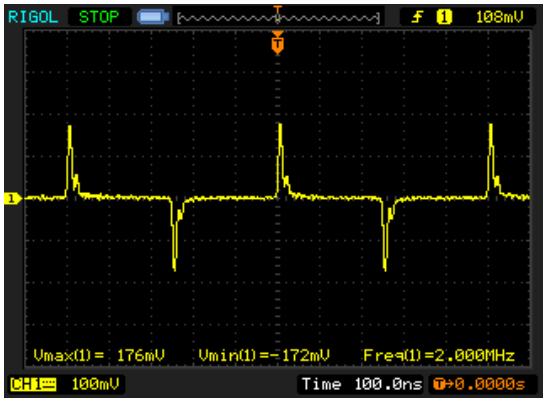

Fig. 8. Positive and negative edge spikes at secondary of 5-turn transformer (3.3V primary signal).

circuit operating at 100kHz, where Channel 1 (bottom) is the 2MHz simulated data into the transformer; Channel 2 is the output of the negative edge amplifier (node 'Neg Edge' in FIGURE); Channel 3 is the output of the positive edge amplifier (node 'Pos Edge' in FIGURE); and Channel 4 (top) is the recovered 2MHz data signal. Since the data recovery circuit was capable of reliable operation with edge spikes of an amplitude as low as about 100mV, the 11-turn transformer was found to be excessive for the data signal transfer. By cutting the PCB copper tracks on the primary and secondary side of the transformer, the performance of the data recovery circuit was tested for a transformer consisting of five turns and three turns. The test showed that for a 3.3V square wave input, the five-turn and three-turn transformer yielded edge spikes of amplitude approximately 170mV and 50mV respectively. FIGURE shows the positive and negative edge spikes at the secondary of the five-turn coreless PCB transformer with a 3.3V, 2MHz primary signal applied (via a small capacitor). Testing has demonstrated that the data recovery circuit is effective over a range of data rates and duty cycles, and that a coreless PCB transformer with as few as four to five turns can be expected to yield reliable performance.

VI. Future Work

VII. Conclusion

Conclusion goes here.

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[3] ——, "An improved gate driver for power MOSFETs using a cascode configuration," pp. 1–6, April 2014.