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**Abstract**—Energy monitoring and power quality analysis has, and always will be, a necessity in industrial and commercial situations....

## I. INTRODUCTION

Currently, industrial energy users are limited to the use of generally expensive and low-bandwidth energy usage data collection devices. Although such metering devices are well suited to high-accuracy, high-energy systems, they are poorly suited to highly modular, multi-sensor data collection schemes. To facilitate industrial process refinement, fault detection and energy usage analysis, the Queensland University of Technology researchers are currently developing a galvanically isolated, low-cost, high-bandwidth data acquisition module.

The complete system (figure) comprises of one or more data acquisition modules (herein referred to as DAQMs), a data consolidation FPGA, and a microcontroller attached to a PC, display or storage device. The DAQM's data conversion device is commercial dual-input sigma-delta IC, with appropriate signal conditioning to facilitate voltage measurement via a resistor divider, and current measurement via a resistive shunt or current transformer (CT). This paper will refer to the data conversion side of the DAQM as the "secondary" side. To power the sigma-delta converter and to transmit data from it to the host, as well as simultaneously providing the converter with a clock signal from the host, a single planar coreless PCB transformer is used. For current sigma-delta converter, the clock is approximately 8MHz, with the data rate of  $f_{clock}/4$  (voltage and current share one data stream) with the maximum input sampling rate of  $f_{clock}/12$ . This transformer, along with the methods used to transfer power, clock and data signals, will be the focus of this paper. The secondary side of the DAQM consists of the coreless transformer driver, clock encoding and data recovery circuitry.

Planar coreless PCB transformers are not a new concept, and considerable work has been presented by Hui, et al [1]. Such papers are primarily focussed on the application of coreless PCB transformers in relatively low-frequency isolated gate drive circuits, and do not discuss high-frequency signal transfer nor bidirectional (clock and data) signal transfer whilst simultaneously extracting power from the PCB transformer's secondary planar winding.

## II. PLANAR CORELESS PCB TRANSFORMERS

The fundamental design of a planar coreless PCB transformer involves two planar copper spirals - one etched onto either side of a regular two-layer PCB. The two windings are thus separated by the PCB's core material, whose material

properties and thickness determine, to some extent, the transformer's performance and primary-to-secondary isolation. This transformer's primary winding is then driven at high frequency, usually in the range of 2MHz to 20MHz in order to achieve either the maximum [input] impedance frequency (MIF - useful in low power systems) or the maximum efficiency frequency (MEF - useful for high power systems). Hui, et al [ref] have demonstrated that an external secondary load capacitor, in the order of 100pF to 1nF, plays a significant role in the determination of the transformer's resonant frequency. In conventional coreless PCB transformer applications, the output (ie: secondary winding) voltage is then rectified and filtered. Transformer efficiencies exceeding 90%, with power density of up to  $24W/cm^2$  have been demonstrated [1].

Planar coreless PCB transformers are very low cost and feature high power densities, no manufacturing restrictions due to core size or shape and are constructed using highly repeatable standard PCB manufacturing process.

A two-winding coreless PCB transformer may be described using the high-frequency transformer model in FIGURE, where [LIST OF PARAMETERS]. The self inductance of the planar winding is given by

$$L_p = \sum_{j=1}^{N_p} \sum_{i=1}^{N_p} M_{ij} \quad (1)$$

$$L_s = \sum_{j=1}^{N_s} \sum_{i=1}^{N_s} M_{ij} \quad (2)$$

And thus, the mutual inductance between the two planar windings may be represented as

$$M_{ps} = \sum_{j=1}^{N_p} \sum_{i=1}^{N_s} M_{ij} \quad (3)$$

where the mutual inductance,  $M_{ij}$ , has been reported by Hurley and Duffy [2]

$$M_{ij} = \frac{\mu_0 \pi}{h_1 \ln(\frac{r_2}{r_1}) h_2 \ln(\frac{a_2}{a_1})} \int_0^\infty S(kr_2, kr_1) S(ka_2, ka_1) Q(kh_1, kh_2) \exp^{-k \mod z} \quad (4)$$

where

$$S(kr_2, kr_1) = \frac{J_0(kr_2) - J_0(kr_1)}{k} \quad (5)$$

$$S(ka_2, ka_1) = \frac{J_0(ka_2) - J_0(ka_1)}{k} \quad (6)$$

### III. TOPOLOGY

#### A. Power

The most basic use for a planar coreless PCB transformer is in an isolated power transfer application. Typically, this would be achieved by driving the transformer at its maximum efficiency frequency (MEF) for high power transfer applications, or, where it is desirable to minimise the quiescent power consumption of the transformer, the maximum impedance frequency (MIF). The MEF will tend to approach the MIF as the transformer's secondary load current decreases [1]. Due to the low secondary load current of the DAQM (approximately 20mW at 3.3V) the MEF of the module's coreless PCB transformer is assumed to be equal to the MIF. In most papers discussing planar coreless PCB transformers, the primary winding is driven in either a single-ended or bipolar manner [FIGURE] with a relatively high supply voltage (12V being a popular choice for isolated gate drive circuits). Since the DAQM is to be a 3.3V supply capable device, the PCB transformer is driven in a bipolar manner to achieve an effective doubling of the primary drive voltage. The primary drive circuit uses a simple relaxation oscillator for the resonant frequency generation, and the transformer's winding is driven directly by the schmitt-trigger's high-current ( $\pm 32\text{mA}$ ) push-pull outputs [FIGURE]. On the transformer's secondary side, the output waveform may simply be rectified using an ordinary voltage-doubler rectifier topology [FIGURE]. The figure shows the use of schottky diodes to minimise voltage loss, however, the effect of the diode's junction capacitance on the transformer's resonant frequency should not be neglected.

#### B. Clock Generation and Recovery

Due to the minimal secondary power required by the DAQM's frontend, the sigma-delta ADC's clock signal may be encoded simply by gating the transformer's primary drive current. [FIGURE] shows a standard silicon diode used to gate the relaxation oscillator such that an external clock signal of arbitrary timing may 100% amplitude-modulate the transformer's primary drive current. To recover the clock signal, the transformer's secondary output is essentially low-pass filtered with a cutoff frequency approximately equal to the [SOMETHING]. [FIGURE] shows the decoding circuit, using a Schmitt trigger inverter (with feedback) to bias the filtered signal and provide clean clock transitions for the data converter's clock input.

Images can be inserted as shown below. We can reference figure 1 like so. Use a starred figure environment for double column floats (see fig. 2).

### IV. MATH

We can include equations like so.

$$\frac{V(s)}{I(s)} = R + sL_s = R \left( 1 + s \frac{L_s}{R} \right) \quad (7)$$

We can also reference equation 7.

#### A. Unnecessary subsection

This subsection is unnecessary, but serves as an example.

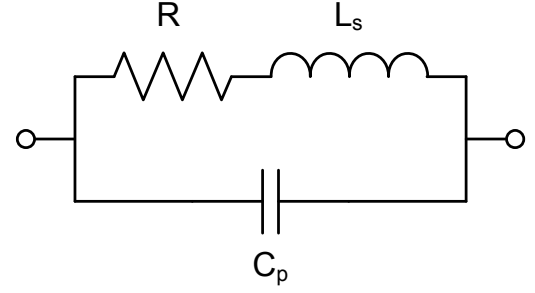


Fig. 1. Lumped circuit model of a non-ideal resistor.

#### B. Unnecessary subsection

Like section IV-A, this subsection is unnecessary, but *also* serves as an example.

### V. CONCLUSION

Conclusion goes here.

### ACKNOWLEDGEMENTS

Probably no acknowledgements required. If the HPC is used the line below should be included.

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### REFERENCES

- [1] J. Biela, D. Aggeler, D. Bortis, and J. W. Kolar, "5kV/200ns pulsed power switch based on a SiC-JFET super cascode," in *IEEE International Power Modulators and High Voltage Conference, Proceedings of the 2008*, 2008, pp. 358–361.
- [2] M. A. H. Broadmeadow, G. F. Ledwich, and G. R. Walker, "An improved gate driver for power MOSFETs using a cascode configuration," in *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on*, April 2014, pp. 1–6.

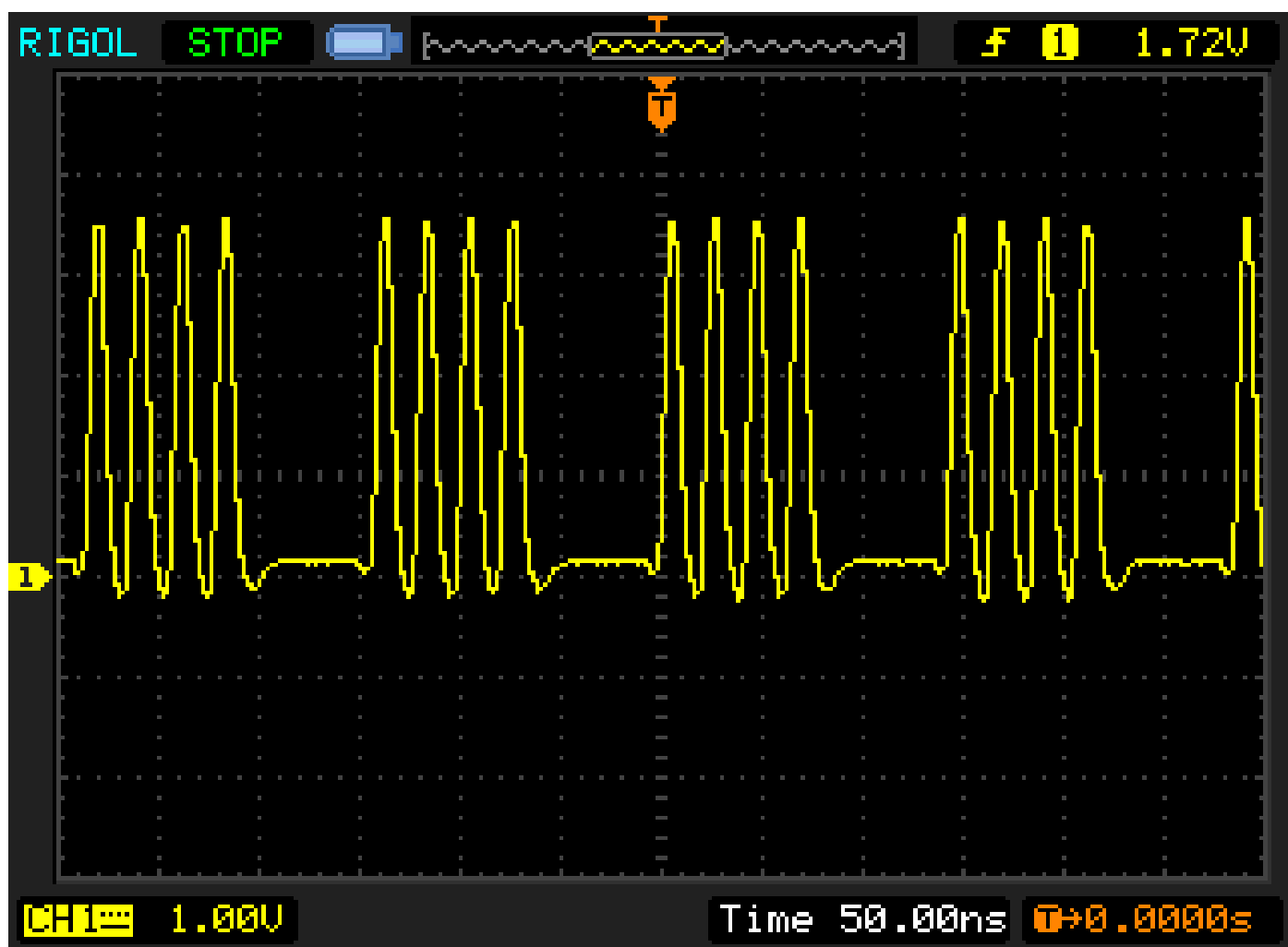


Fig. 2. An example scope capture.