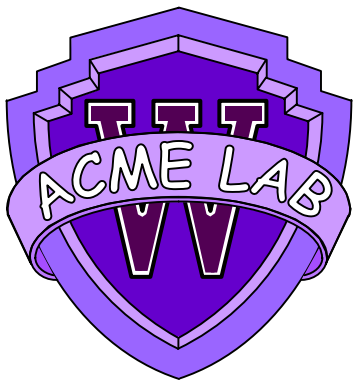
State of the Art Architectures Xilinx and Altera



Mark L. Chang

ACME Seminar

June 30, 2003

The Timeline

- 1998 – Xilinx Virtex
- 1999 – Xilinx Virtex-E
- 2000 – Xilinx Virtex-II
- June 2000
  - Altera Nios soft-core processor ships
  - Excalibur announced

The Timeline

- Sept. 2000
  - Excalibur architecture unveiled
- April 2001
  - Xilinx MicroBlaze soft-core processor ships
- October 2001
  - Excalibur ships

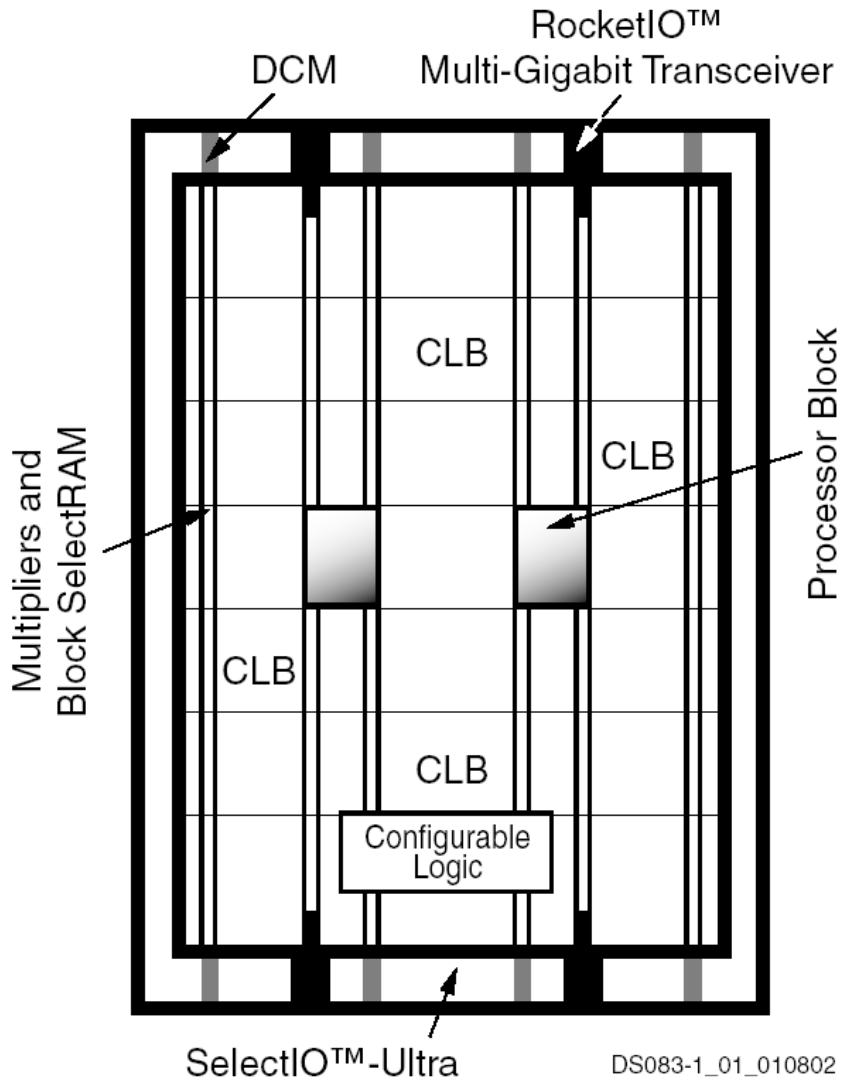
The Timeline

- February 2002
  - Altera Stratix announced
- March 2002
  - Xilinx Virtex-II Pro ships
- June 2002
  - Stratix ships

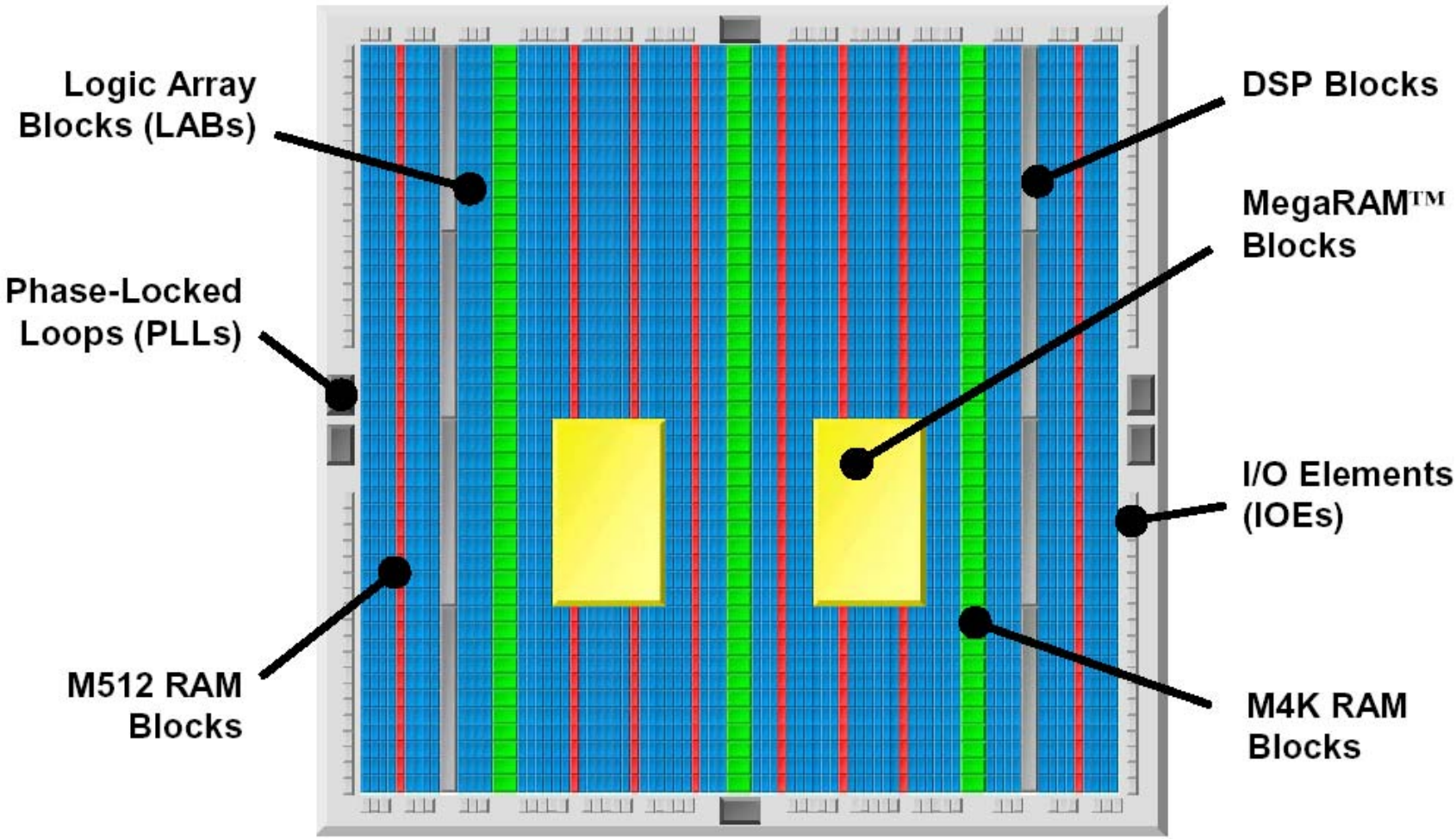
Head-to-Head

- Xilinx Virtex-II Pro
  - 1.5v 130nm copper
  - 125,136 logic cells
  - 10Mb RAM
  - 556 18x18 multipliers
  - Up to four PowerPC 405 cores
- Altera Stratix
  - 1.5v 130nm copper
  - 114,140 logic elements
  - 10Mb RAM
  - 224 9x9 multipliers
  - No hard processor cores (Excalibur, based on Apex 20k)

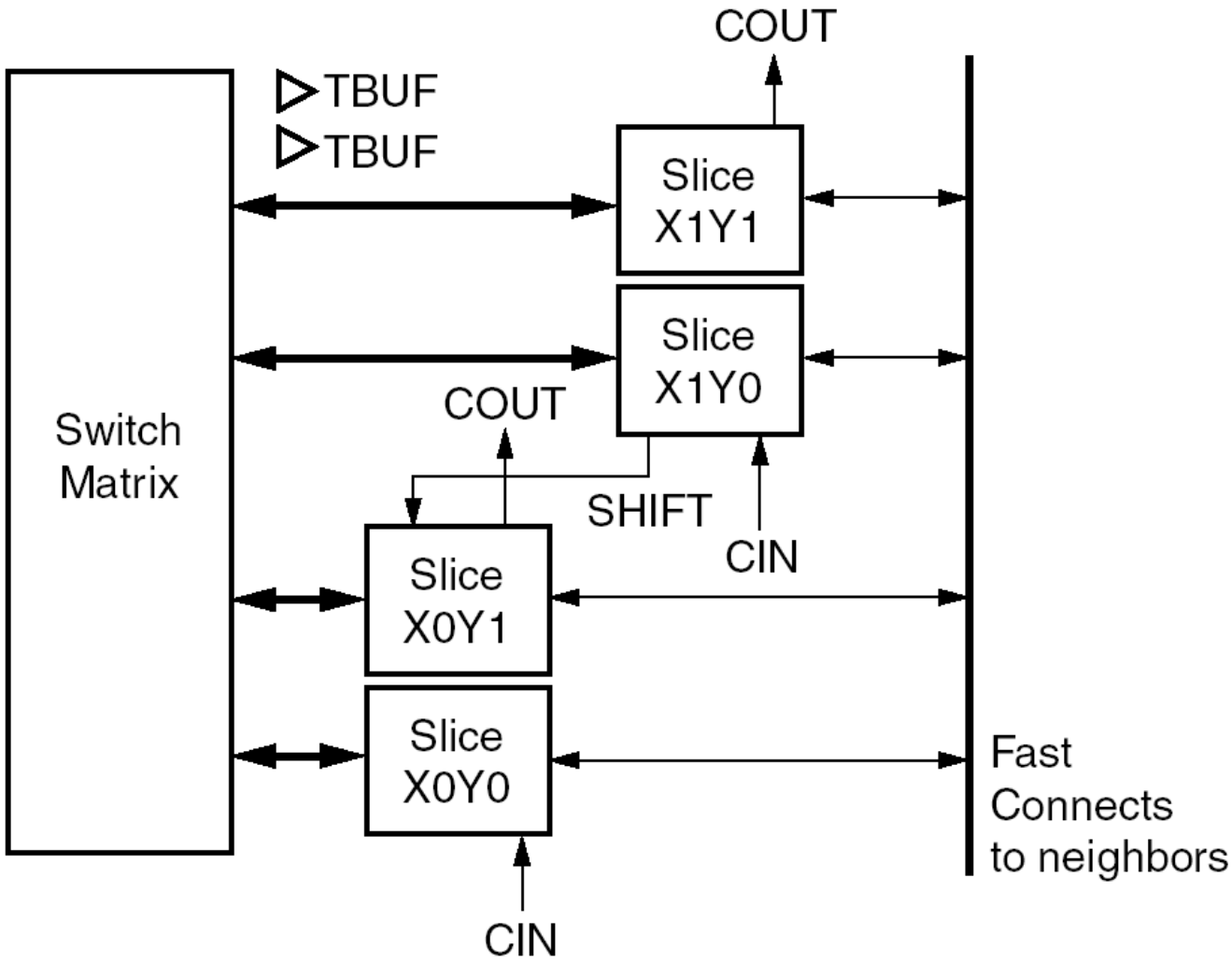
Xilinx Virtex-II Pro



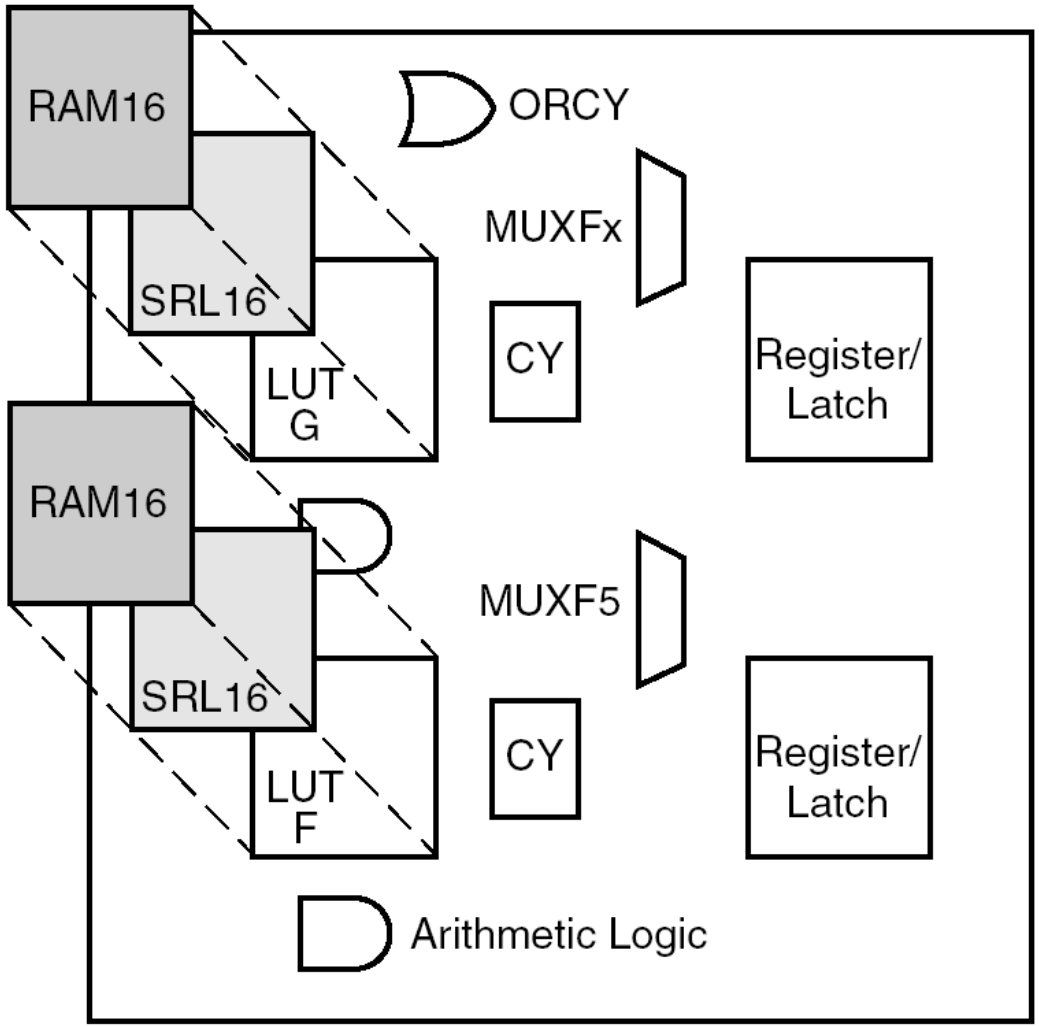
Altera Stratix



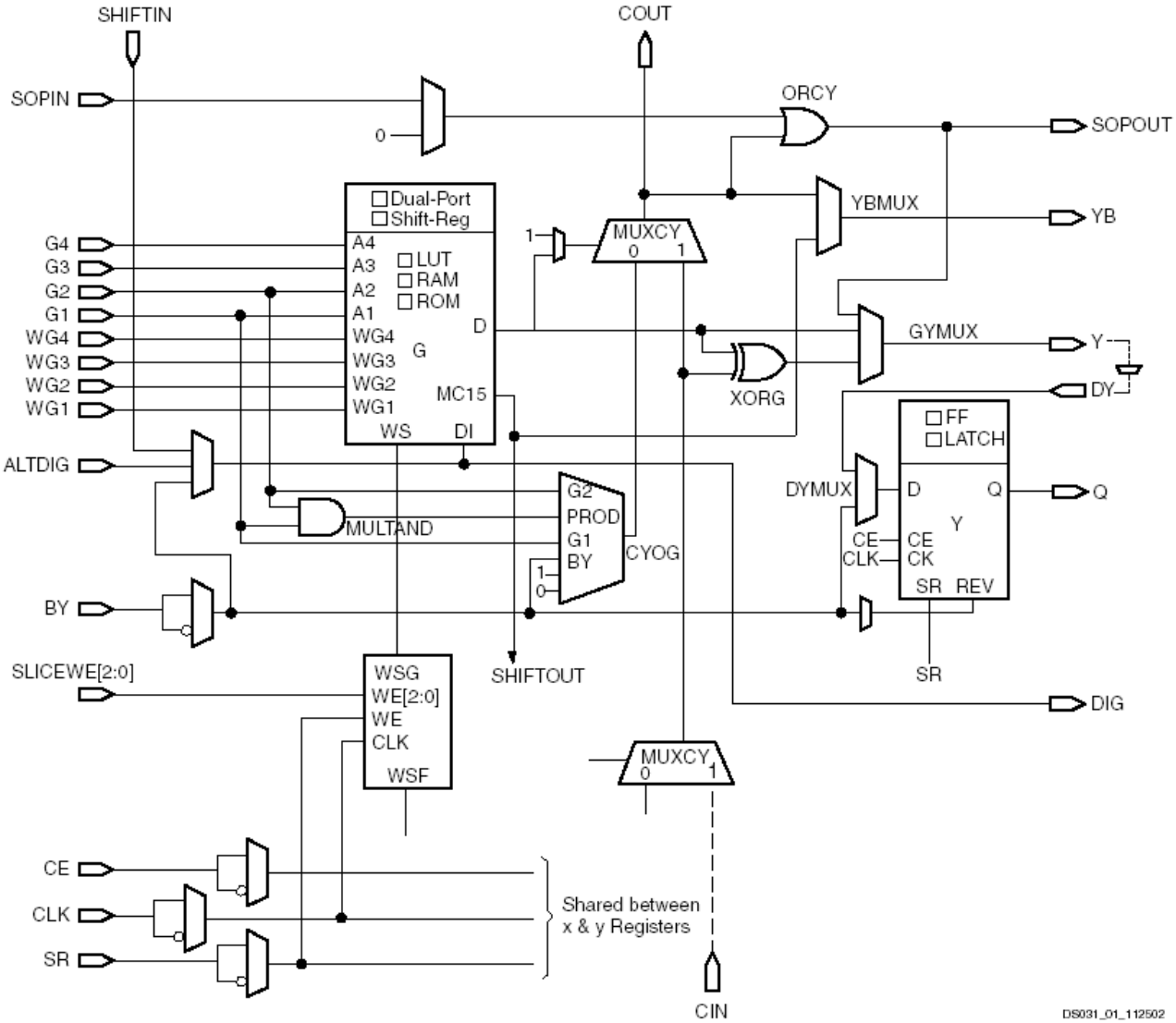
Xilinx Virtex CLB



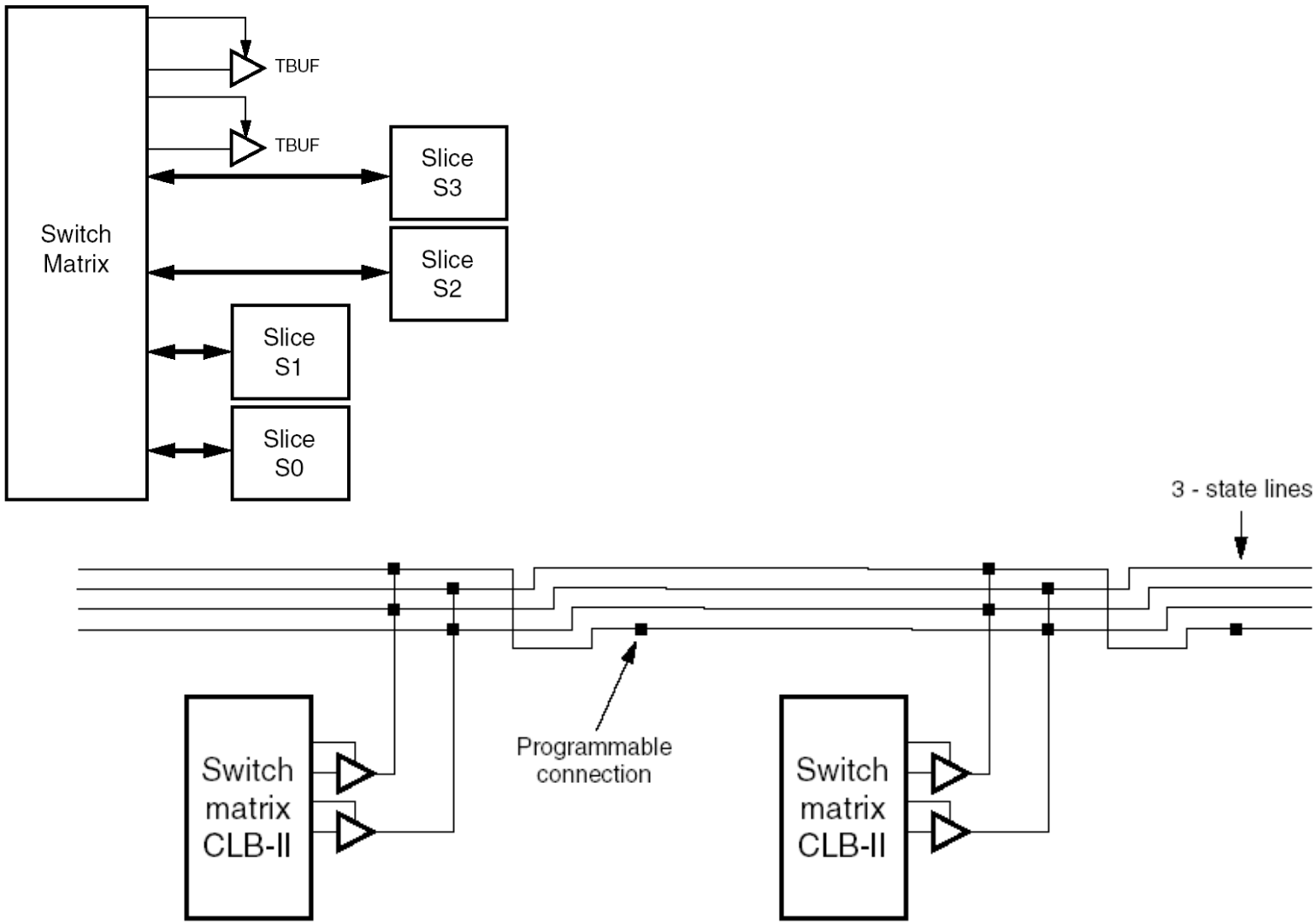
Virtex Slice



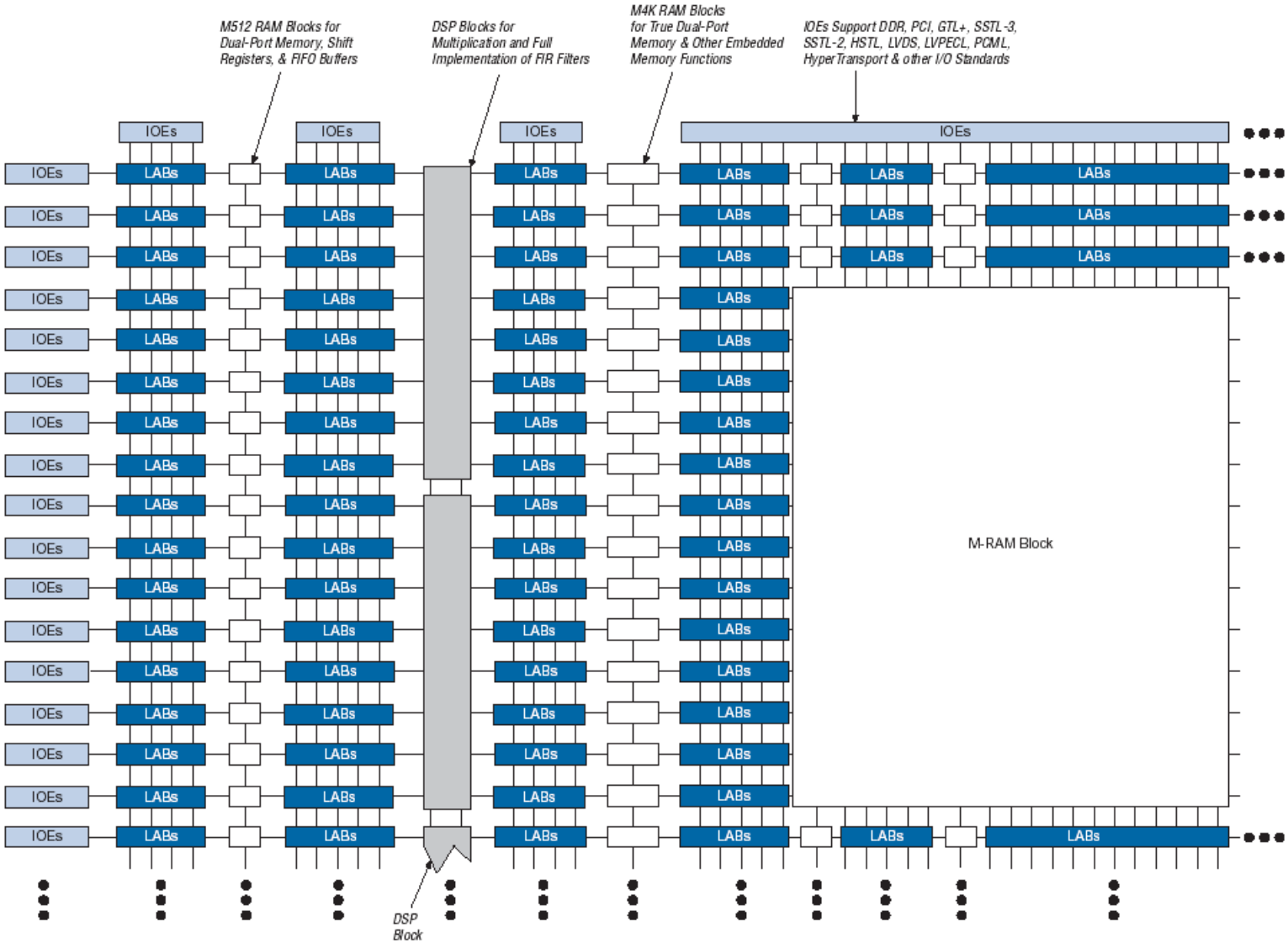
Half Slice


SHIFTIN
COUT
SOPIN
0
ORCY
SOPOUT
Dual-Port
Shift-Reg
LUT
RAM
ROM
G4
G3
G2
G1
WG4
WG3
WG2
WG1
A4
A3
A2
A1
G
D
MC15
WS
DI
1
MUXCY
0
1
YBMUX
YB
GYMUX
Y
DY
XORG
FF
LATCH
DYMUX
D
Q
Y
CE
CLK
CK
SR
REV
ALTDIG
MULTAND
G2
PROD
G1
BY
CYOG
1
0
BY
SLICEWE[2:0]
WSG
WE[2:0]
WE
CLK
WSF
SHIFTOUT
SR
DIG
MUXCY
0
1
CE
CLK
SR
Shared between
x & y Registers
CIN
DS031_01_112502

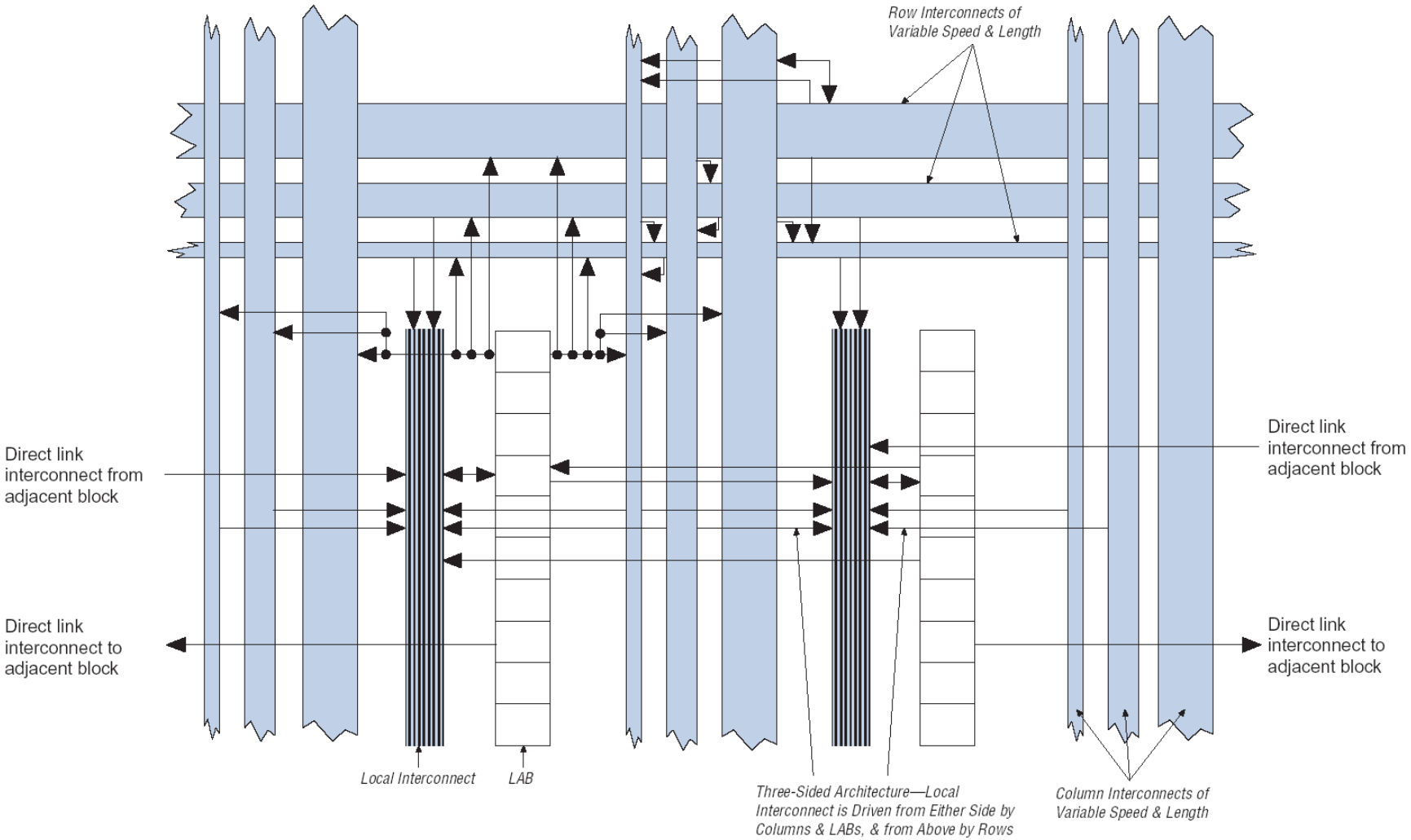
3-State Buffers



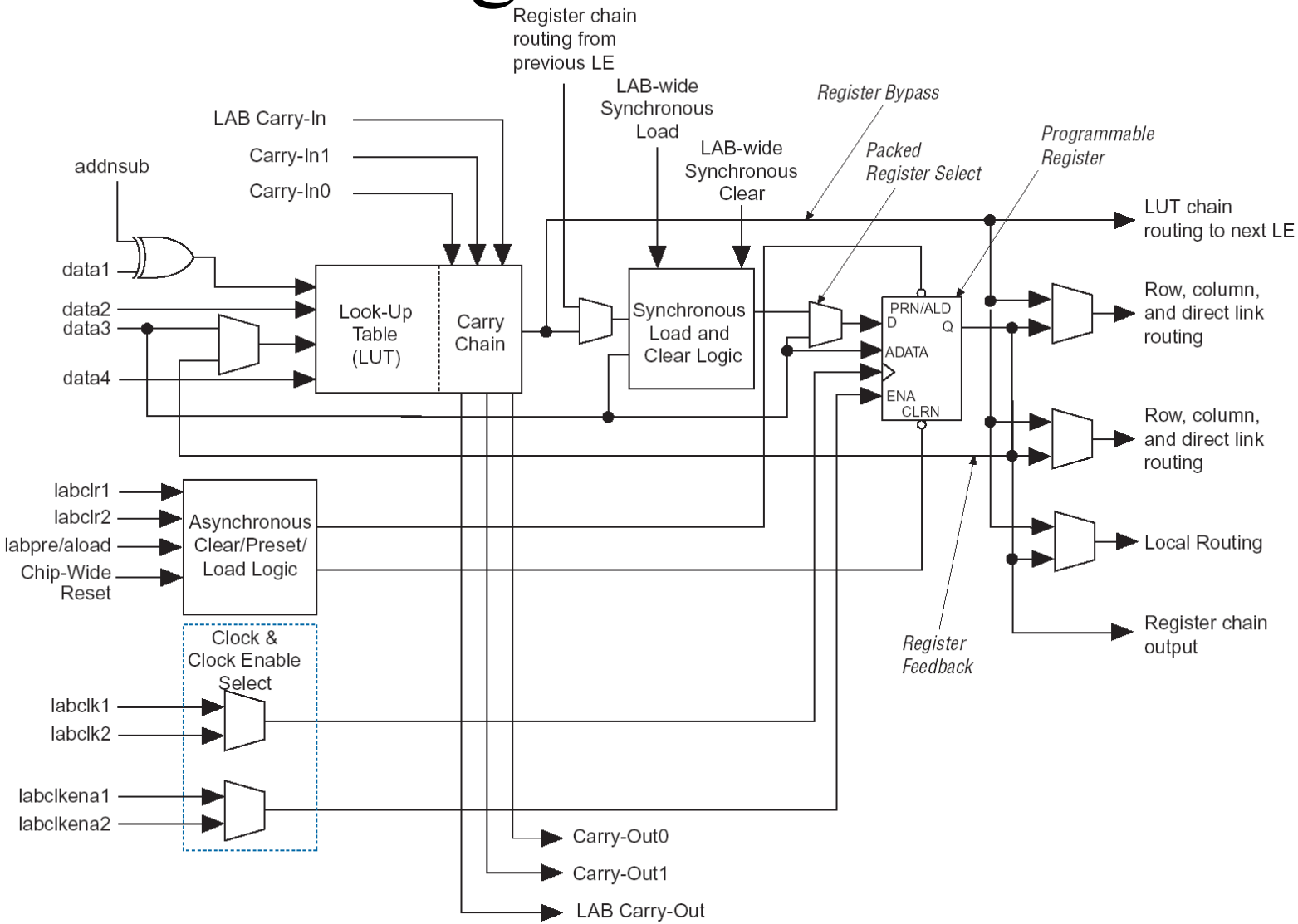
Altera Stratix



Logic Array Blocks (LABs)

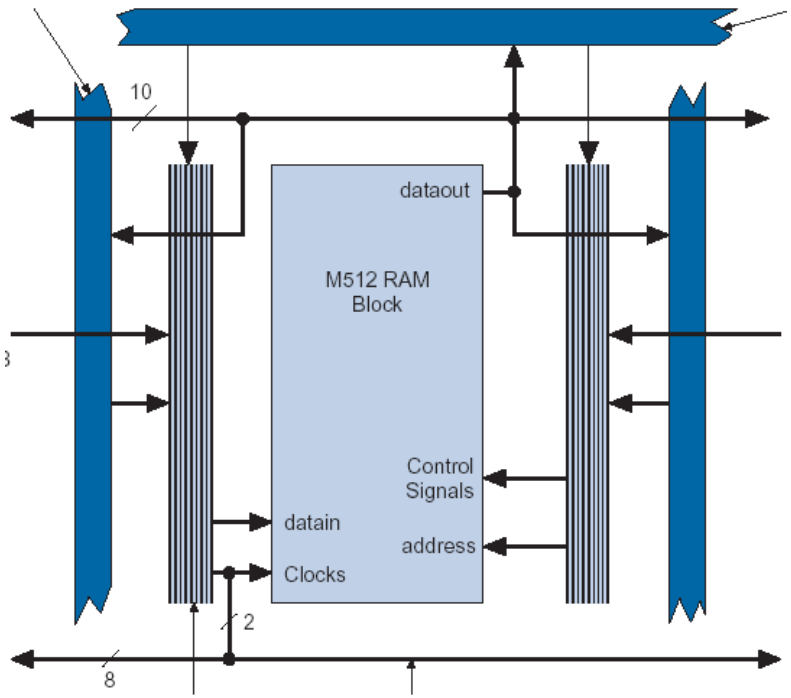


Logic Element

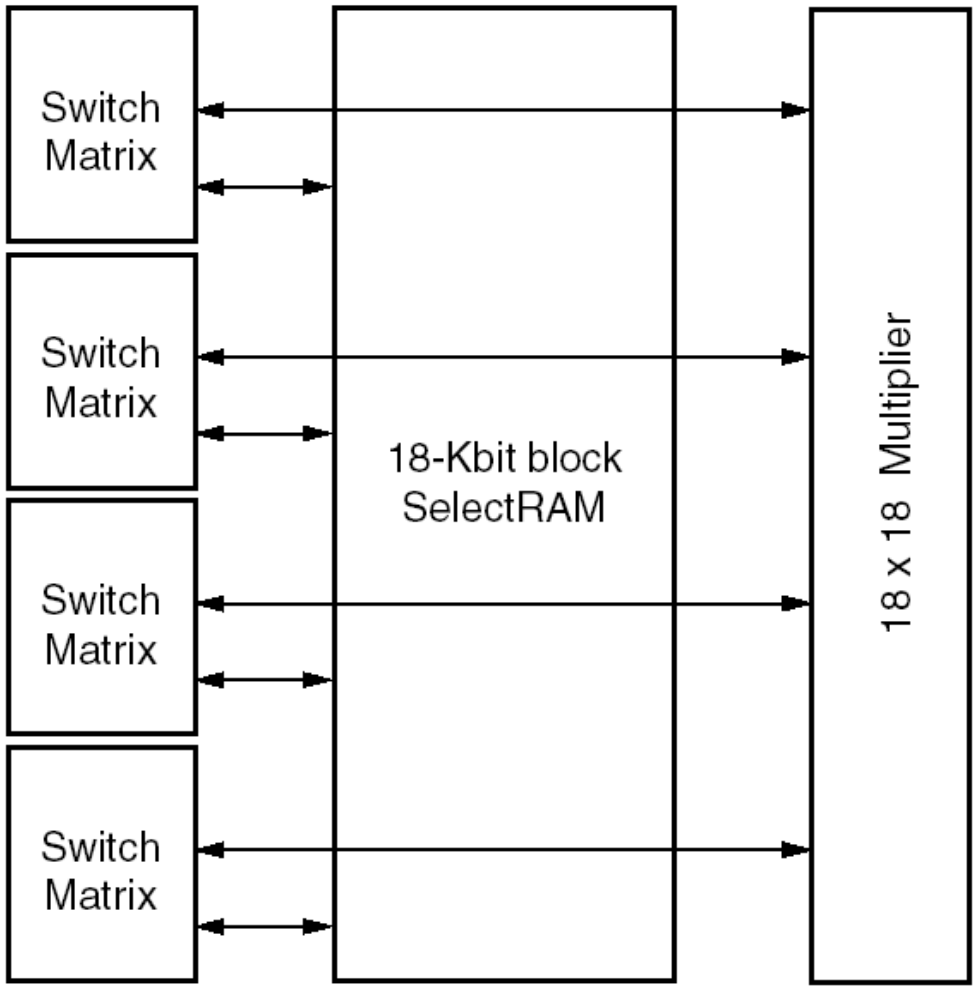


Embedded RAM

- Xilinx – Block SelectRAM
  - 18Kb dual-port RAM arranged in columns
- Altera – TriMatrix Dual-Port RAM
  - M512 – 512 x 1
  - M4K – 4096 x 1
  - M-RAM – 64K x 8



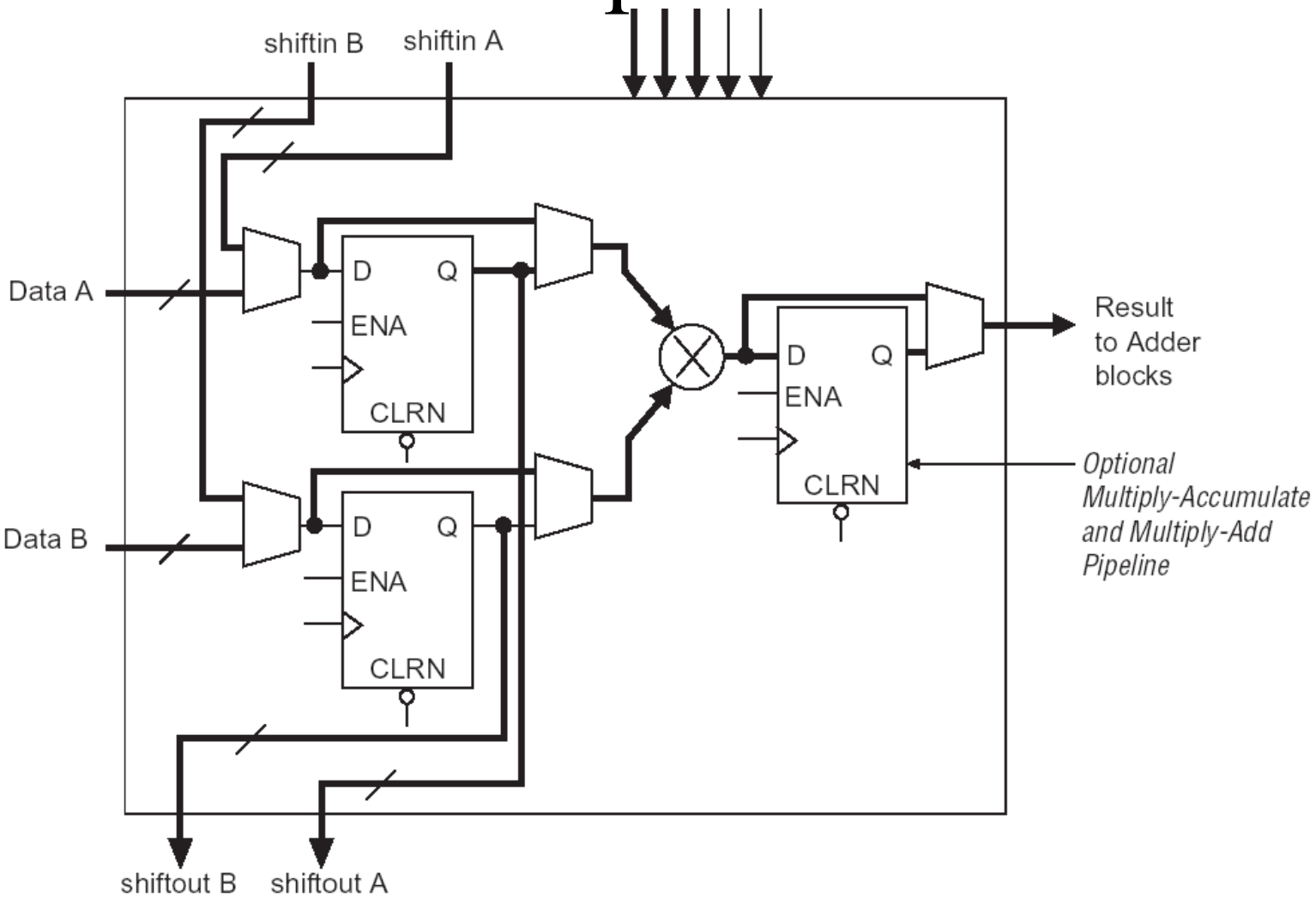
Xilinx: Embedded Multipliers



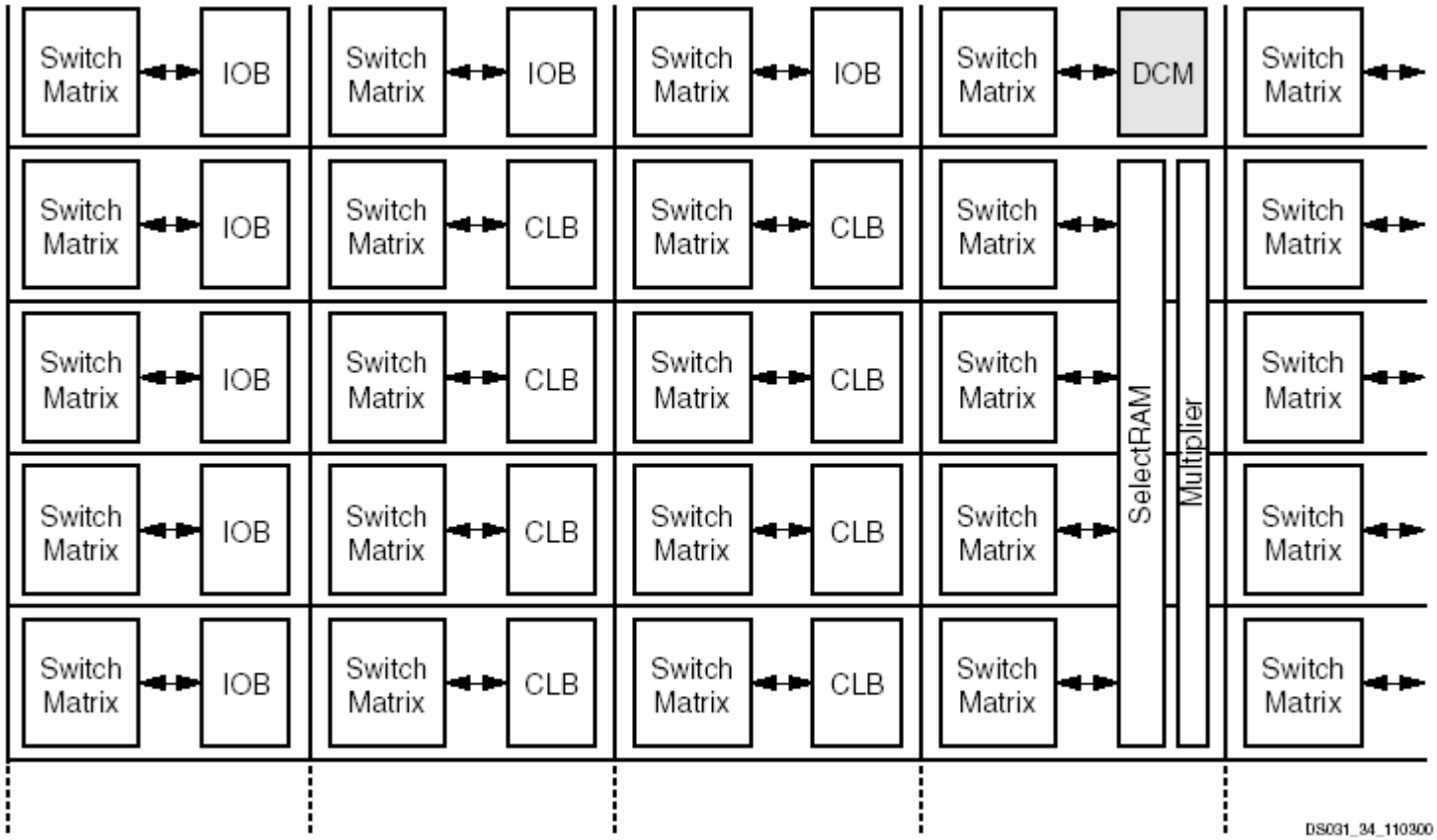
Altera: Embedded DSP Blocks

- Two DSP Block columns per device
- Number varies by height of column
- Can implement:
  - Eight 9x9 multipliers
  - Four 18x18 multipliers
  - One 36x36 multiplier
- Contains adder/subtracter/accumulator
- Registered inputs can become shift register

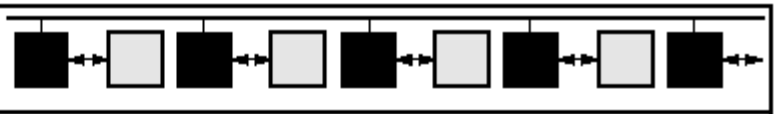
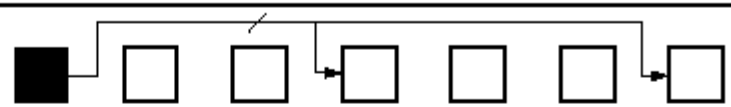
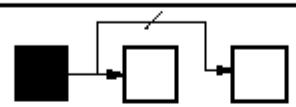
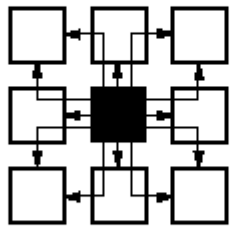
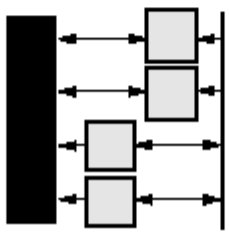
Altera Multiplier Sub-block



Virtex: Active Interconnect



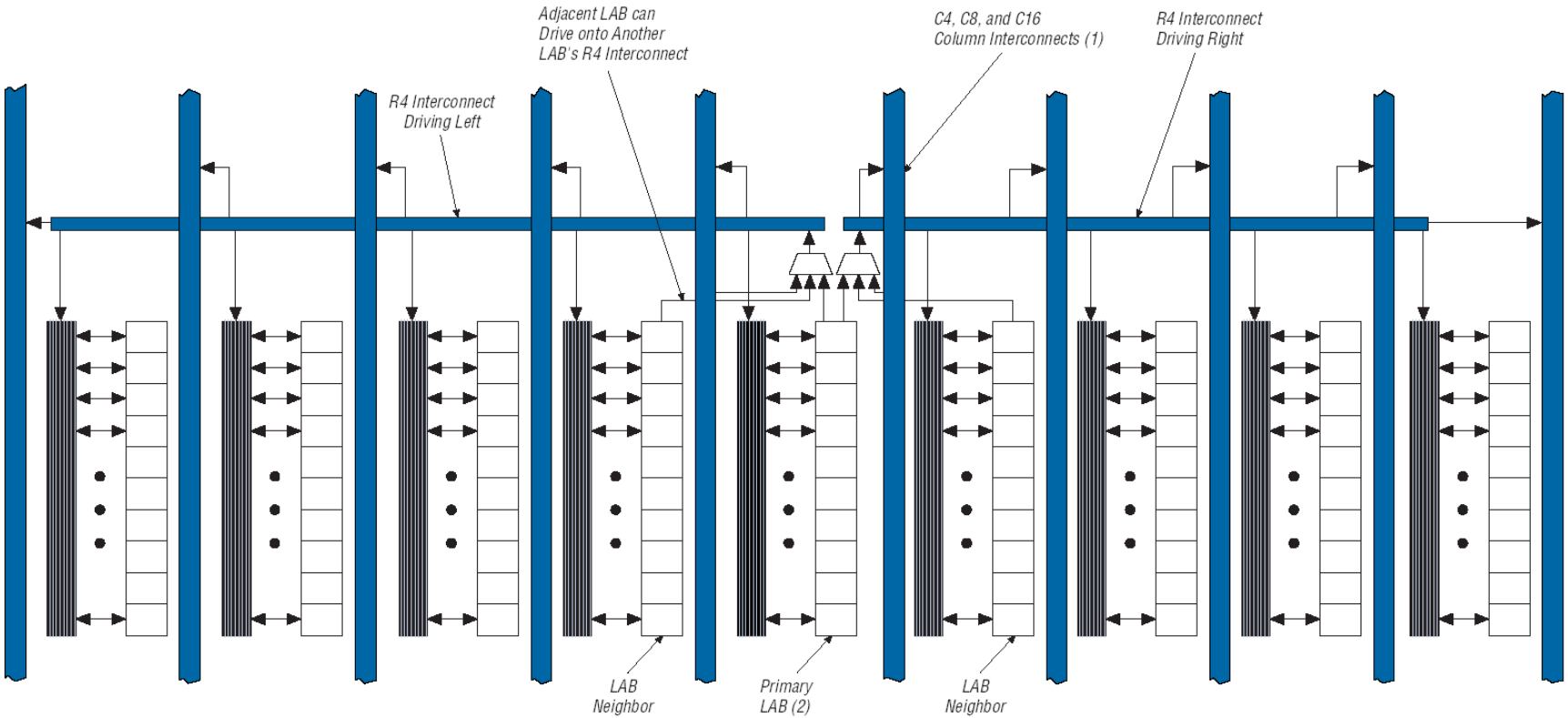
Virtex Hierarchical Interconnect

24 Horizontal Long Lines 24 Vertical Long Lines	
120 Horizontal Hex Lines 120 Vertical Hex Lines	
40 Horizontal Double Lines 40 Vertical Double Lines	
16 Direct Connections (total in all four directions)	
8 Fast Connects	

Altera: MultiTrack Interconnect

- Direct link between LABs and adjacent blocks
- Row interconnects
  - 4, 8, and 24 blocks left or right
- Column interconnects
  - 4, 8, and 16 blocks up or down

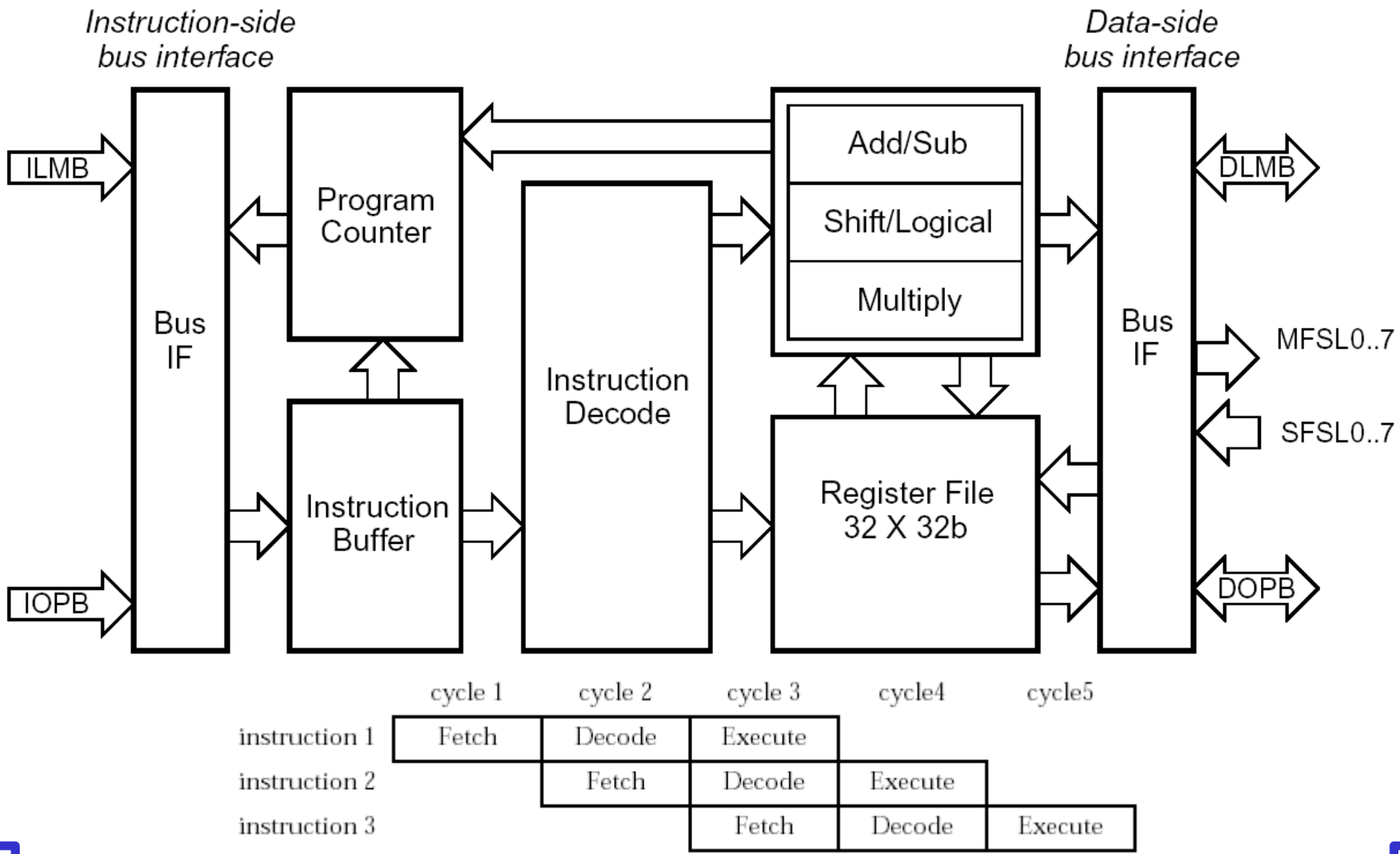
Stratix: R4 Interconnect



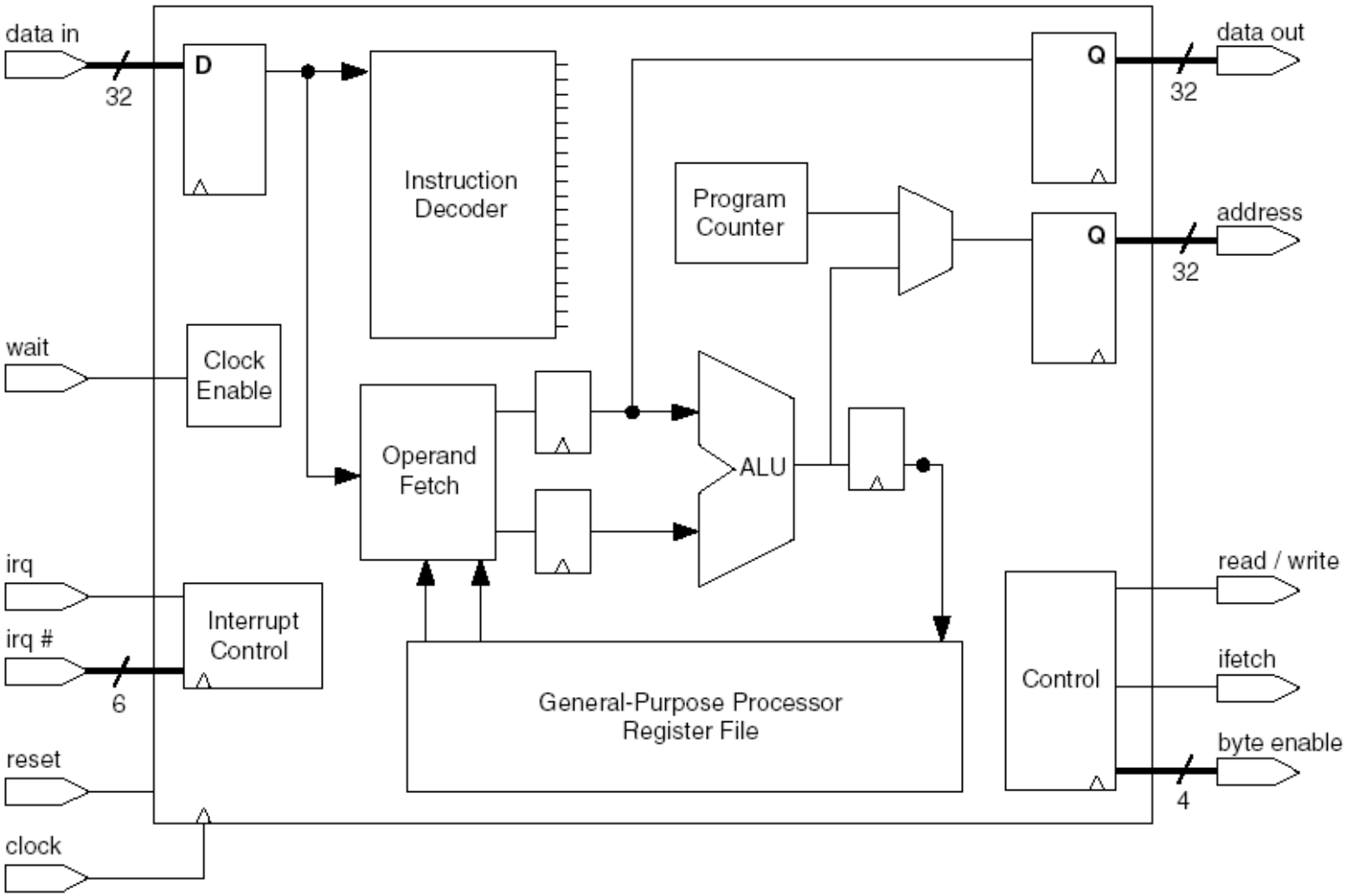
Big Differences

- Xilinx
  - 3DES bitstream decrypter on-board
  - RocketIO serial transceivers
  - Partial reconfiguration
- Altera
  - Documented self-reconfiguration in Excalibur

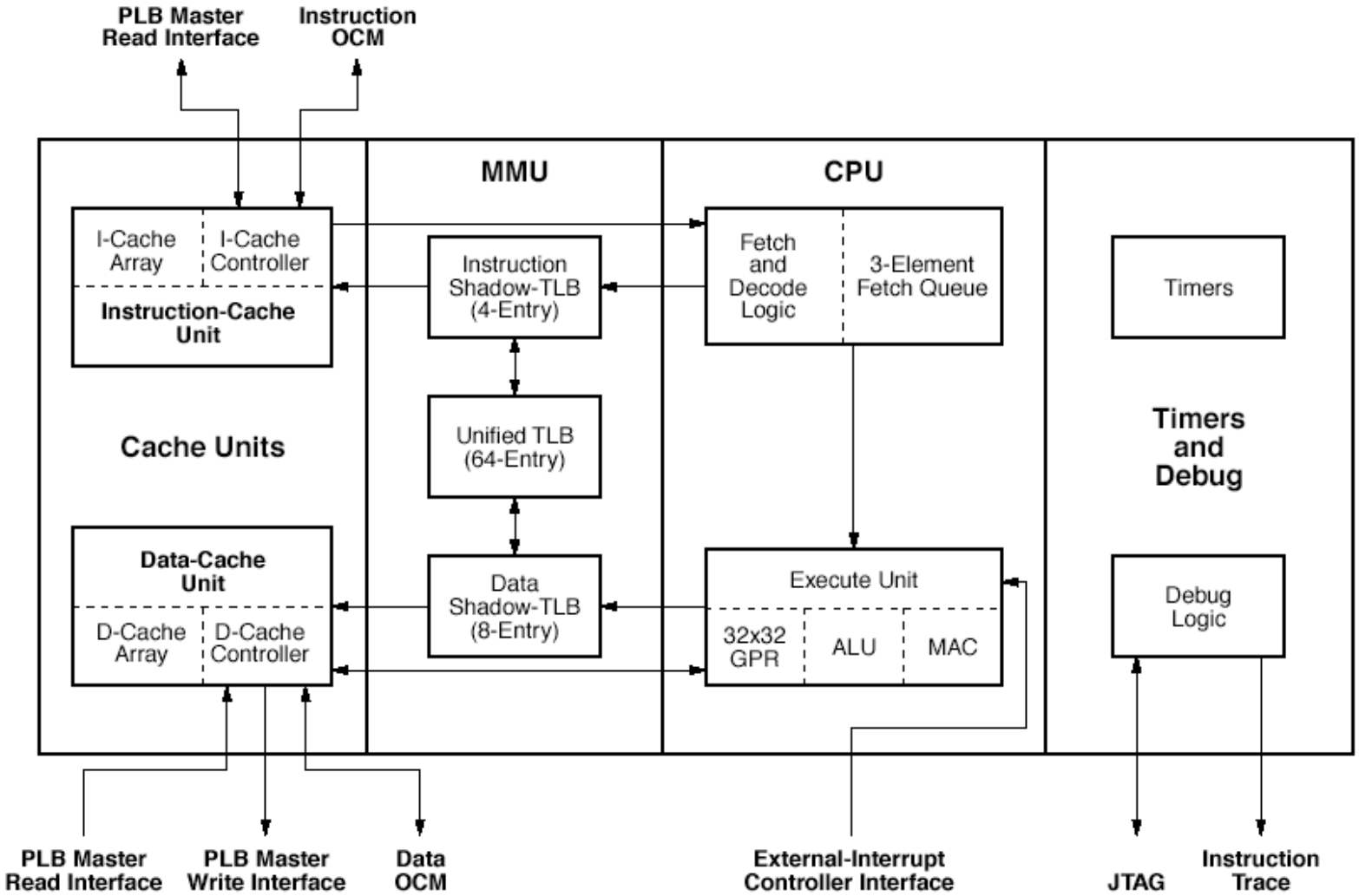
Xilinx MicroBlaze



Altera Nios


data in
32
D
Instruction Decoder
Program Counter
Q
data out
32
Q
address
32
wait
Clock Enable
Operand Fetch
ALU
irq
irq #
6
Interrupt Control
General-Purpose Processor Register File
Control
read / write
ifetch
byte enable
4
reset
clock

Virtex PowerPC Core



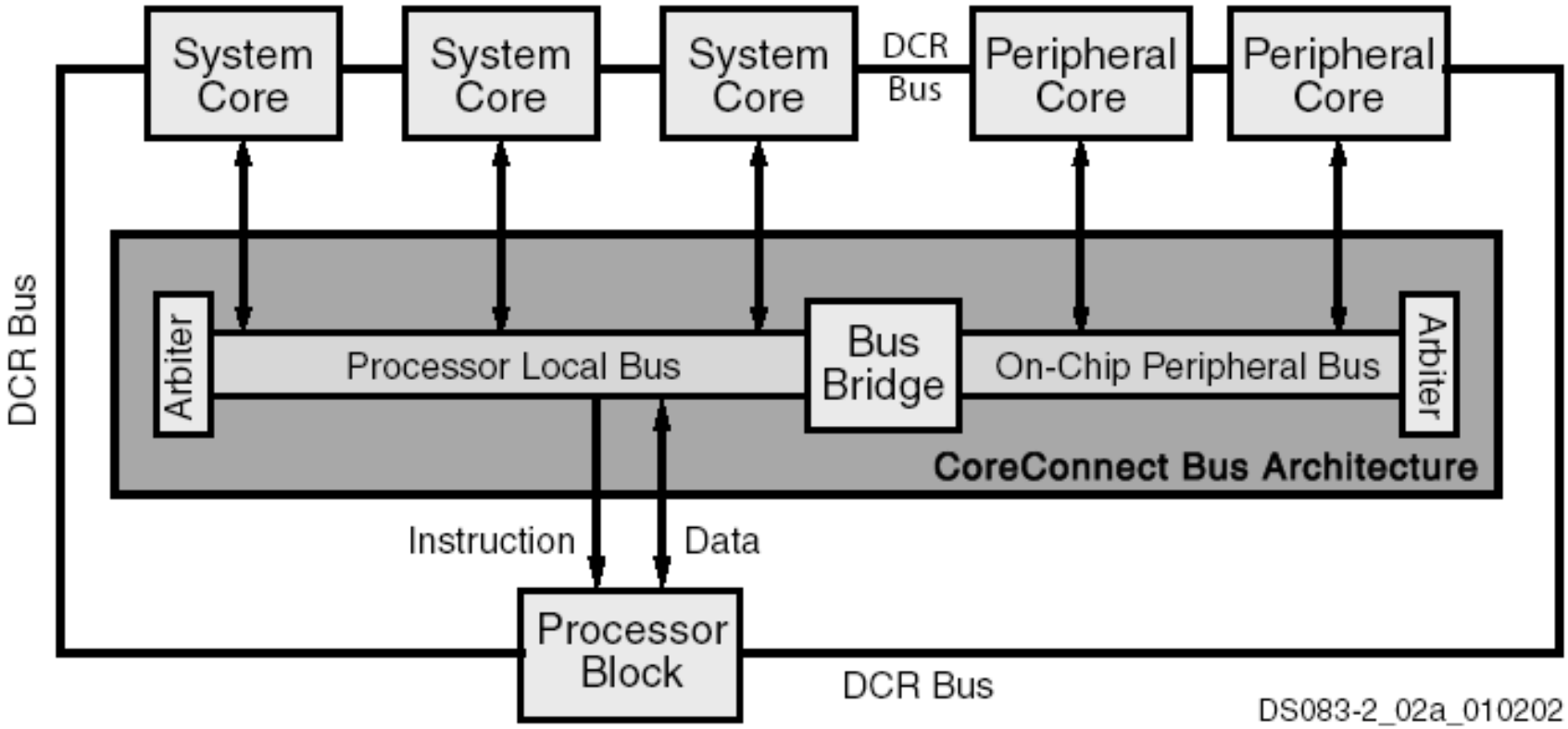
PowerPC 405

- Five-stage pipeline
- Independent instruction and data caches
  - 16KB two-way set associative (256 x 32B)
  - Write-back or write-through data cache
- Static branch prediction
- Real memory management unit
  - TLB, memory protection
- 300MHz+, 420 MIPS

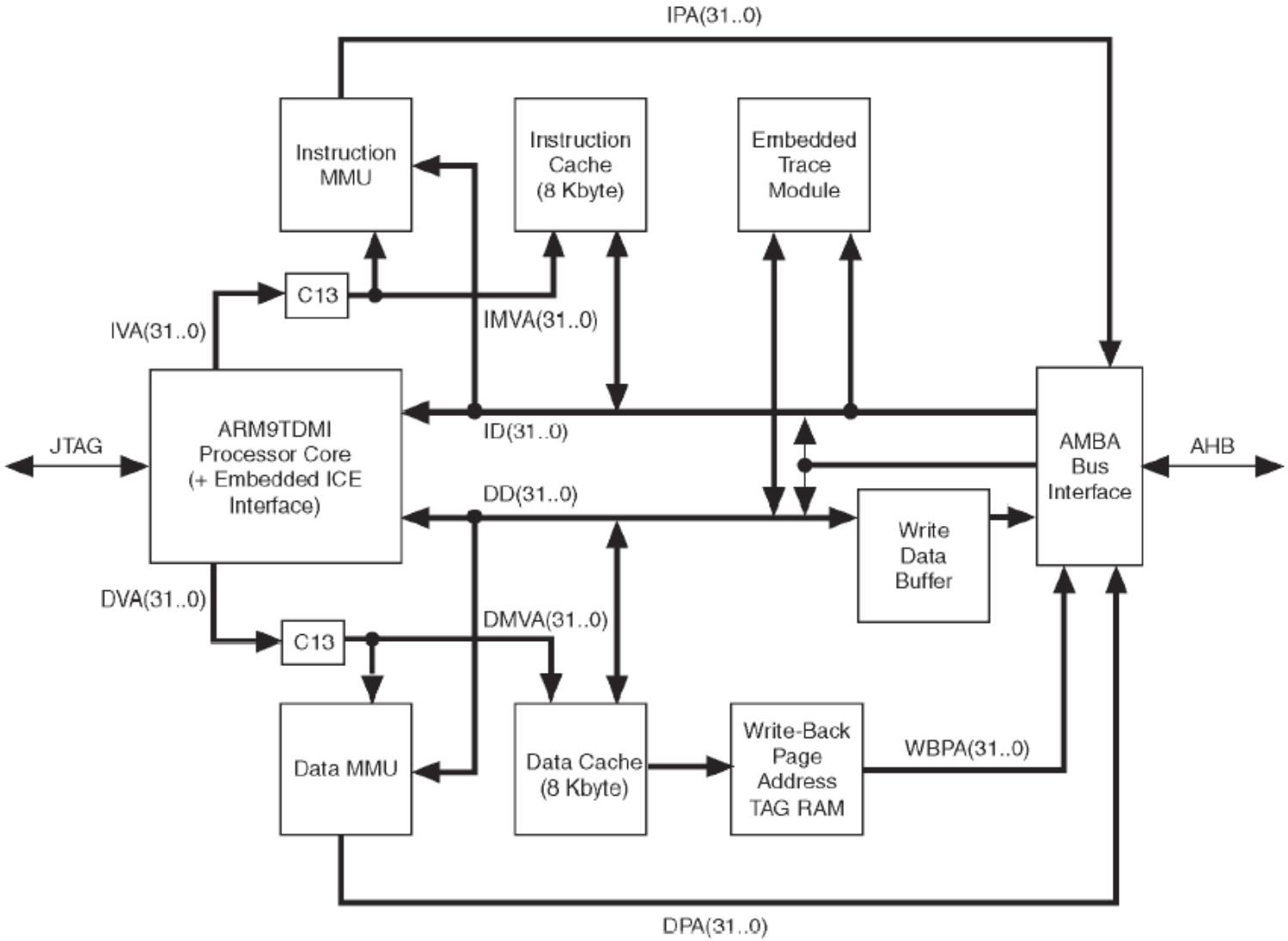
Interface to Virtex

- On-Chip Memory Controller (OCM)
  - Interface between PowerPC core and BRAM
  - Separate data and instruction OCMs
  - Scratch-pad memory
  - Bi-directional data transfer to FPGA blocks
  - Storage is interrupt service routines
- Processor Local Bus

Processor Local Bus



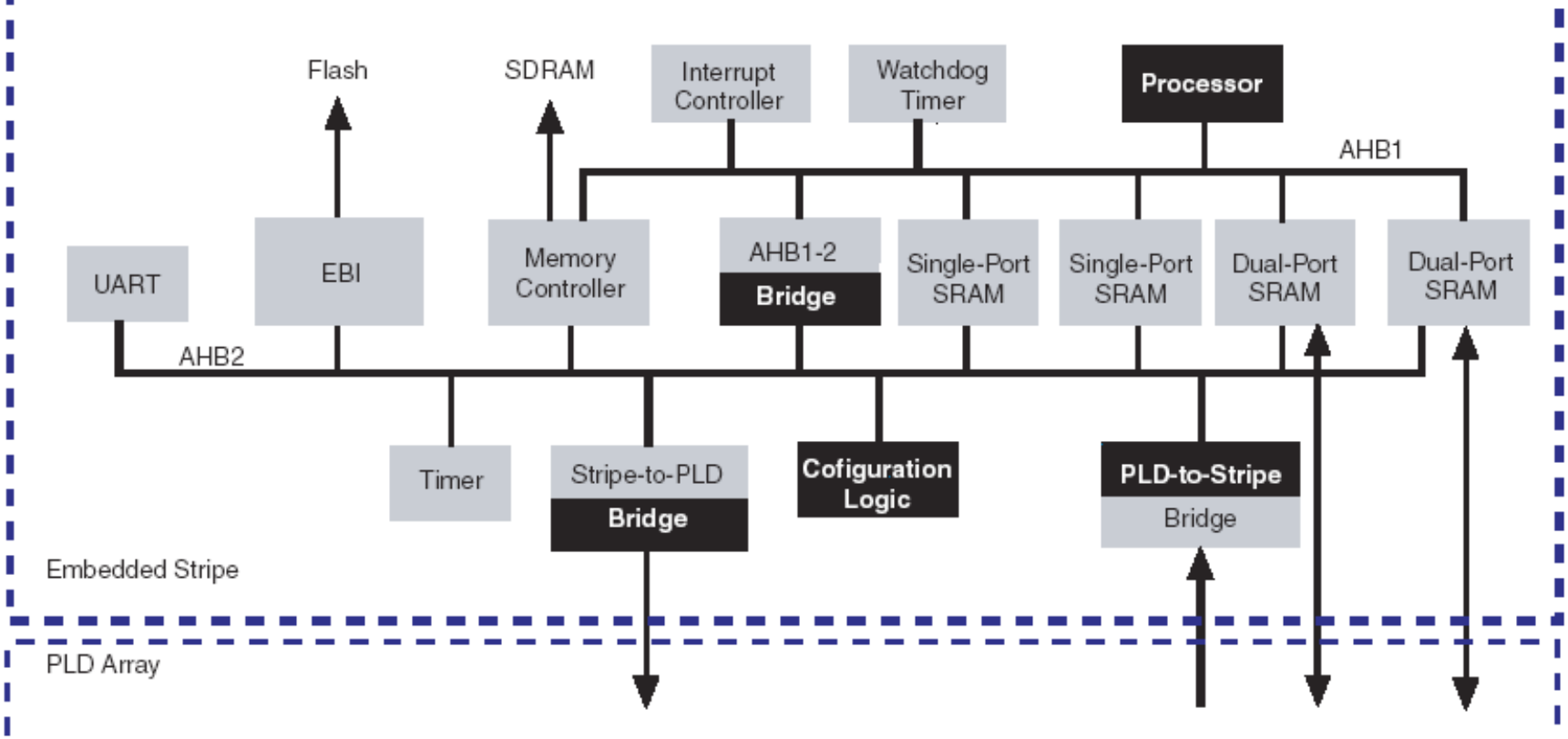
Excalibur ARM Core



ARM 922T

- Single “stripe” embedded in Apex 20K
- Five-stage pipeline
- 8KB 64-way set-associative instruction and data caches
- 256KB internal single-port SRAM
- 128KB internal dual-port SRAM
- All FPGA interface through ABMA buses

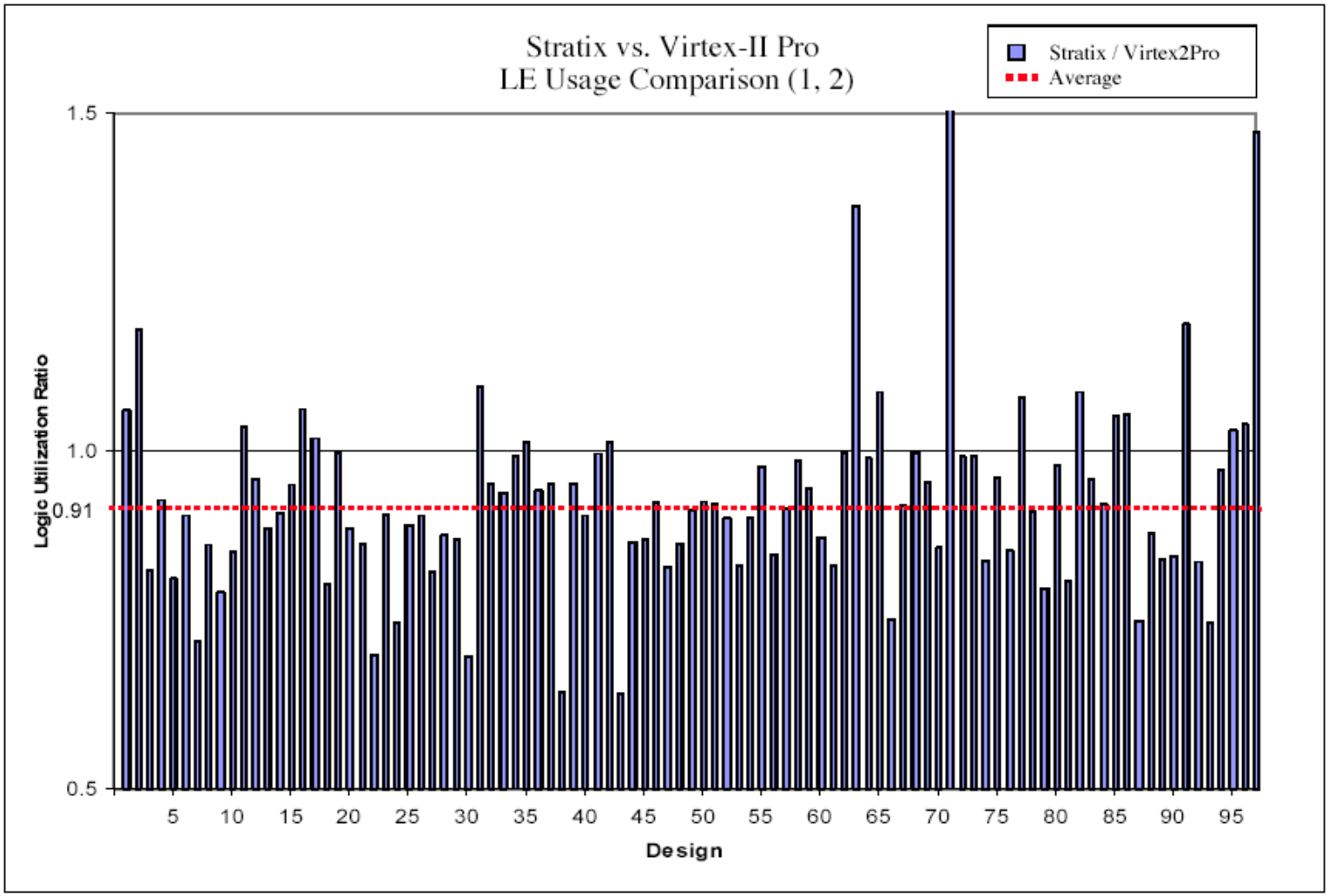
ARM922T Stripe



Head-to-Head

- Implement 97 customer designs
- Sizes up to 61,000 LEs
- Basic unit of comparison: LE
  - 4-LUT, register, and anything else associated
- 80% are more efficient on Altera
- Uses on average 9% fewer LEs
- 41% are >10% more efficient

Logic Utilization



DSP Block vs. 18x18 MUL

Table 4. Stratix vs. Virtex-II Pro Multiplier Implementation Resource Requirement Comparison

Multiplier Size	Resources			
	Stratix		Virtex-II Pro	
	DSP Block	LE (2)	18x18 Multiplier Block	LE (2)
Signed 9x9	1/8 *(1)*	0 [0]	1	0 [36]
Signed 18x18	1/4 *(1)*	0 [0]	1	0 [72]
Signed 36x36	1	0 [0]	4	326 [397]
18x18 MAC	1/2	0 [0]	1	49 [134]
18x18 Complex Multiplication	1	0 [0]	4	76 [153]
4 Tap, 16-bit FIR Filters with Parallel Inputs	1	[0]	4	[280]
4 Tap, 16-bit FIR Filters with Serial Inputs	1	[0]	4	[199]

Memory Comparison

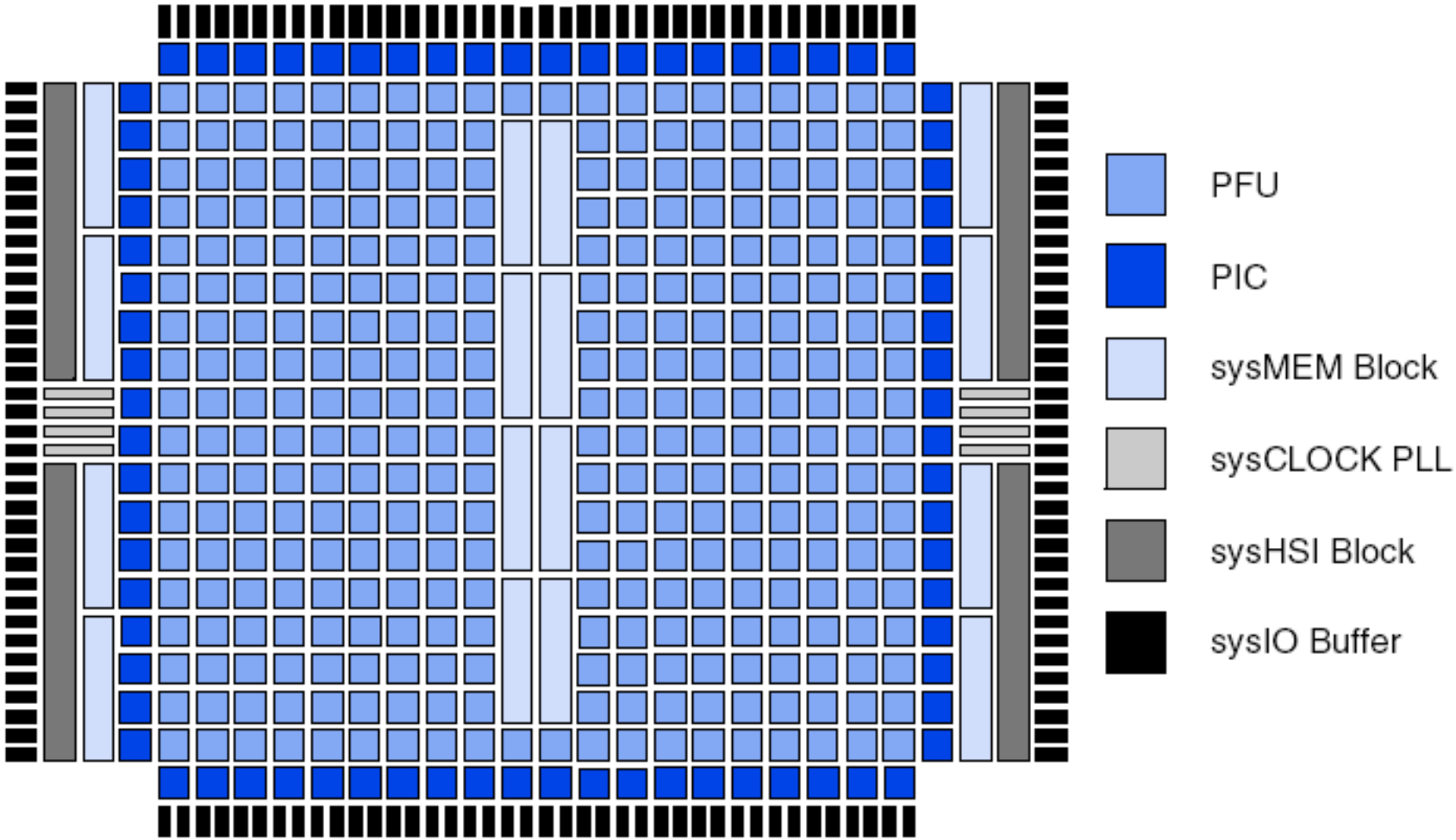
Table 5. Stratix and Virtex-II Pro Memory Resources Usage Comparison

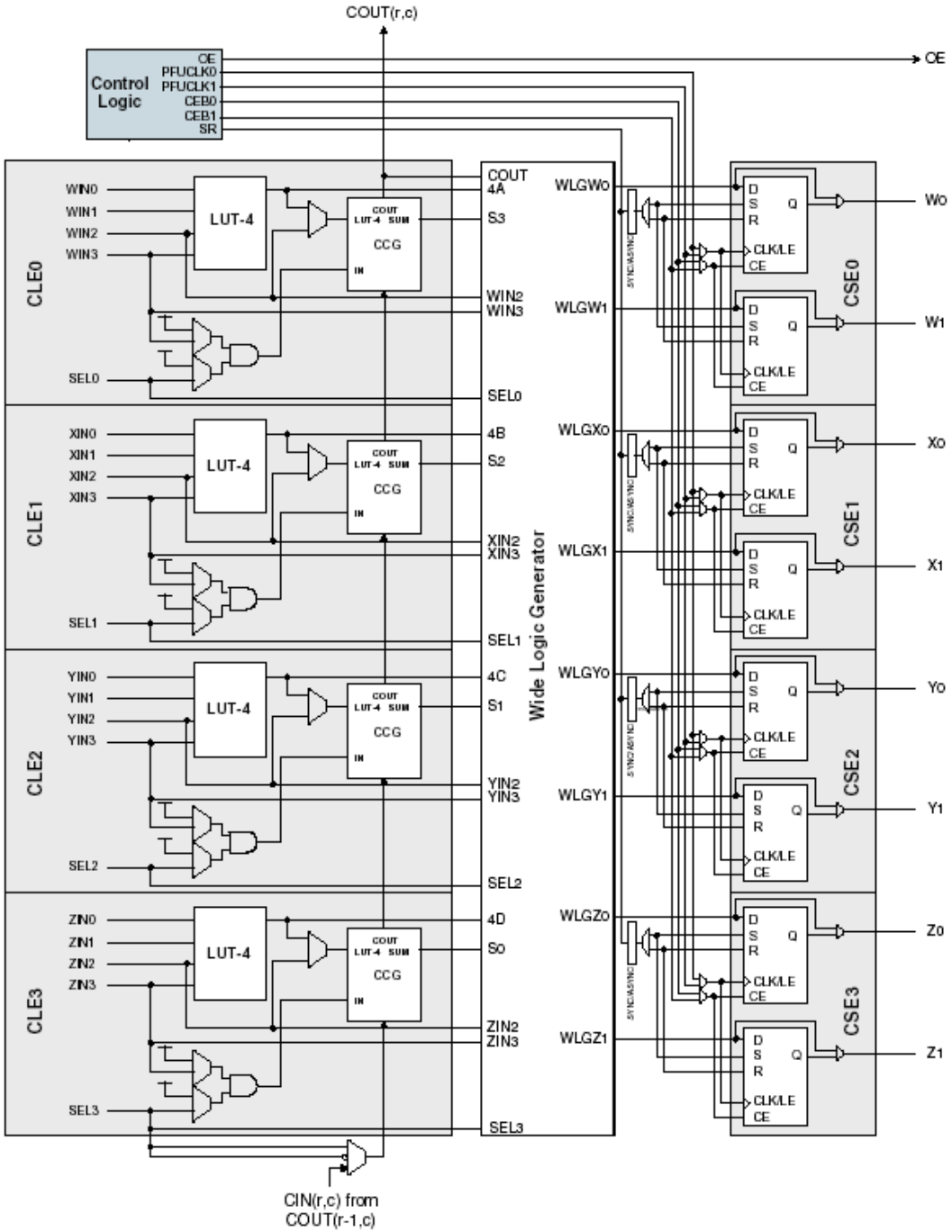
Memory Size	Stratix Memory Resources	Virtex-II Pro Memory Resources
< 1K bits	One or two M512s	LEs used as distributed SelectRAM+
		One 18Kb block SelectRAM+ (94+% unused)
1K bits - 10K bits	Multiple M512s or M4Ks	LEs used as distributed SelectRAM+
		One 18Kb block SelectRAM+ (44-94% unused)
>= 10 Kbits	M4Ks or M-RAM	1 or Multiple 18Kb block SelectRAM+

Lattice Semiconductor ispXPGA

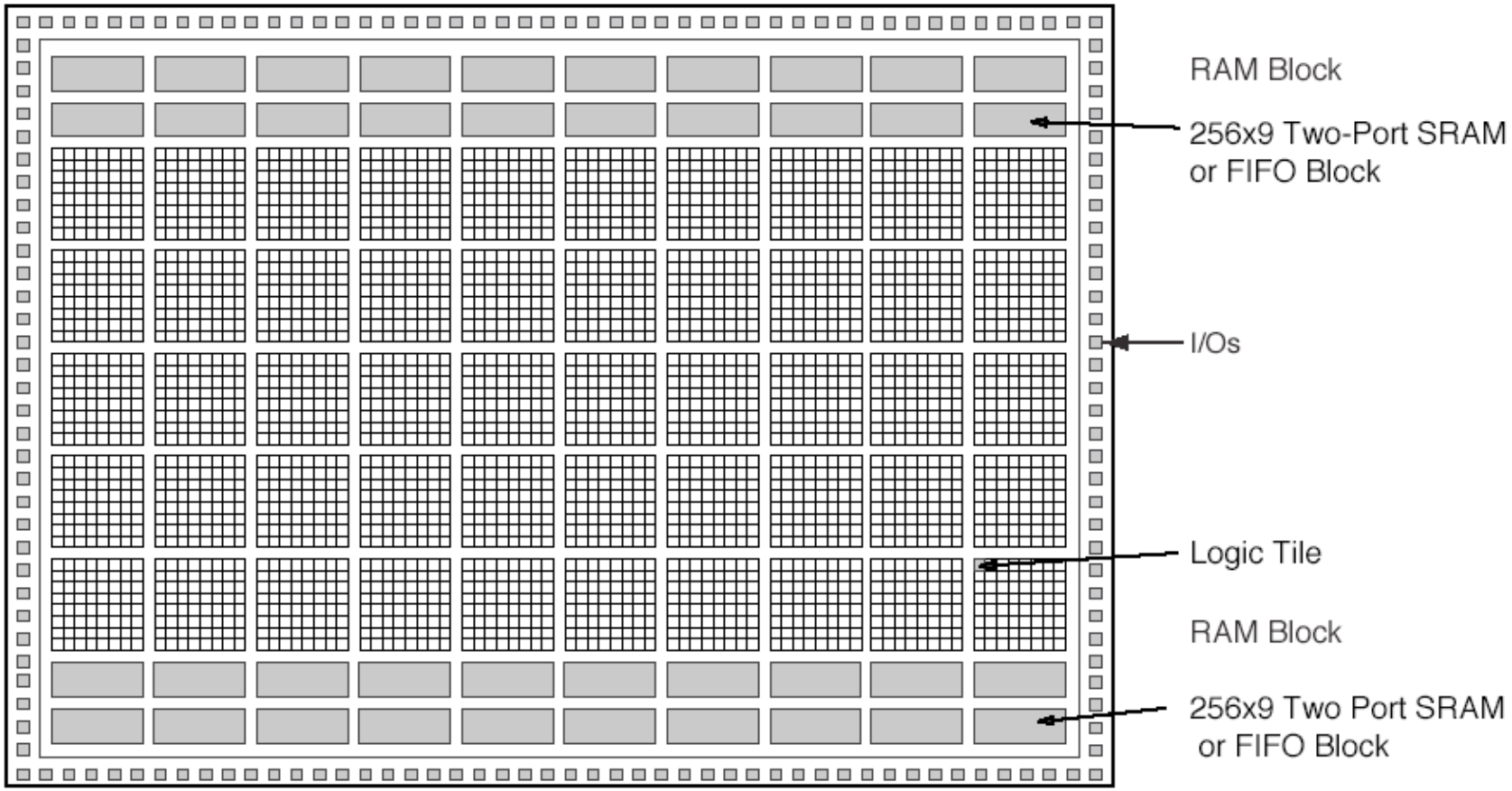
- E^2CMOS built-in to FPGA die stores configurations
- Non-volatile, but still SRAM-based for infinite reconfigurability
- Four 4-LUTs per block
- Two flip-flops per 4-LUT
- Small embedded RAMs

ispXPGA


PFU
PIC
sysMEM Block
sysCLOCK PLL
sysHSI Block
sysIO Buffer


COUT(r,c)
Control Logic
CE
PFUCLK0
PFUCLK1
CEB0
CEB1
SR
OE
CLE0
CLE1
CLE2
CLE3
WIN0
WIN1
WIN2
WIN3
XIN0
XIN1
XIN2
XIN3
YIN0
YIN1
YIN2
YIN3
ZIN0
ZIN1
ZIN2
ZIN3
SEL0
SEL1
SEL2
SEL3
LUT-4
COUT
LUT-4 SUM
CCG
IN
COUT
4A
4B
4C
4D
S3
S2
S1
S0
Wide Logic Generator
WLGWo
WLGW1
WLGXo
WLGX1
WLGYo
WLGY1
WLGZo
WLGZ1
SYNCASYNC
D
S
R
Q
CLK/LE
CE
CSE0
CSE1
CSE2
CSE3
Wo
W1
Xo
X1
Yo
Y1
Zo
Z1
CIN(r,c) from
COUT(r-1,c)

Actel ProASIC



Actel ProASIC