Alternative Reconfigurable Architectures

ACME Seminar

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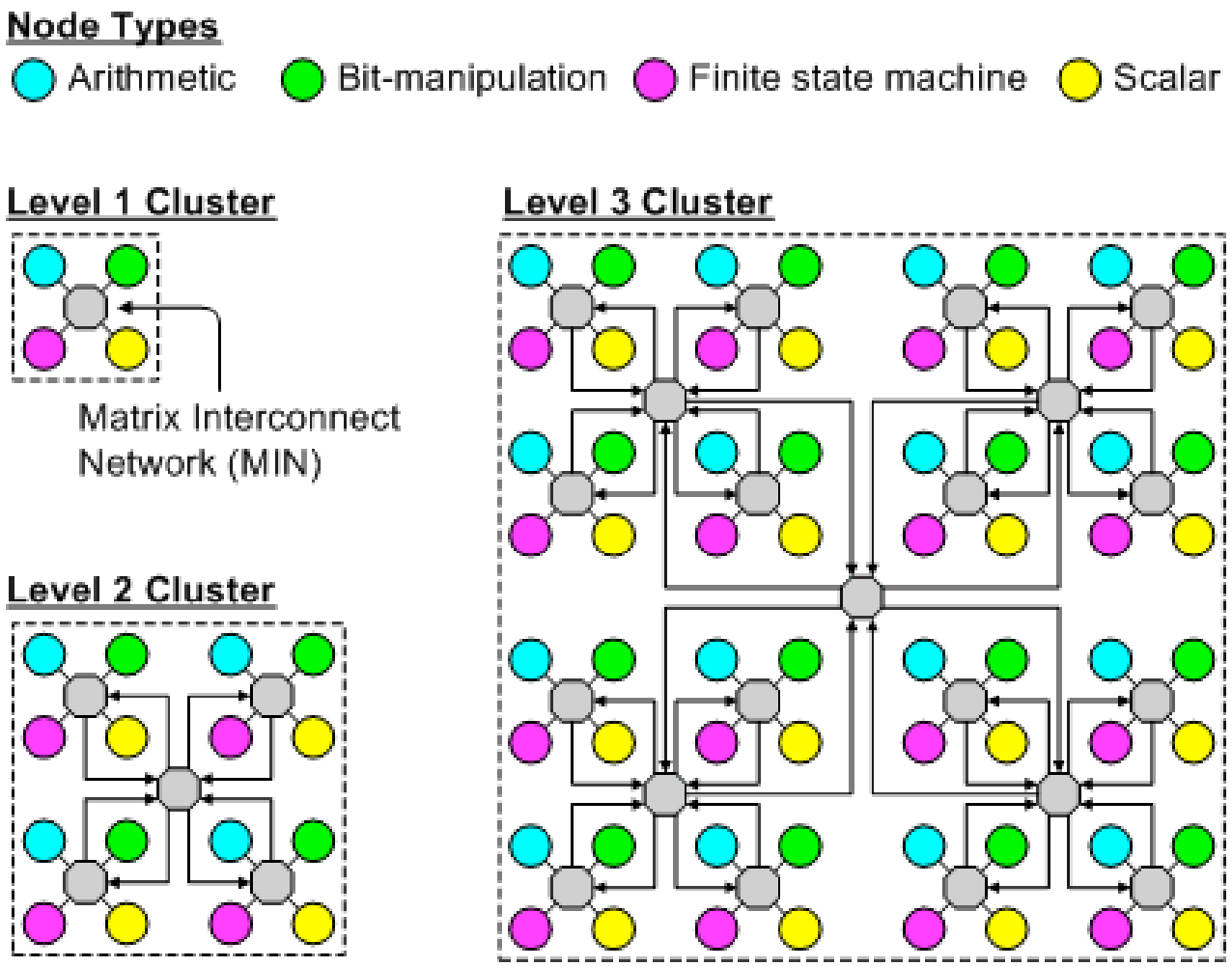
Life Beyond Virtex

- Added functionality
  - Virtex-II Pro, Altera Excalibur
- Increased granularity
  - QuickSilver ACM
  - PicoChip
  - PACT XPP
  - Morpho Technologies MS1
- Reduced granularity
  - Cell Matrix

QuickSilver ACM

- Targeting cellular handsets
  - W-CDMA, CDMA-2000, MPEG-4
- Diverse computational requirements are not good for “standard” homogenous FPGAs
- Uses a heterogeneous array of nodes instead

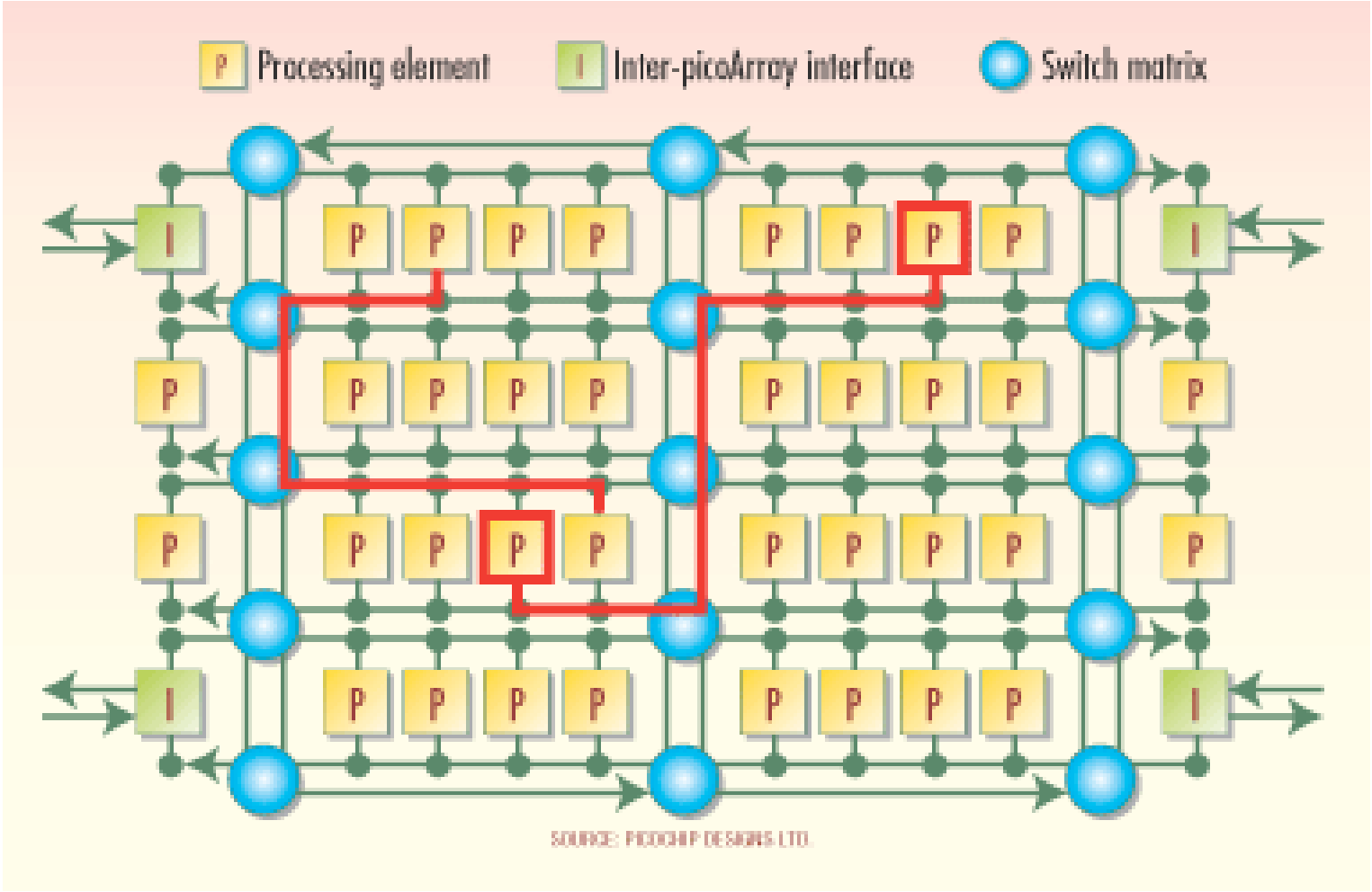
QuickSilver Architecture



PicoChip

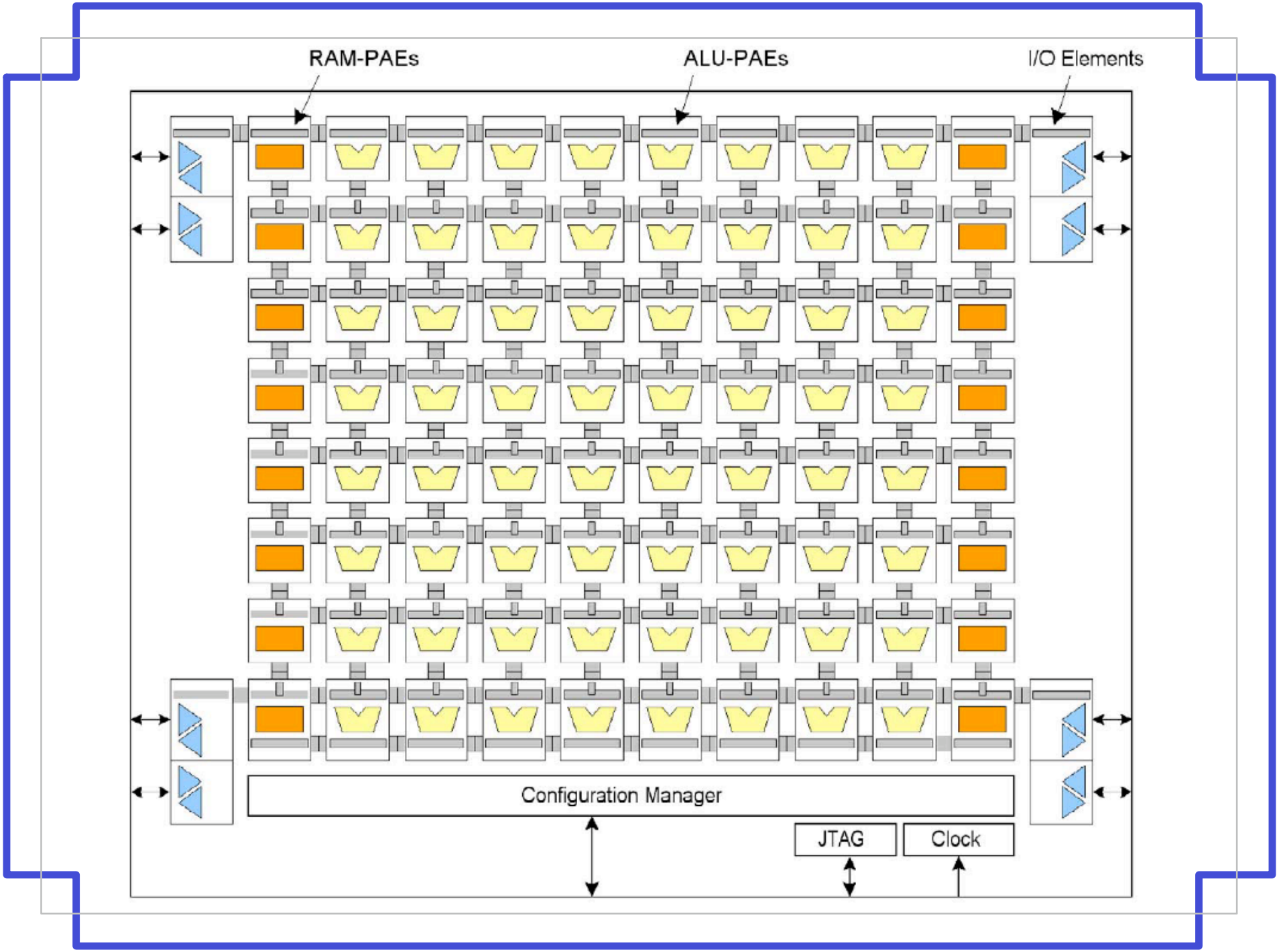
- Again, targeting W-CDMA
- Utilizes array of 430 processors on a single chip
- 13mm x 13mm die size, 160M transistors 0.13um TSMC
- 160MHz operation

PicoChip Architecture

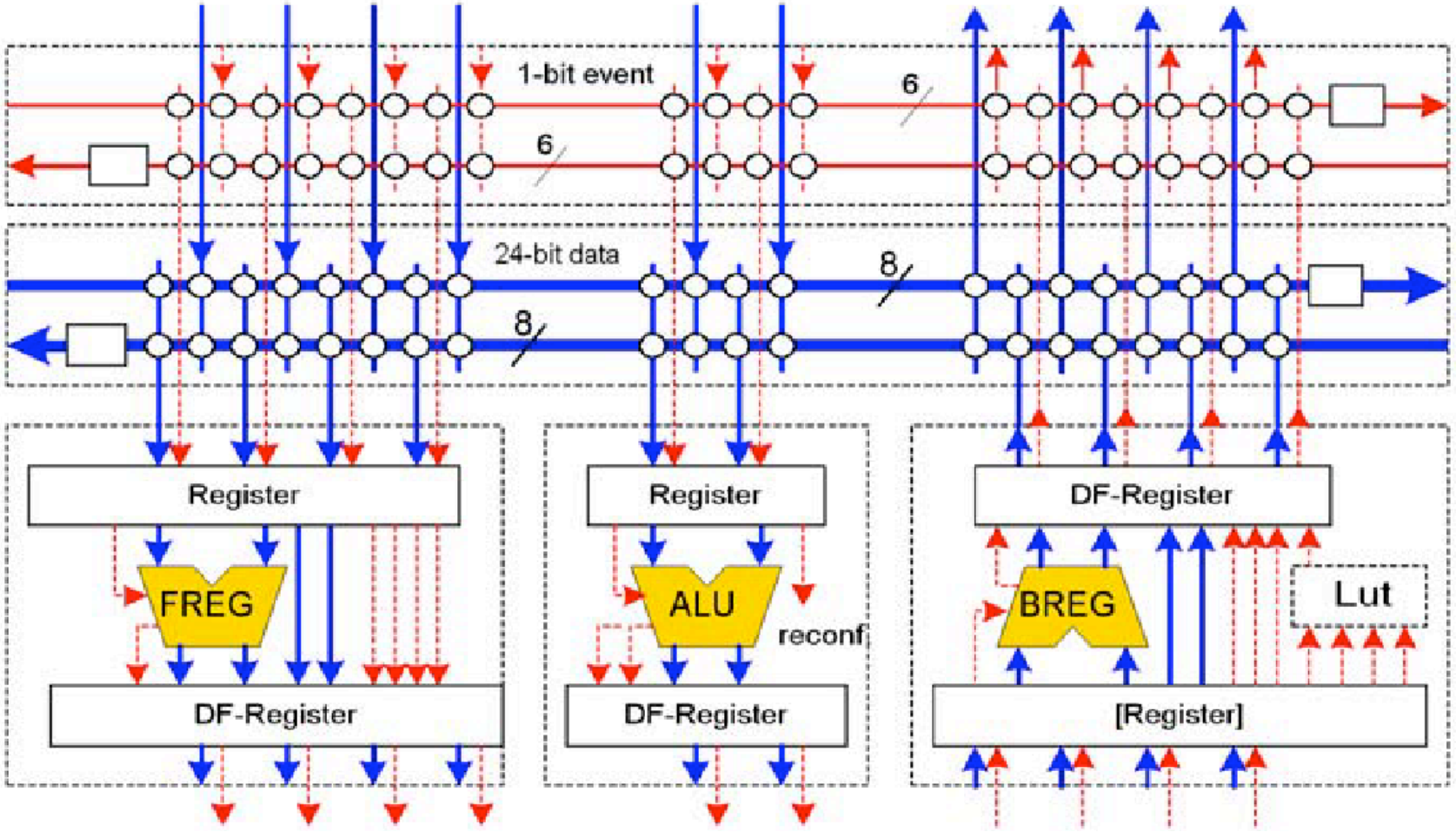


PACT XPP

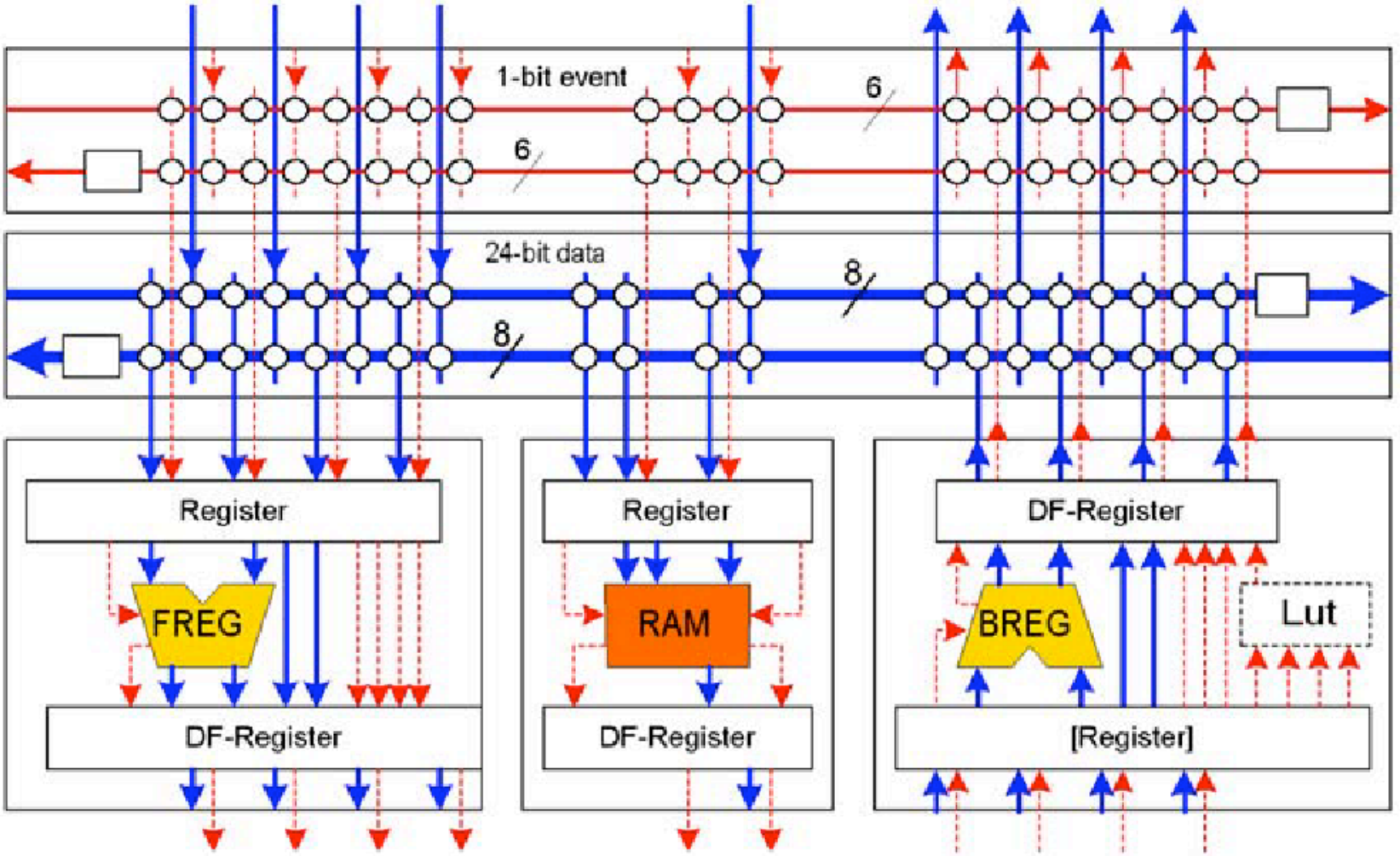
- Xtreme Processing Platform
- Developed as a synthesizable Verilog IP core
- Configurable
  - Word size (16/24/32-bit)
  - Routing and event channels
  - RAM size
  - I/O elements
- XPP64-A1 released as prototype


RAM-PAEs
ALU-PAEs
I/O Elements
Configuration Manager
JTAG
Clock

ALU-PAE


1-bit event
6
6
24-bit data
8
8
Register
FREG
DF-Register
Register
ALU
reconf
DF-Register
DF-Register
BREG
Lut
[Register]

RAM-PAE


1-bit event
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DF-Register
Register
RAM
DF-Register
DF-Register
BREG
Lut
[Register]

Results: OFDM Decoder

Decoder implementation

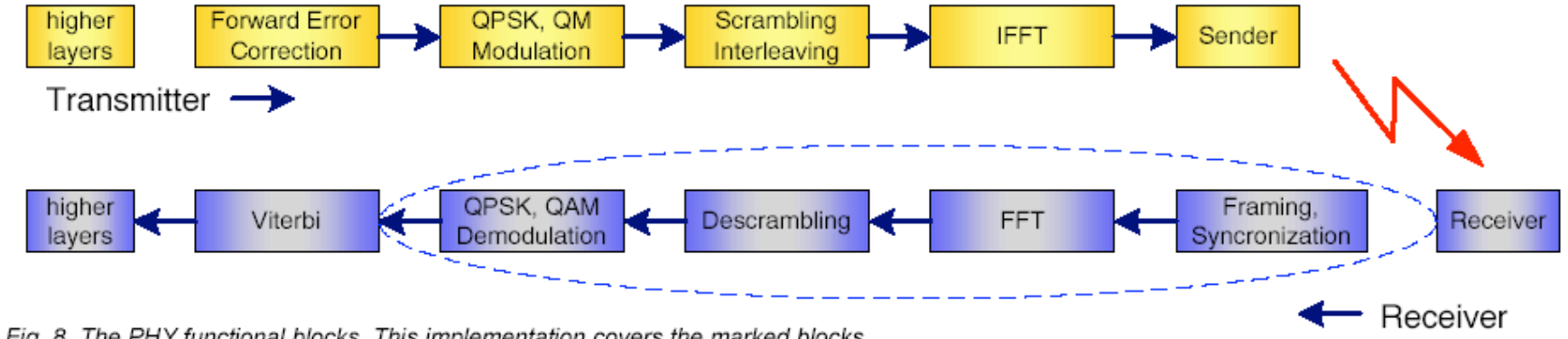


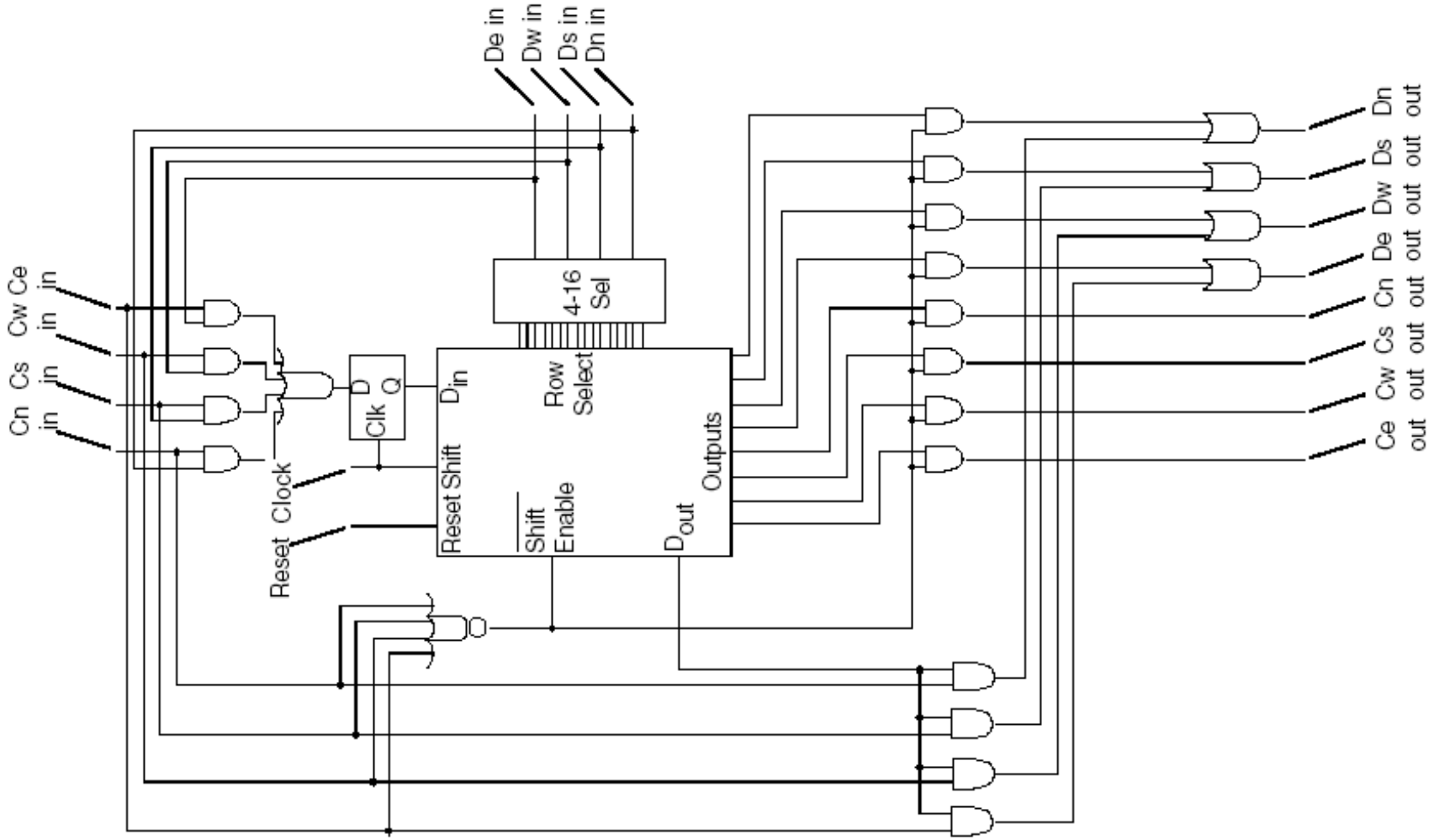
Fig. 8 The PHY functional blocks. This implementation covers the marked blocks.

- Burst rate: 40Mbit/s
- Raw rate: 24Mbit/s
- Power: 19.1mW
- Design clocked at 40MHz

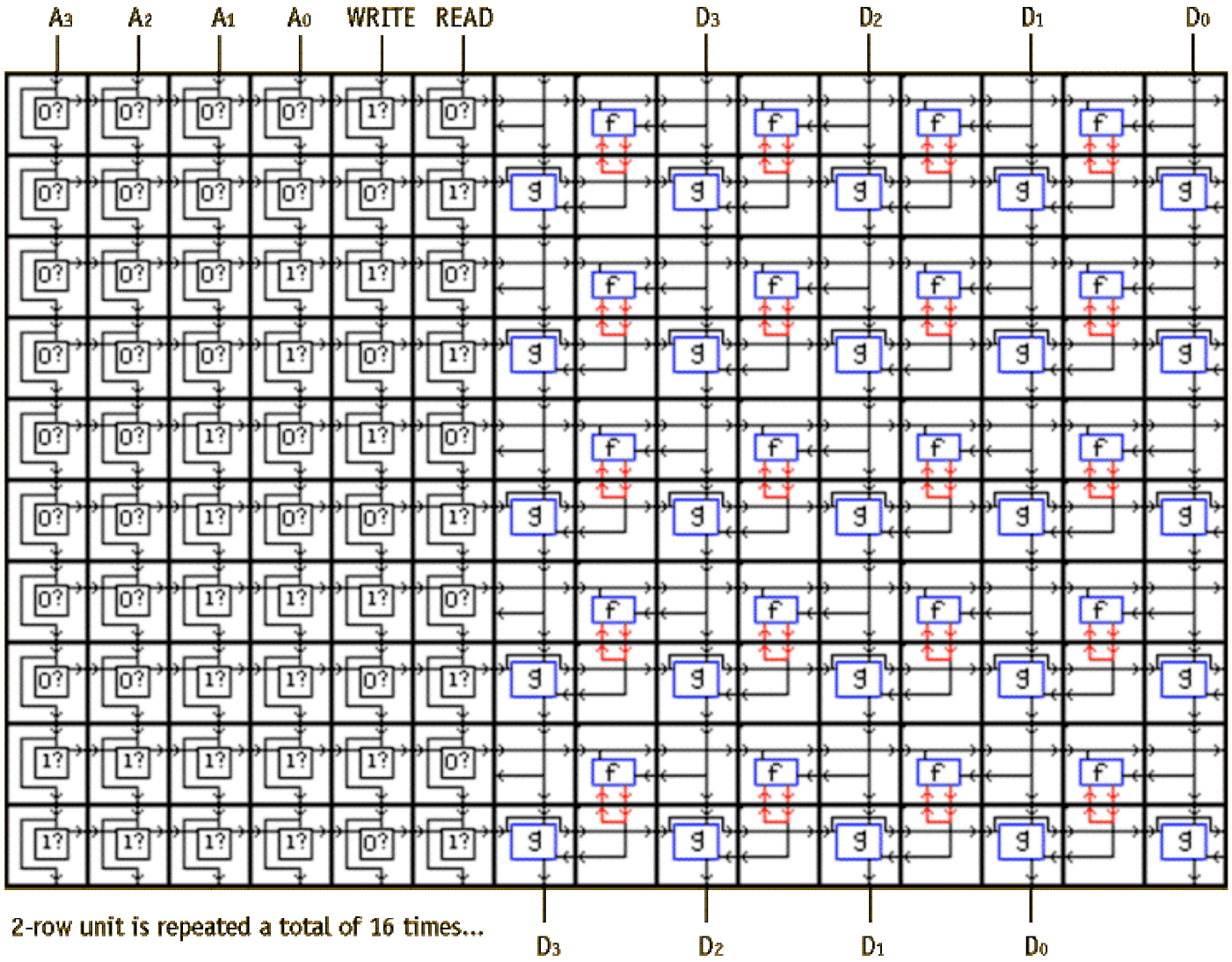
The Cell Matrix

- Given nano-scale switches, how do we organize them to perform computation?
  - Self-(re)onfiguration
  - Parallel confugration
  - Fault tolerance
  - Scalability
  - Easy to nano-fabricate

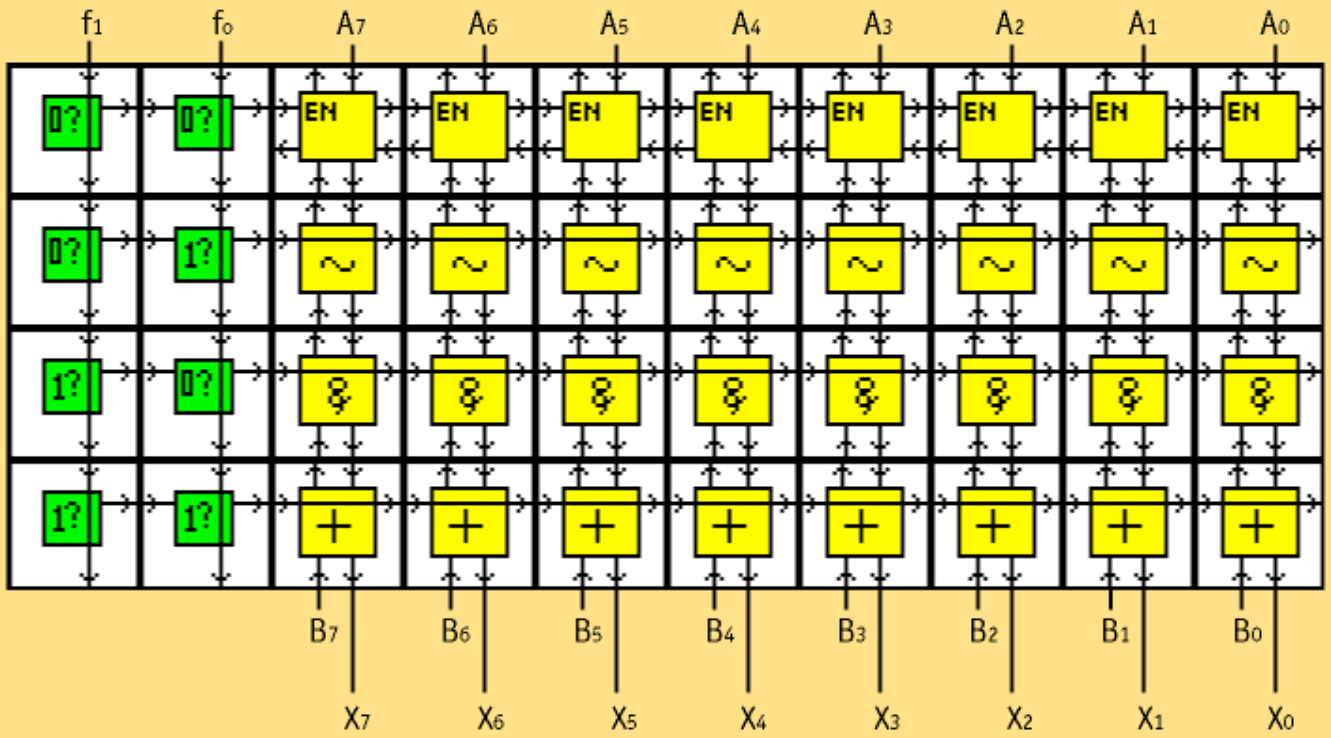
Single Cell Schematic



16 x 4 bit memory implemented on a set of Cell Matrix cells

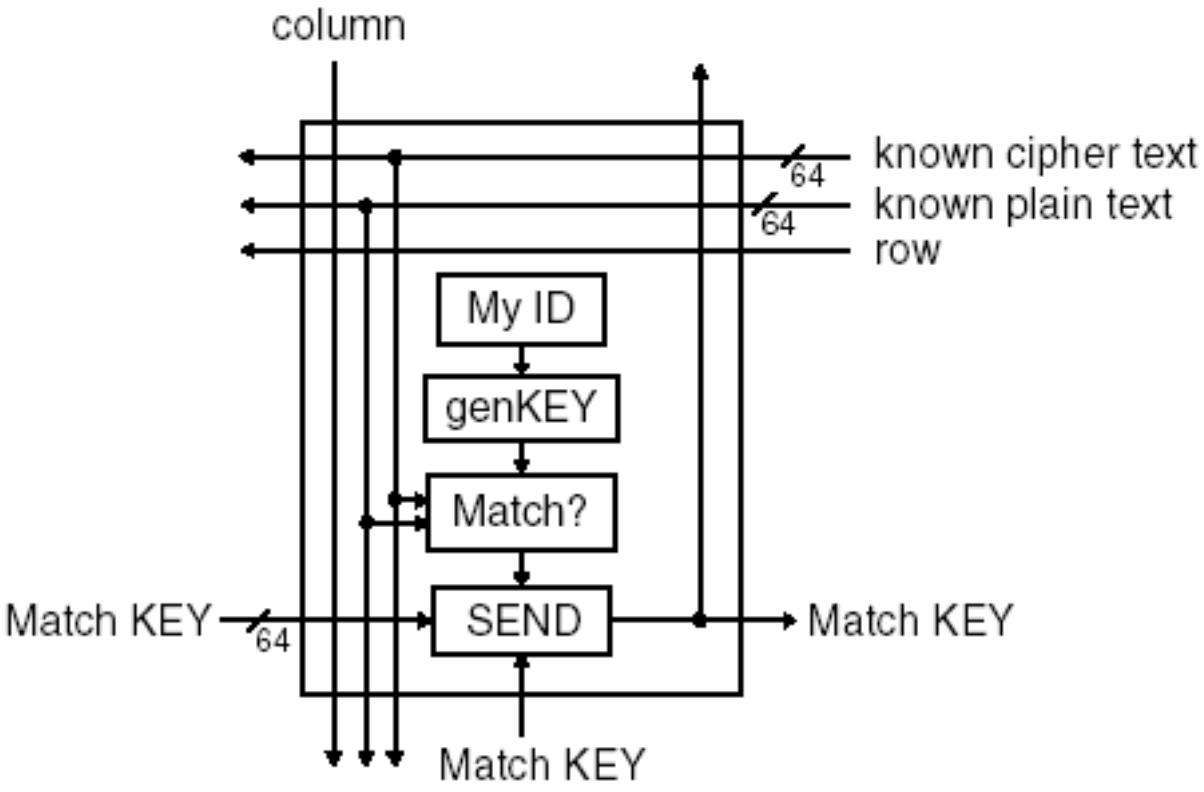


8-bit ALU

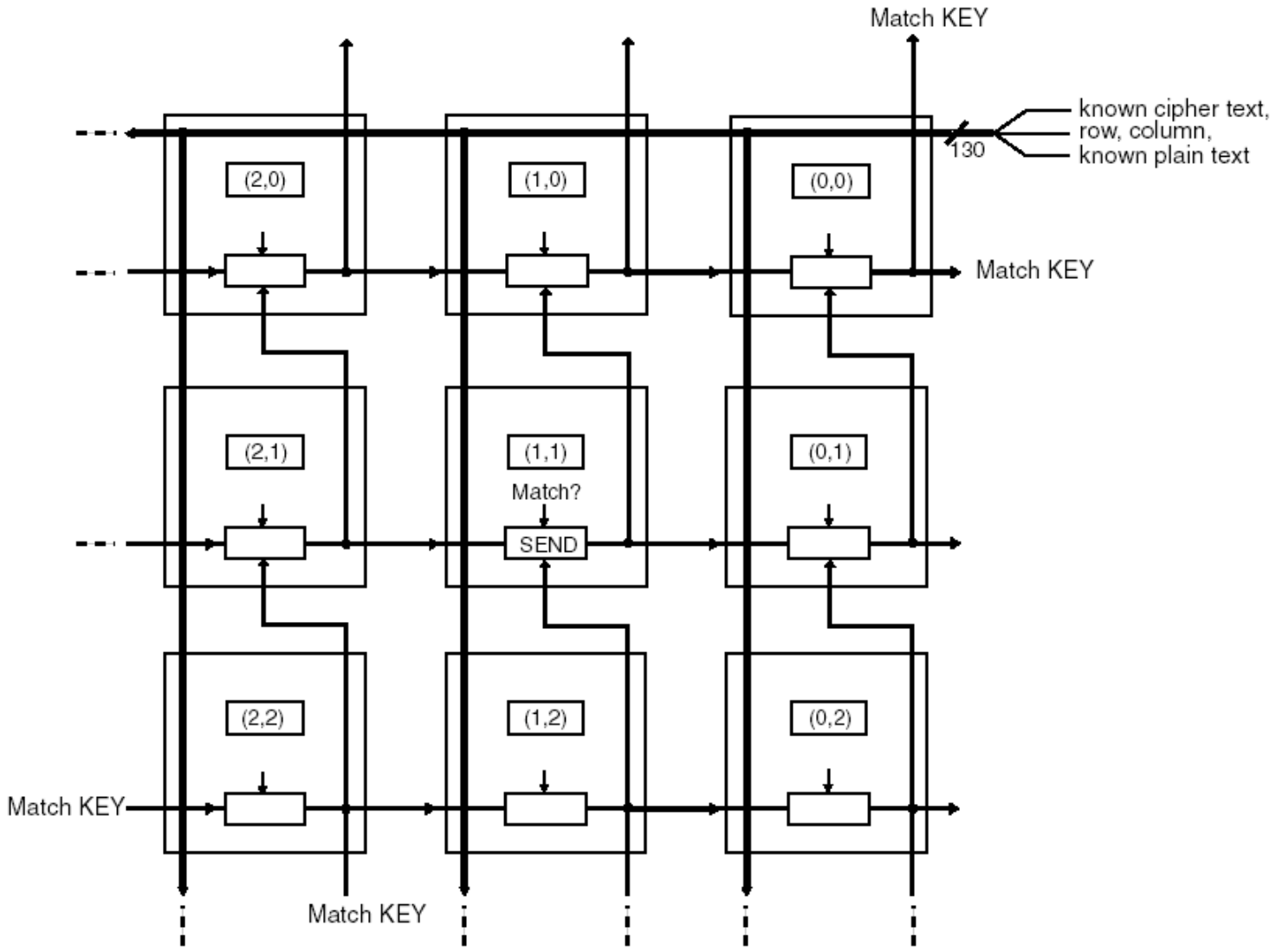


f_1	f_0	X
0	0	A + B
0	1	$\overline{A}$
1	0	A & B
1	1	A I B

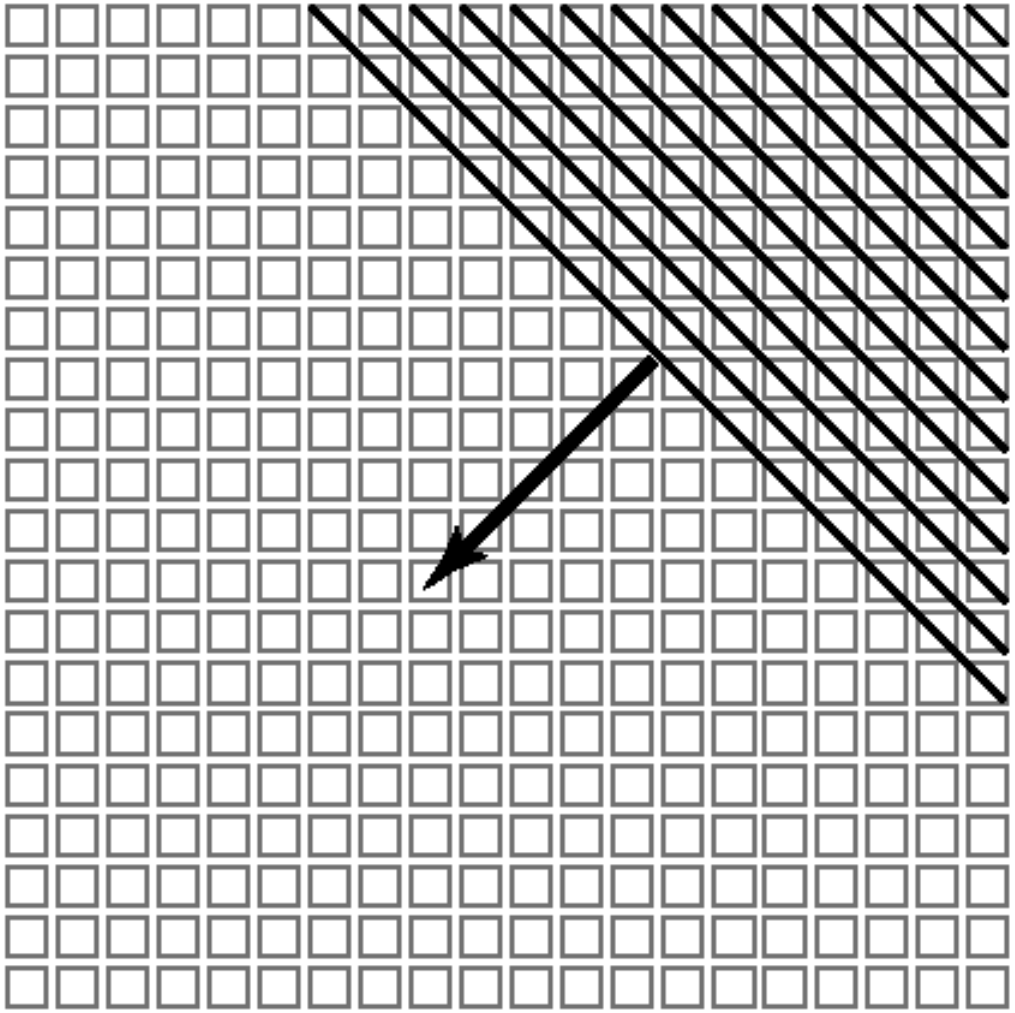
56-bit DES Decryption Processor



Communication Design



Parallel Self Configuration



Implementation Results

- Implemented four-bit DES cracker in simulation
  - Each processor is about 2500 cells
- For full 56-bit decryption
  - 10^17 processors
  - 4 million cells per processor
  - Assuming 1ps cell delay time, 200ms total propagation time across the cube = 40k characters/s decrypted