Survey of Nanoscale Digital System Technology

Mark L. Chang

ACME Seminar

May 10, 2002

Where did I get this info?

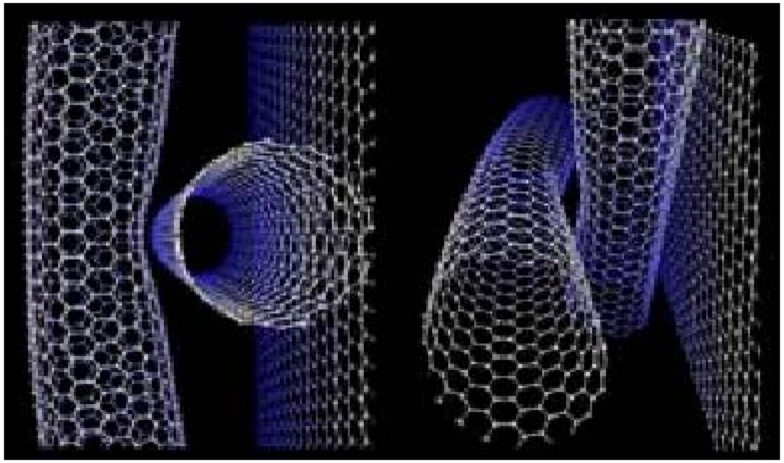
- Evening workshop at FCCM'02
- Mike Butts – moderator
- Panelists
  - Andre DeHon – Caltech
  - Phil Keukes – HP Labs

Nanoelectronics is T.N.B.T.™©®

- *The Next Big Thing*
- Molecular-scale devices
  - Programmable *only*
  - Good for FPGA and NVRAM architectures
  - Up to 1 *trillion* devices/sq. cm.
  - 1 million times smaller than today's "micro-scale" devices
- Mass fabricated cheaply
- Have some lab results right now
- Timeline
  - 16 Kbit RAM: 2005
  - Niche products: 2008
  - Equivalent to CMOS density: 2011

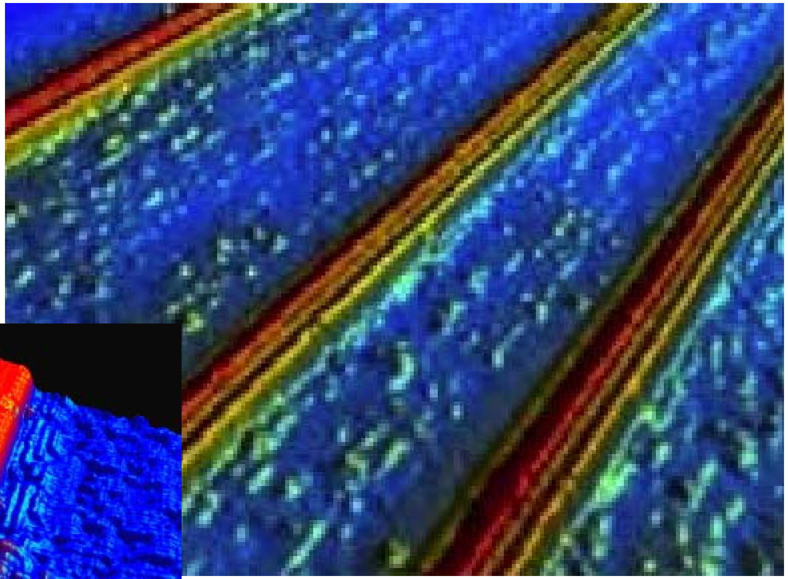
Carbon Nanotubes (NTs)

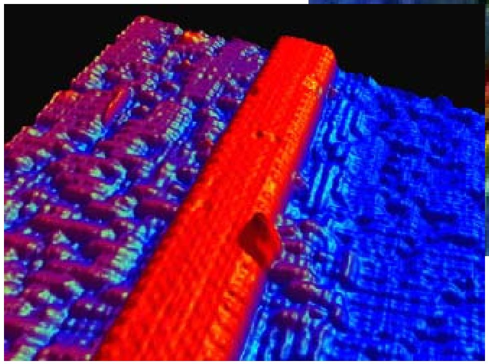
- Carbon sheet one atom thick, wrapped around like a tube
- Variant of the BuckyBall carbon molecule
- 1-5 nm wide, several mm long
- It is a single molecule
  - Extremely strong
  - Flexible
- Both a metal and semiconductor
  - Depends on lattice geometry
  - No way to synthesize pure batch of either yet



Silicon Nanowires (NWs)

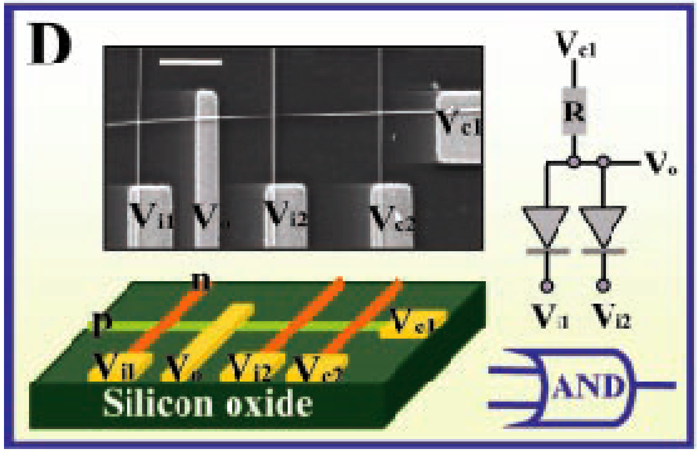
- Single-crystal of silicon
  - 6-20 nm diameter, 1-30 um long
- Fabricated in bulk by laser-assisted growth
- Ge, Au, GaP, GaN, InP NWs have also been made
- p-type and n-type NWs
  - Doped with phosphorus and boron
- Can be wire or semiconductor

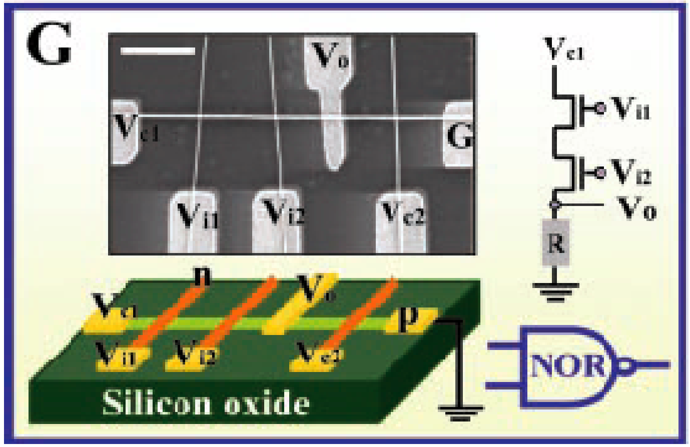




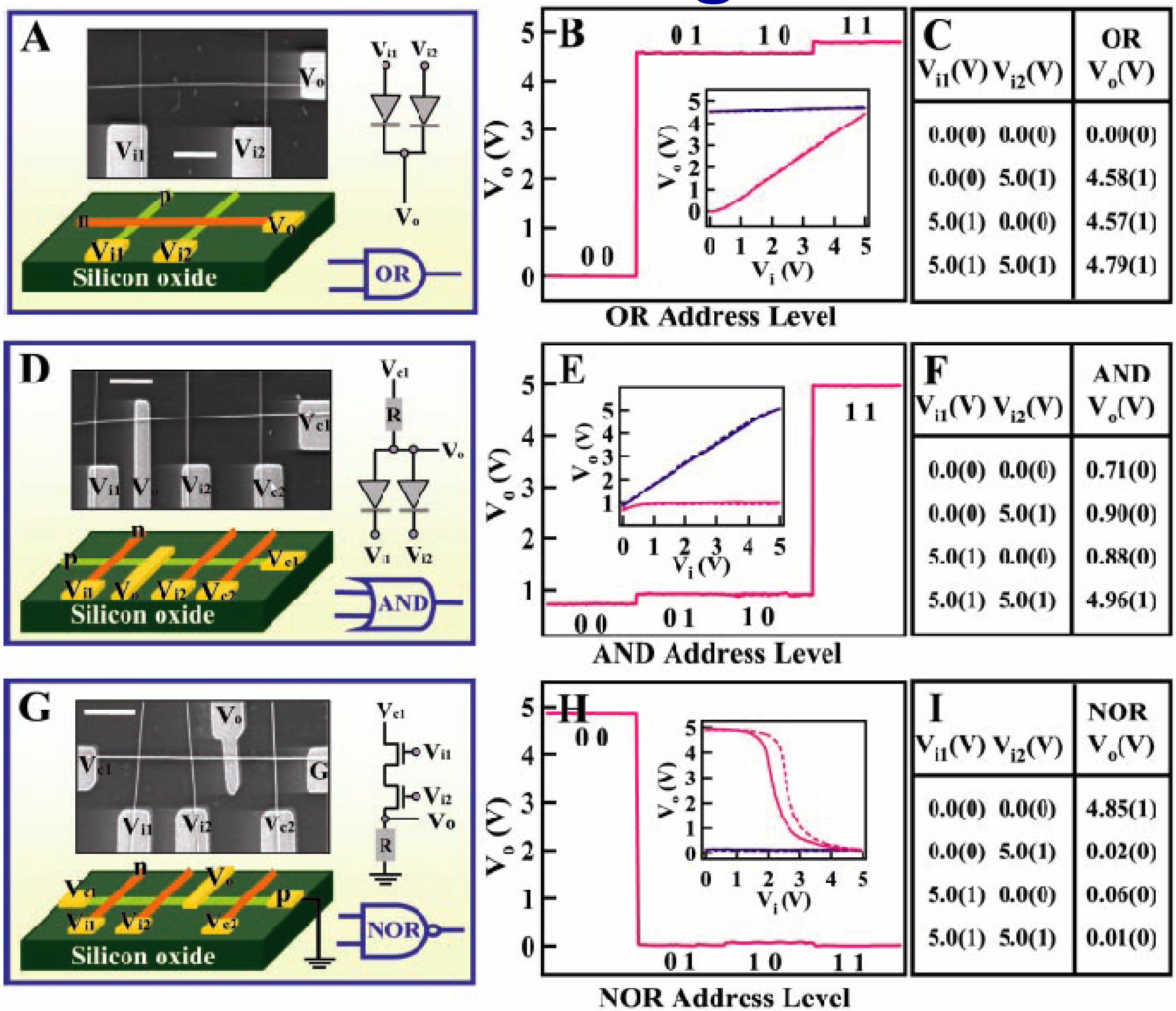
Transistors and Diodes

- Diode: cross two doped NWs
  - 90% yield
  - 1V up to 5V turn-on adjustable via oxidation
- FET: oxide between NWs
  - p: Si NW channel
  - n: GaN NW gate
  - Voltage gain = 5



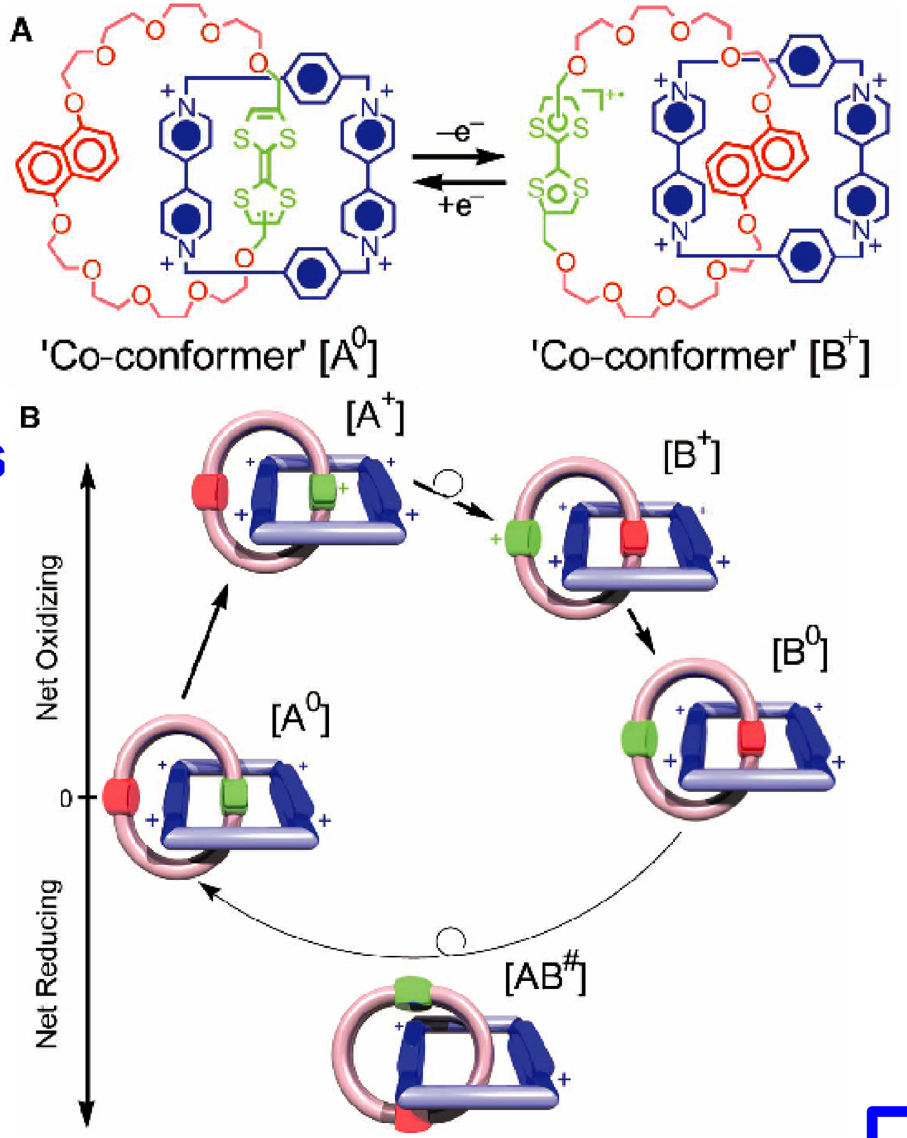


More Logic

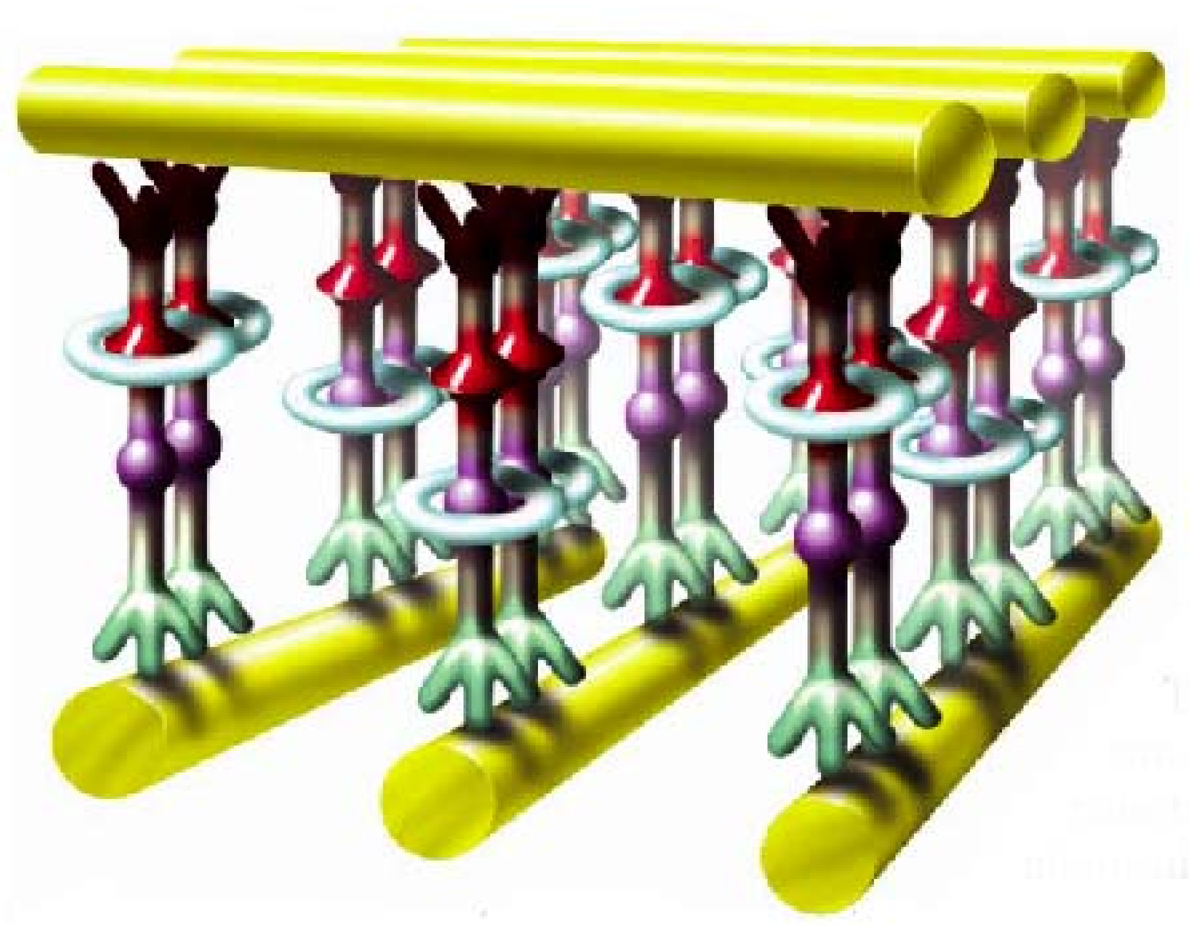

A
Silicon oxide
OR
B
OR Address Level
0 0
0 1
1 0
1 1
C
OR
V_{i1}(V) V_{i2}(V) V_o(V)
0.0(0) 0.0(0) 0.00(0)
0.0(0) 5.0(1) 4.58(1)
5.0(1) 0.0(0) 4.57(1)
5.0(1) 5.0(1) 4.79(1)
D
Silicon oxide
AND
E
AND Address Level
F
AND
V_{i1}(V) V_{i2}(V) V_o(V)
0.0(0) 0.0(0) 0.71(0)
0.0(0) 5.0(1) 0.90(0)
5.0(1) 0.0(0) 0.88(0)
5.0(1) 5.0(1) 4.96(1)
G
Silicon oxide
NOR
H
NOR Address Level
I
NOR
V_{i1}(V) V_{i2}(V) V_o(V)
0.0(0) 0.0(0) 4.85(1)
0.0(0) 5.0(1) 0.02(0)
5.0(1) 0.0(0) 0.06(0)
5.0(1) 5.0(1) 0.01(0)

Molecular Switches

- Organic molecules with two parts
- Interlocking rings
- Applying voltage oxidizes the molecules and shifts the rings
  - 2v opens, -2v closes
- Non-volatile programmable switch

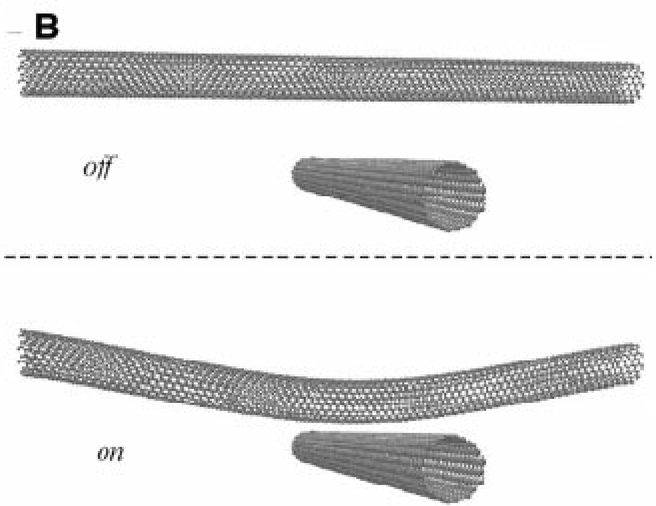


Molecular Switches



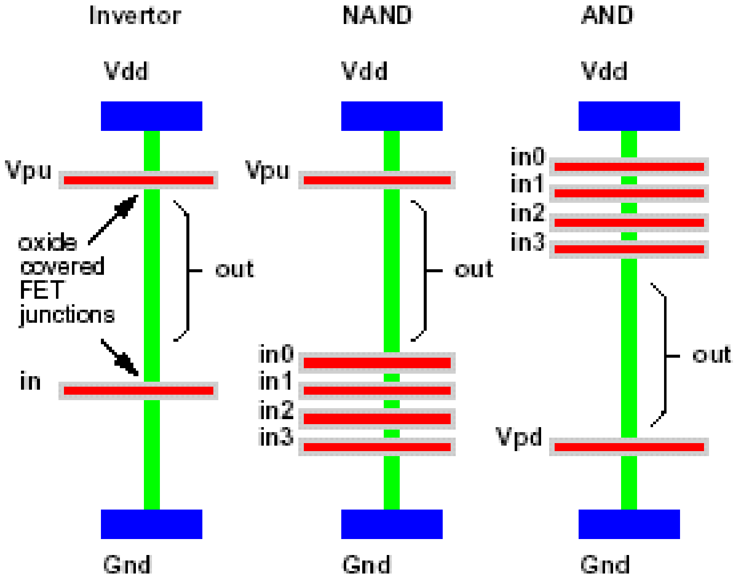
Mechanical Switches

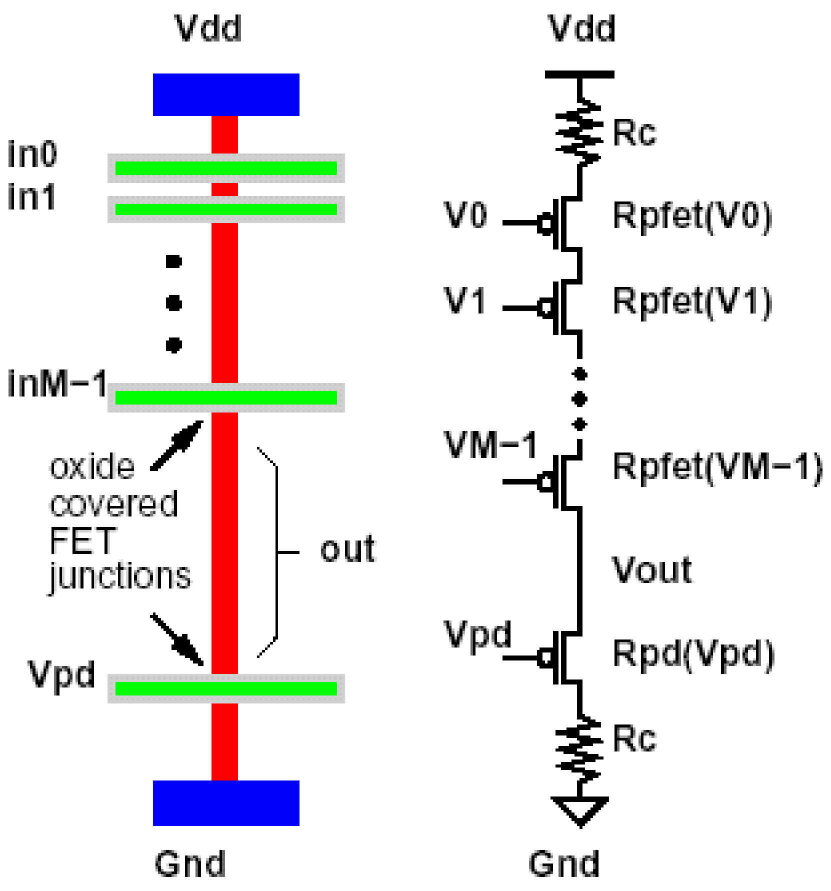
- NW/NT crossbar
- Programmable array of non-volatile bistable switches
  - Charge attracts wires to touch
  - Van der Waals force sticks them together
  - Opposite charge repels and opens the junction
- Diode array
  - Semiconducting lower half should make diodes at the junctions



Logic Gates

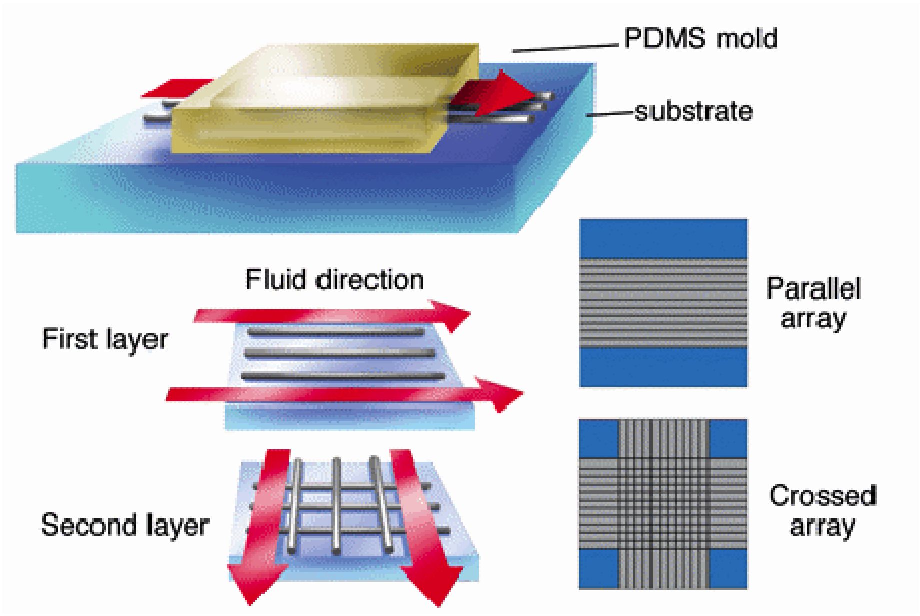
- **Build NOR from NW-FET crossbar arrays**
  - **Grow oxide over NW bottom wire to form FET**
  - **One time programmable**
  - **Static power dissipation**





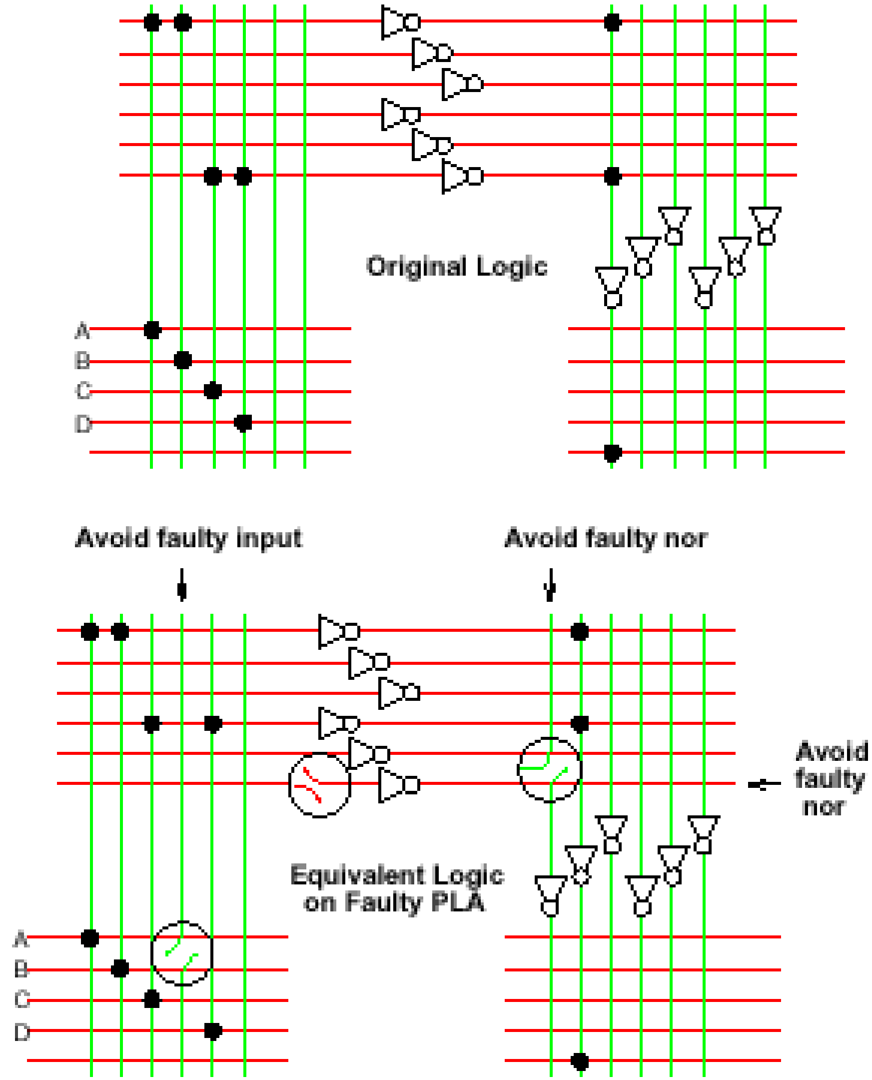
Bottom-Up Self-Assembly

- **We can't make nano-circuits *top-down***
  - **Lithography can't get to the nano scale**
- **Make them *bottom-up* with chemical self-assembly**
  - **Their own physical properties keep them in regular order, much like crystals do when they grow**
- **Fluid flow self-assembly**
  - **Flow rate and duration controls wire separatio**
  - **Higher flow, more alignment**
  - **Longer duration, more density**
  - **Crossbar generated in two passes**



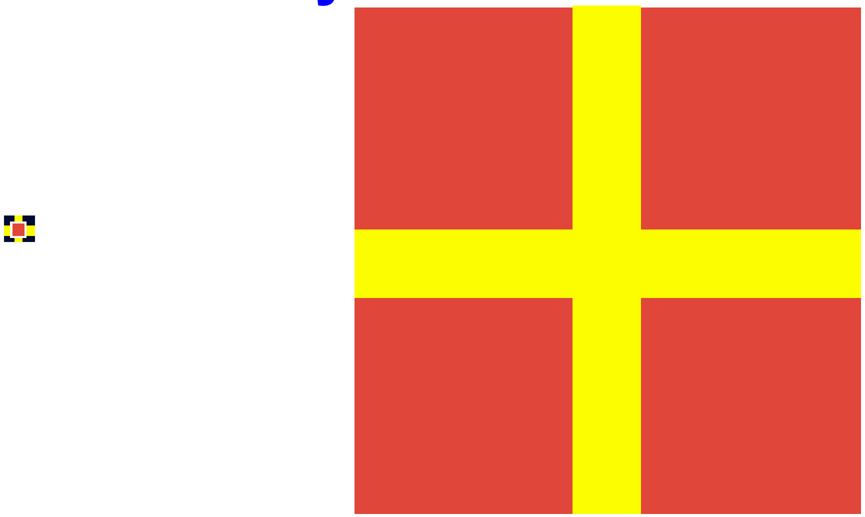
Implications

- **Defect tolerance is necessary**
  - Nature of chemical process is uncertain
  - Alignment imperfect at single molecule level
- **Programmable designs**
  - FPGA with lots of spares
  - Test and program around defects
- **Cheap fab, cheap gates**
  - Batch chemical process makes regular materials
  - Fabrication cost per device practically zero



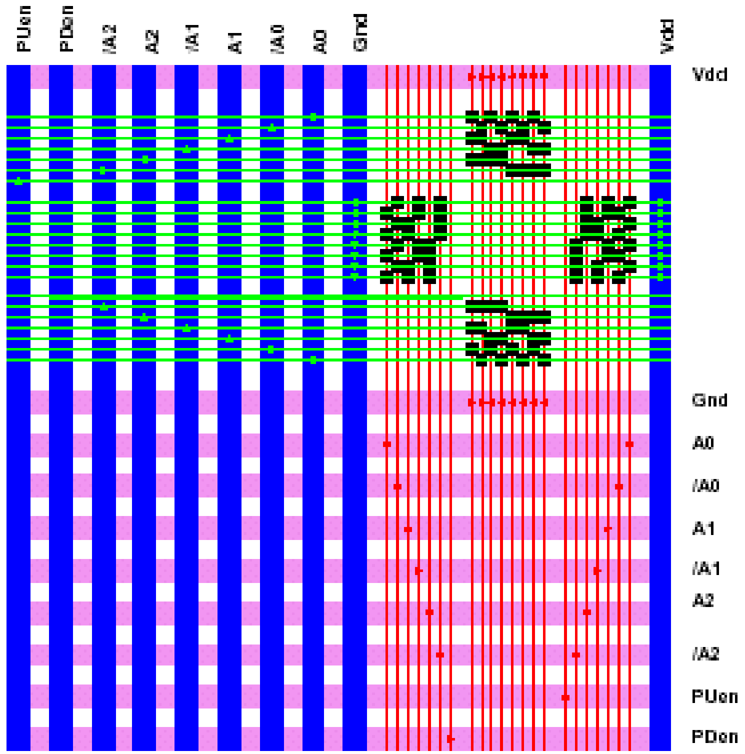
Crosspoint Density

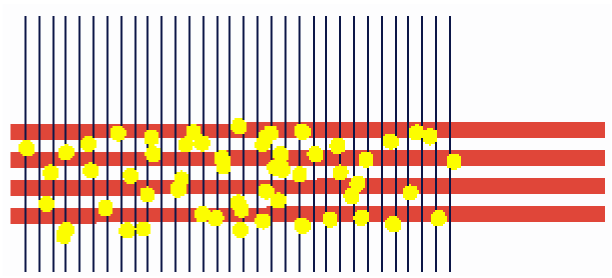
- CMOS crosspoint costs about 8 transistors
  - SRAM cell, big n-channel pass transistor
  - Far larger than minimum feature size
- NW or NT crosspoint fits iniside the wire crossover
- Area difference is 625x
- Makes NanoFPGAs very attractive



Interface to Microelectronics

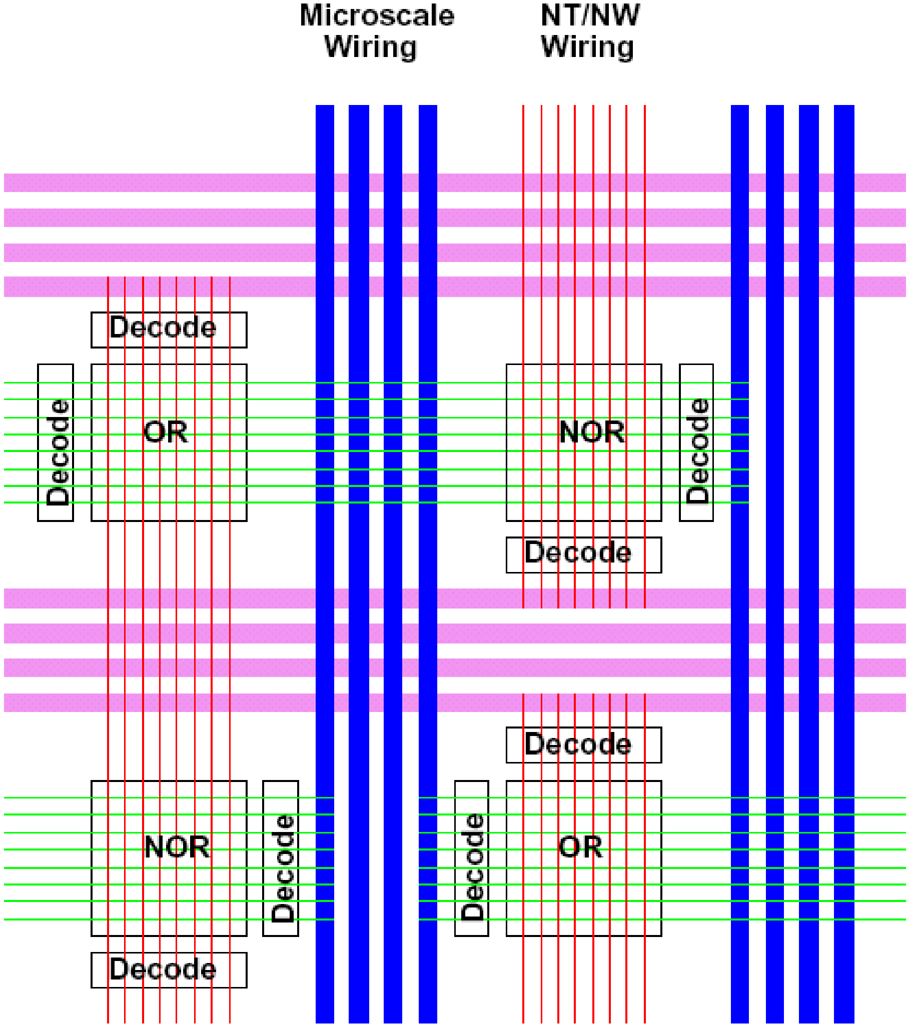
- Need to get out to the micro world
- Can't position any features at the nano scale
- Connect log(n) microwires to a set of N nanowires to make decoders



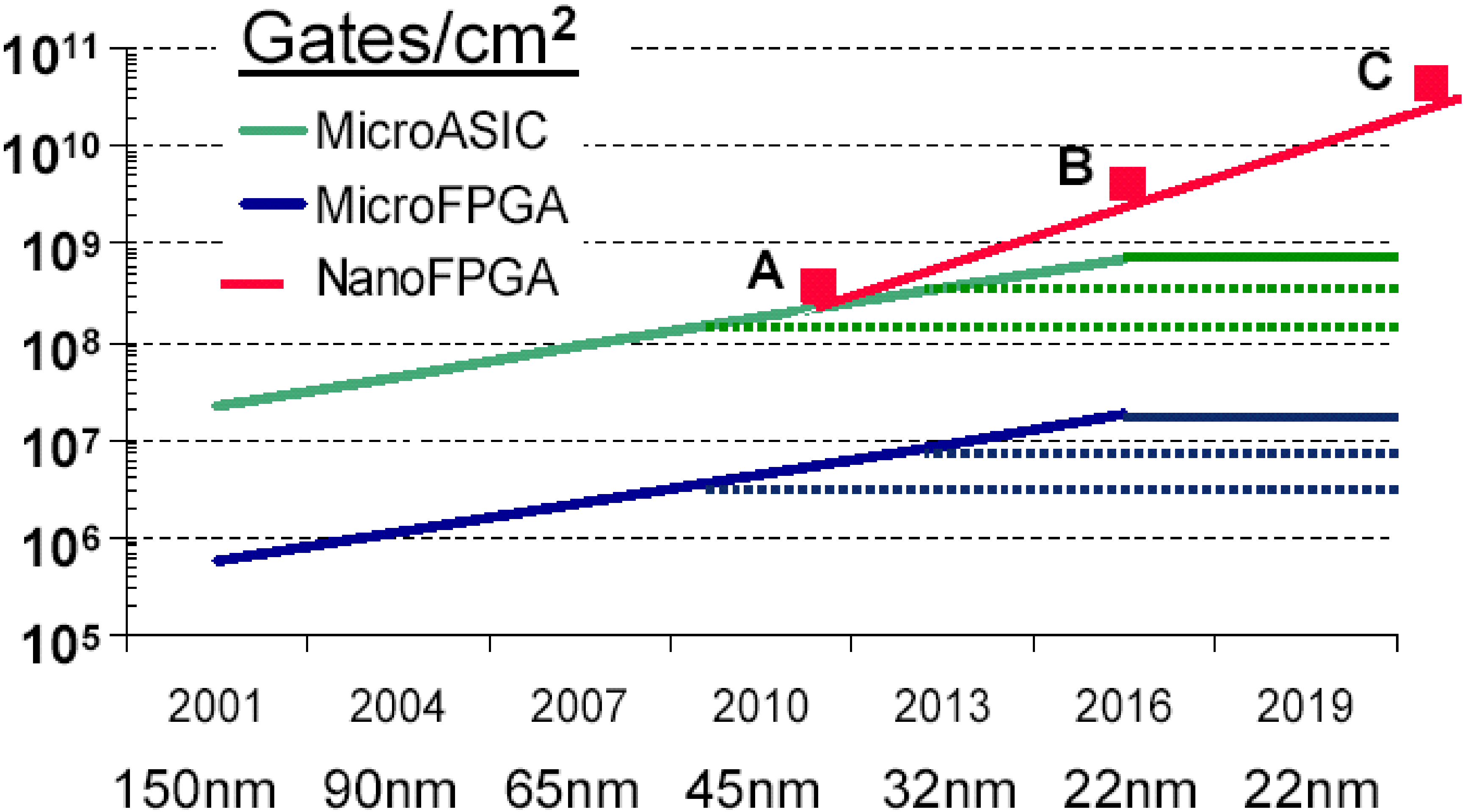


System Level Interconnect

- Programmable OR/NOR, NVRAM nanoarrays
- Interconnect arrays through
  - Extending NWs across multiple arrays
  - Through fully populated interconnect crossbars
  - NW-FET buffer/registers in-between when needed
- Interface to microwires with N-log(N) decoders



Logic Density Projections



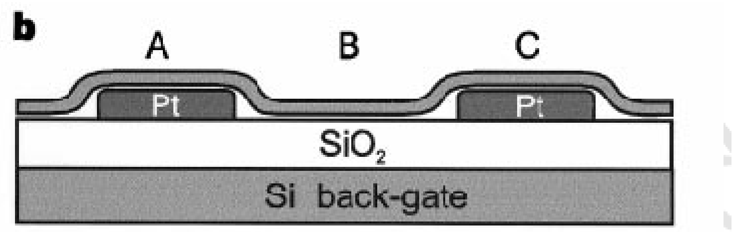
A: 50nm/20%/400M, B: 25nm/50%/4B, C: 10nm/80%/40B

No free lunch™

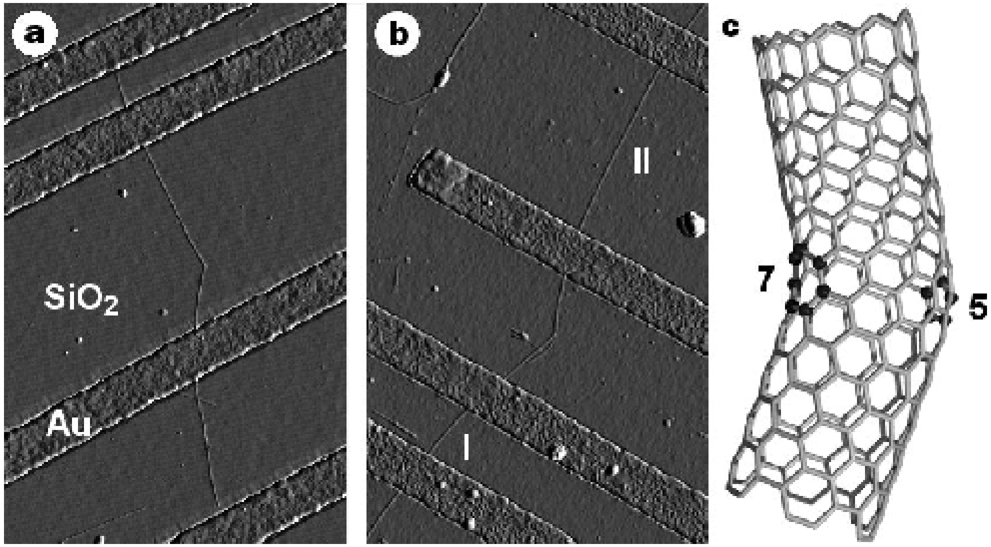
- Power:
  - 10^{11} devices/cm^2 * 1 nanowatt/device = 100 watts/cm^2
  - That's a lot of juice!
- Signal integrity/crosstalk not addressed
- Quantum effects?
  - Electrons can act like waves too…
- Reliability
  - Creeping defects after fab?
  - Cosmic ray damage or hardness?
- Programming effort
  - Work around defects to get a defect-free generic array
  - OR place & route a billion gates!

What do we get for Gigagates?

- **Macro-scale computing**
  - **Massive massive massive parallel machines**
  - **Simulations (ASCI red/white/blue)**
  - **Weather**
- **Micro-scale computing**
  - **100 MIPS in 10 sq. um.**
  - **Powered by ambient light**
  - **Biosensors**



b
A
B
C
Pt
Pt
SiO2
Si back-gate


a
SiO2
Au
b
II
I
c
7
5