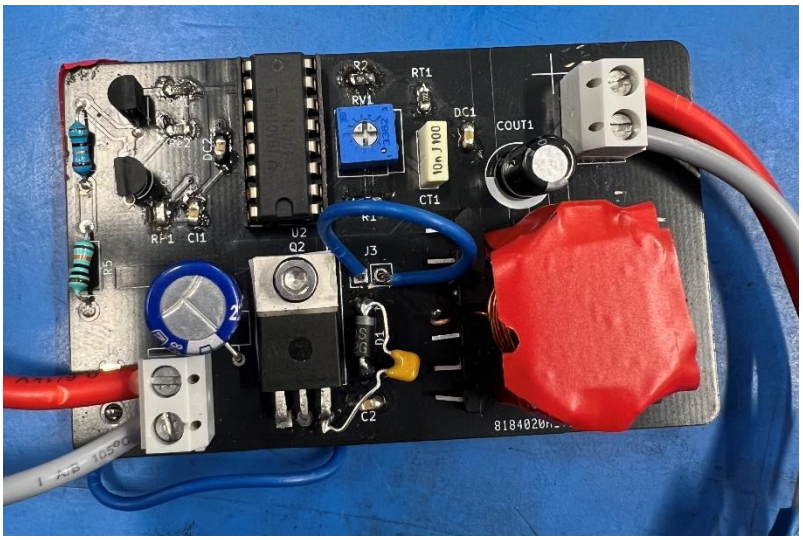
ENEL372
Power and Analogue Electronics



Solar Car Report

Group 6
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Contents

Introduction

This report will cover the design and performance of a DC-DC converter in a solar car application. From this, recommendations will be made for further improvements.

The model solar car is made from an aluminium chassis. On the chassis are a 10-Watt solar panel, DC motor, servo, gearbox, and battery. The battery is used for operating the servo motor which allows for steering of the car. The solar panel, DC motor, and gearbox drive the car.

Solar panels produce varying power depending on the output voltage and current required. Under operation, the DC motor's current requirement changes depending on the torque requirement. On startup, DC motors tend to draw a large amount of current. This is usually called the starting current. This large current draw occurs because the back EMF is zero due to the motor not being started yet. Once the motor is running, back EMF begins to oppose the voltage applied. This leads to a net voltage reduction, leading to a proportional current reduction. Eventually the current stabilises as a function of the load. The load may increase during operation due to mechanical reasons such as friction or a weight being placed on the solar car.

Due to the constant power assumption, the only way the panel can produce enough current for the load requirement is by reducing the output voltage. Reducing the output voltage moves the panel's operating point in the voltage/current curve. This means it will no longer produce the maximum power for all supply voltages. Introducing a DC-DC converter allows for the panel to operate at maximum power by converting to a voltage and current that the DC motor requires.

The following design constraints were imposed:

- DC-DC converter to be a buck converter
- Control chip must be the TL494
- N-channel MOSFET IPP034N03L
- Diode SB240S
- Inductor core is of type RM8
- Maximum capacitance in the buck circuit is 350 μF

A buck converter is a type of DC-DC converter that steps down a higher input voltage to a lower output voltage while increasing the current to maintain power balance. It does this by switching and using an inductor as an energy source and store. Capacitors are used to smooth voltage ripple. Buck converters are often used due to their high efficiency (typically around 90%).

Circuit Design

Design Description

The design of the buck is comprised of four main sections: PWM Generation, Power Booster, Control, and Buck. The PWM signal is used to switch the buck. The Power Booster takes the PWM signal and increases the current to switch the MOSFET on the buck. The Controller keeps the solar panel at the correct voltage by changing the duty cycle of the PWM signal.

The converter was designed on KiCAD and made into a PCB. The PCB was 40 mm by 80 mm. Ground and power planes were included to reduce noise. The full design of the PCB is in Appendix B.

PWM Generation

This will talk about the TL494 and how it generates a PWM signal.

The TL494 generates various frequencies of PWM based on the values of two components labelled Rt and Ct. We designed for a 50 kHz switching frequency and checked the datasheet for appropriate values. 50kHz was chosen was to find a good balance to smooth the motor current and low enough to avoid the power losses that occurred every time the transistors in the motor drive circuit turned on or off. The high value also let us choose reasonable inductor and capacitor values for the buck circuit. The values of RT and CT can be found in Figure 1.

$$f = \frac{1.1}{R_T C_T}$$

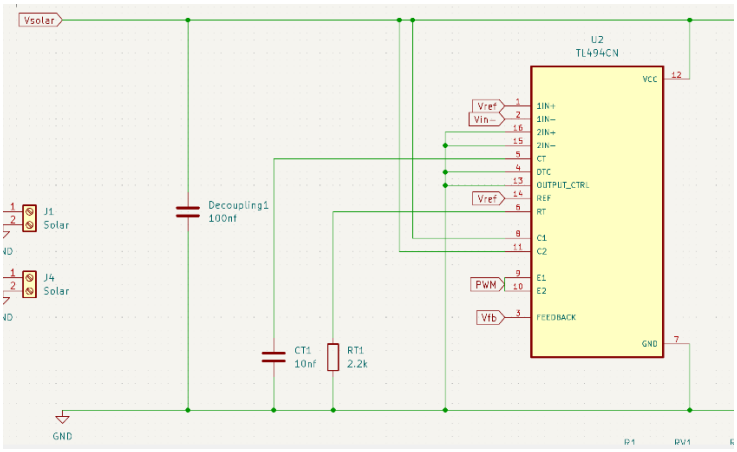


Figure 1: The TL494 circuit

Power Booster

The Power Boost circuit takes an PWM input from the IC and boosts the current such that it can switch the MOSFET. The schematic is shown in Figure 2.

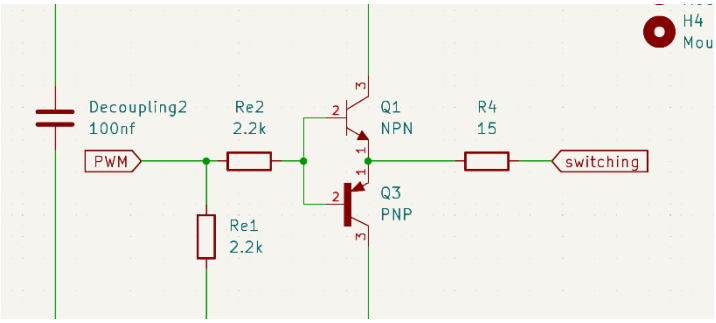


Figure 2: The push-pull amplifier circuit

Re1 and Re2 were determined to be 2.2 kΩ. This limits the current through the IC and the BJT base current for proper operation. These were maximised to reduce the current in the IC while still providing enough current to the BJTs to switch. The NPN amplifies the turning on voltage and the PNP amplifies the turning off of the MOSFET. R4 was determined to be 15 Ω. This was to limit the current to the gate of the MOSFET providing proper operation.

Control Design

It was determined that the solar panel max power was at 16-17 V. On the datasheet it states that the maximum efficiency was at 15 V. Making the setpoint adjustable was important for different use cases and environments.

The controller is an integrator with the ability to have proportional control added in. It uses the opamp in the TL494 IC and is an integrating opamp circuit. This is shown in Figure 3.

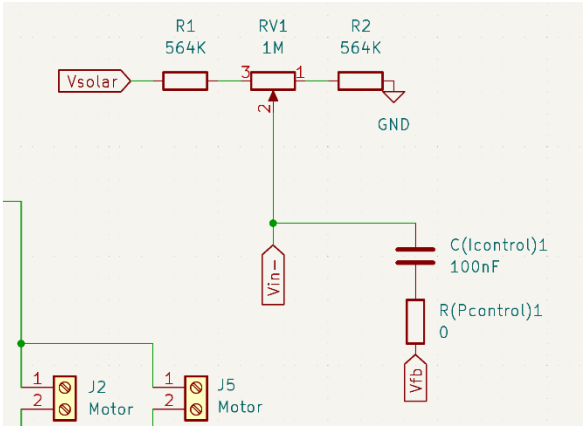


Figure 3: The integrator feedback circuit

The controller is used to set the voltage of the panel and keep it at a given setpoint. The setpoint can be changed with the potentiometer but is designed around 15V. The panel voltage is reduced with a voltage divider such that the voltage to V- of the opamp is 5V for the given setpoint. This was due to the TL494 producing a clean 5V reference signal reducing noise in the control circuit. This 5V is V+ and Vfb is the Vout of the opamp. The control effort is done on the duty cycle of the PWM going to the switching of the buck. The duty cycle directly controls the panel output current. Changing the current from the panel changes the voltage of the panel and hence achieves setpoint.

The Ki gain was calculated with equation below.

$$K_i = \frac{1}{\tau}, \qquad \tau = RC$$

The time constant was 100ms from this R is 330 kΩ and C is 100 nF. The resistors were chosen to minimise the value of the capacitor.

Buck Design

The key components involved with the buck converter contain input and output capacitors, a power inductor, an N-type MOSFET and a resistor R5 across the MOSFET. Certain characteristics and values for these components were calculated and considered to produce a fully functioning buck converter.

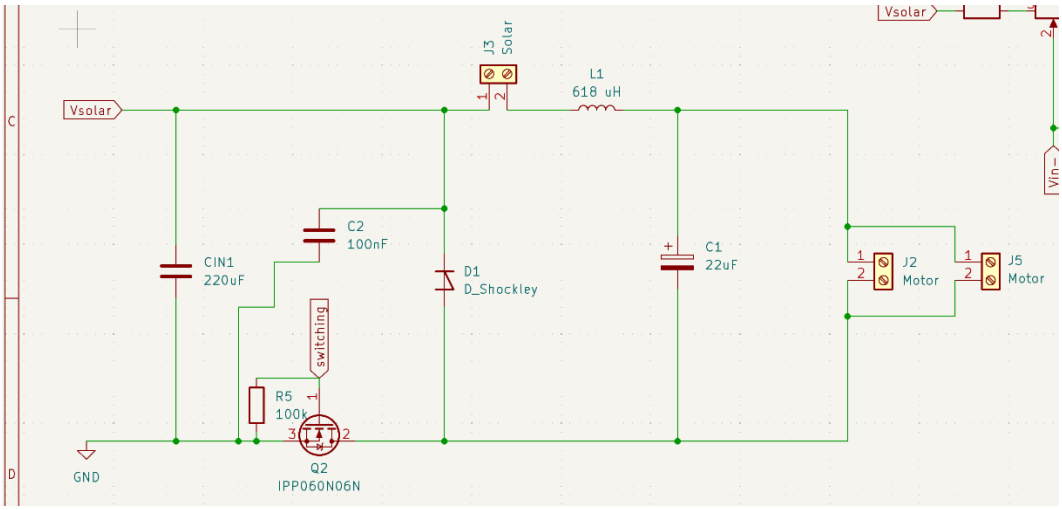


Figure 4: Buck converter circuit

The inductor current becomes discontinuous if any part of the inductor current waveform drops to zero. This occurs when the lower half of the inductor current ripple amplitude becomes larger than the average output current. Therefore, to design for continuous inductor current, the average output current should be greater than half of the inductor current ripple. This gives the equation for continuous inductor current as seen below.

$$I_o > \frac{\Delta i_L}{2}$$

Using this equation and considering the change of inductor current when the buck converter is on, a value for the inductor can be calculated to achieve the continuous inductor current criterium. Rather than having the inductance equation depend on output voltage, the transfer function for the buck converter can be used to make the inductance equation depend on the input voltage. This is more desirable because the output voltage will be changing under various loading conditions but the input voltage from the solar panel will remain constant and at maximum efficiency. These derivations give the final inductance equation which will be used to calculate the inductance size.

$$L > \frac{V_s D(1-D)}{2 f_s I_o}$$

The current inductor waveform must be continuous for all cases for the solar car. The worst-case duty cycle of 0.5 is considered as well as a worst-case output current value upon startup gives this equation.

$$L > \frac{V_s}{8 f_s I_o}$$

The values used to derive the inductor value were 15 V for the supply voltage, 50 kHz for the switching frequency, and a worst case 2.5 A average output current. The minimum inductor value for these values was to be no less than 15 μH. When the inductor was designed, increasing the minimum value meant that there would be no opportunity for the inductor current to become discontinuous. Also, this would minimize any current ripple running through the inductor.

For the power inductor not to saturate there needs to be a sufficient airgap between the two halves of the inductor core. The equations used are referenced in Appendix C below. The turns product ratio was calculated based off the 1 mH inductance, a field strength of 300 mT and a max current 2.53 A. Then using the area of the inductor core to divide the turns product ratio gave the minimum number of turns which ended up being 134. However, this number of turns was not able to fit in the inductor core resulting in 67 windings and an inductor value of 618 μH. The reluctance was then calculated to give an airgap of 279 um between the two halves of the core.

The input capacitor *Cin1* in the buck converters purpose is to make sure a relatively constant current is drawn from the solar panel. The solar panel has the characteristic where if too much current is drawn, the voltage of the solar panel drops, and it is no longer working at maximum power. To get a constant voltage, the current must remain constant too. Assuming there is no output voltage ripple and that the buck converter is acting at 100% efficiency, it can be assumed that input and output current are equal. With the worst-case scenario duty cycle equalling to 0.5, the equation below can be used to calculate the input capacitance.

$$C_{in} > \frac{I_o}{4 f_s \Delta V_S}$$

Using the worst-case average output current of 2.5 A, a switching frequency of 50 kHz and a voltage ripple of 2% results in *Cin1* having to be larger than 41.7 μF. However, in the design *Cin1* was increased significantly to 220uF to reduce input ripple. The remaining allowable capacitance was then used on the output capacitor *C1*. There is current flowing through *C1* there will be an associated voltage variation which is the voltage ripple. This is derived from the change in inductor current when the switch from this equation for output capacitance *C1*.

$$C_{out} > V_o \frac{1 - D}{8 L f^2{}_s \Delta V_o}$$

Using the worst-case duty cycle of 0.5 and a worst-case output of 7 volts, this resulted in a minimum value of the output capacitance *C1*. Values used for the inductor were 618uH, 50kHz for the switching frequency and designing for an output voltage ripple of 2% results in *C1* being no less than 14.2uF. Again, by going over this value this ensures the output voltage ripple will be reduced even further.

C2 was added in as the diode experienced high di/dt which causes inductive coupling.

N-channel MOFSFETs were chosen for the switching components because they switch quickly, making them a desirable choice for the buck converter. The resistor *R5* is a 100 kΩ resistor that is connected across the MOSFET's Gate-Source. This is to reduce the MOSFET's parasitic Gate-Source capacitance. *R5* acts as a safety for the circuit encase it is short circuited, this will ensure that the parasitic capacitance effect of the MOSFET remains discharged whenever there is no PWM signal present.

Analysis

PCB

The main problems with the PCB arose due to a general lack of capacitors.

C2 on the PCB diagram found in Appendix B did not function as intended. This was due to a design error that resulted in one end of the resistor being connected to V_{CC} and not the cathode of the diode D1 as it should have been. Another resistor was added in that connected the cathode to ground, for which the shortest loop area was at the MOSFET source.

In the power boost section of the PCB, the high frequency switching component experiences a high change in current with respect to time (di/dt). To reduce the noise, a decoupling capacitor was added across the terminals of the transistors.

The PCB worked as intended in all other areas.

PWM Generation

The PWM signal produced from the TL494 is shown in Figure 5.

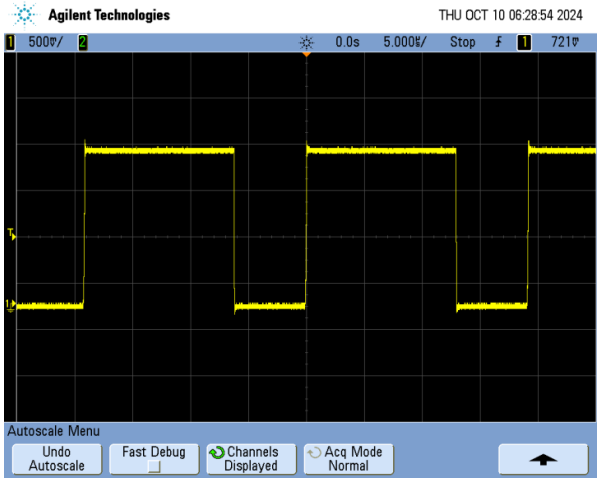


Figure 5: PWM Signal Generation using TL494

The PWM signal generated a 50kHz signal as expected, with very little noise. Initial tests showed that when the motor load was manually increased, the feedback altered the duty cycle accordingly.

Power Boost

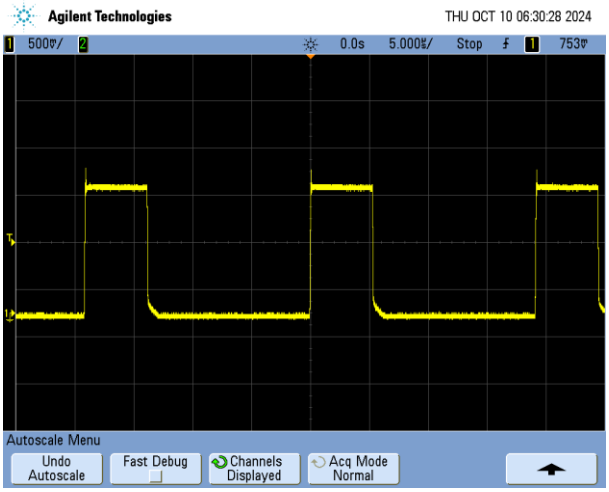


Figure 6: PWM signal after leaving the push-pull amplifier

The power boost circuit work as intended. Taking the PWM waveform from the IC and boosting the current without changing the waveform. There is a small spike in voltage on the rise due to the large loop area to and from the MOSFET. This causes inductive coupling from high di/dt on the rise. There is also small distortion on the fall due to forgetting the diode, so the current on the way back has to drop through two resistors instead of one.

Buck

The inductor current and V_{GS} is shown in Figure 7. The Gate-Source voltage resembles the simulated LTspice data found in Appendix D.

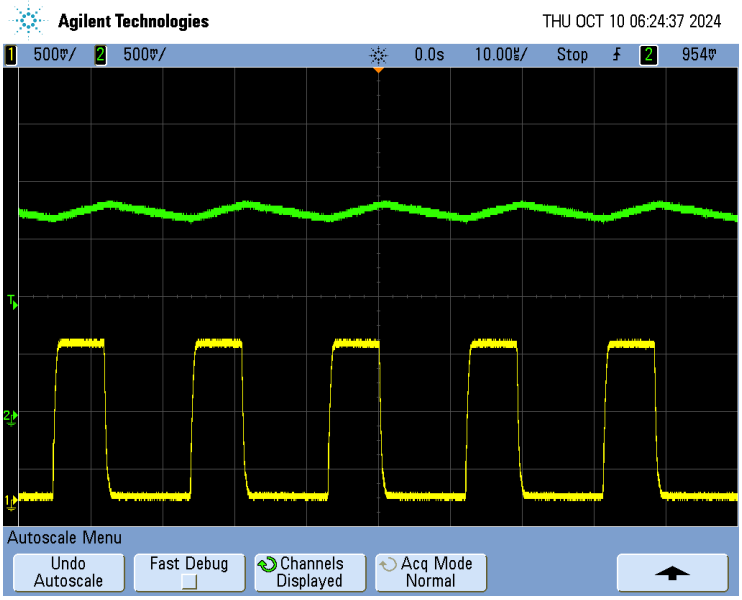


Figure 7: Inductor current and MOSFET Gate-Source voltage

The inductor current waveform of the buck converted behaved as continuous current. The current ripple of the inductor is linear. Having a linear inductor current waveform is advantageous because the change

in gain to duty cycle will also be linear. This ensures the duty cycle curve does not have to change for different loads. This leads to less losses which drastically increases the efficiency of the buck converter. It is clear to see that the inductor does reach saturation as this would produce non-linear current ripple.

The V_{DS} of the MOSFET is shown in Figure 8.

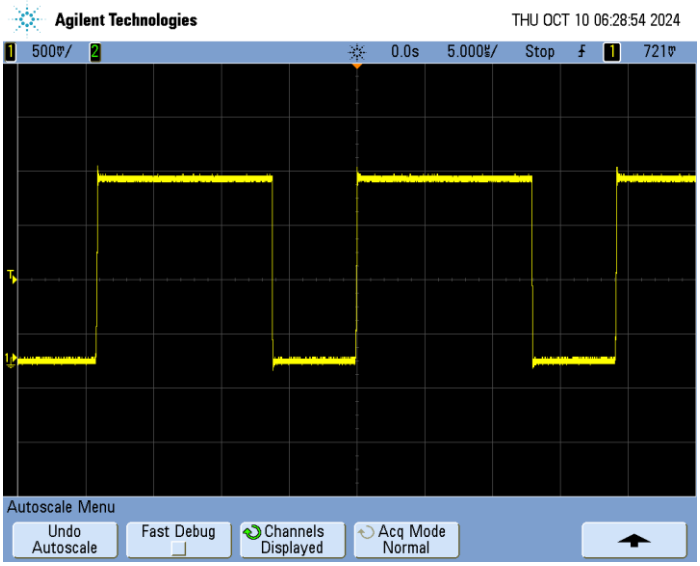


Figure 8: MOSFET Drain-Source voltage

The drain-source voltage showed a clean PWM signal complement of the V_{GS}. This shows that the power boost circuit is working as intended. This also resembled the corresponding simulated voltage plot in Appendix D which was obtained from LTspice.

The output voltage is shown in Figure 9.

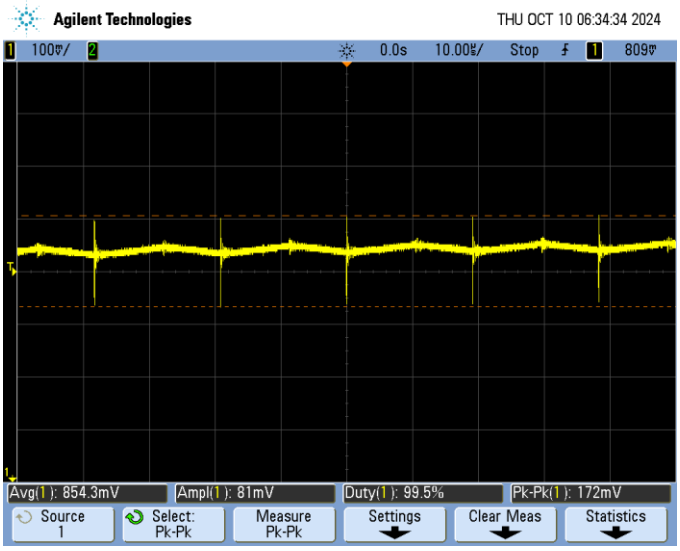


Figure 9: Output voltage across motor terminals

The voltage ripple is similar to the inductor current waveform where the longer gradual curve of the waveform mirrors when the inductor is ramping up and the sharp rise in the output voltage resembles

as the inductor ramps down. The spike in voltage is due to noise coming from the motor load. In designing the motor, it was assumed a resistive load but there is also inductive load in the motor.

Discussion

Overall, the circuit produced output voltage and current that could drive the DC motor smoothly. The circuit controlled the voltage of the panel to keep it in a peak power level, and the PI controller enabled the circuit to respond to various load cases including the high torque case on startup and variances during steady-state operation due to mechanical load changes.

Further improvements include:

An improvement to the current design is to implement a transistor in place of the diode D1 that limits the direction of current. This would result in a type of synchronous circuit where, instead of dropping voltage across the diode, the circuit would simply turn off, eliminating power losses across this component. The timings for this transistor would need to be in sync with the PWM signal timings.

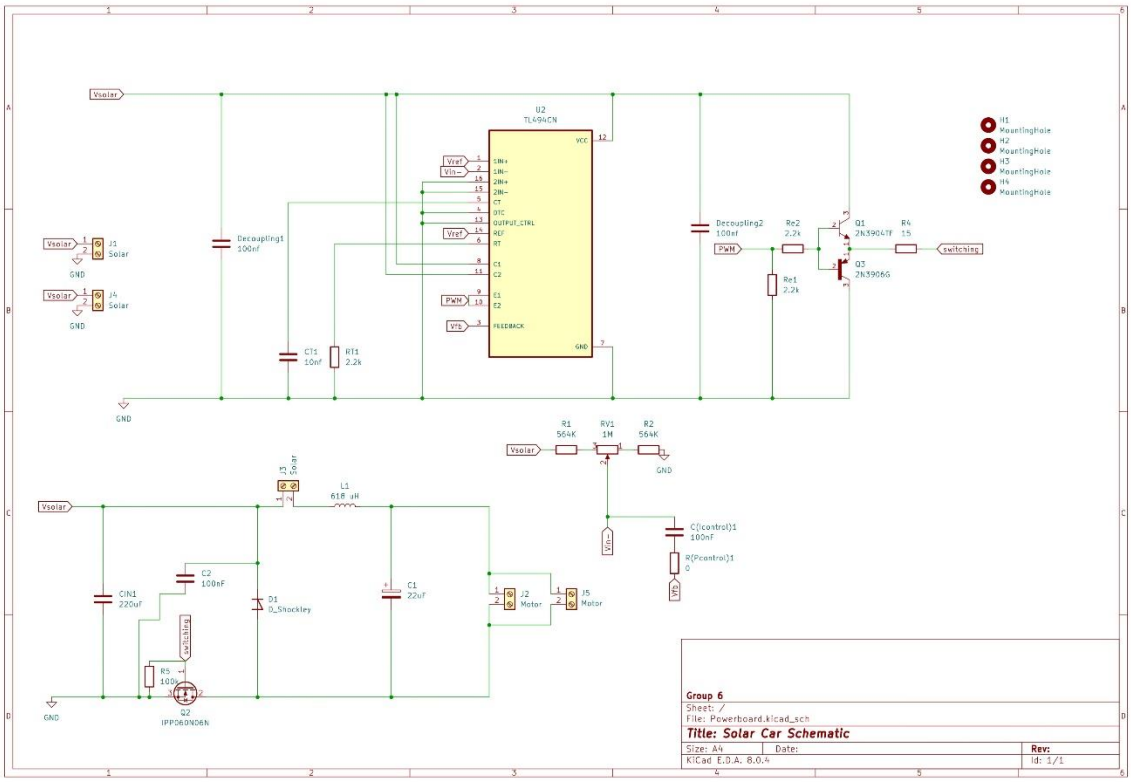
Another improvement is to place a diode in parallel across Re2. Resistors Re1 and Re2 had the same value, and the idea was that the diode would ensure that the voltage drop would be the same for each direction of current. This would ultimately allow for slight faster switching. However, this diode was omitted in the schematic of the ordered PCB due to it being forgotten about. This results in the switching on taking slightly longer than the switch off. The overall performance impact is minimal.

Another improvement is to add a resistor into the control circuit to create a proportional-integral (PI) controller. This would have the effect of making the current reach the setpoint quicker. In combination with the integral control, this would provide a circuit that reaches the setpoint quickly and eliminates the steady-state error by summing the errors over time.

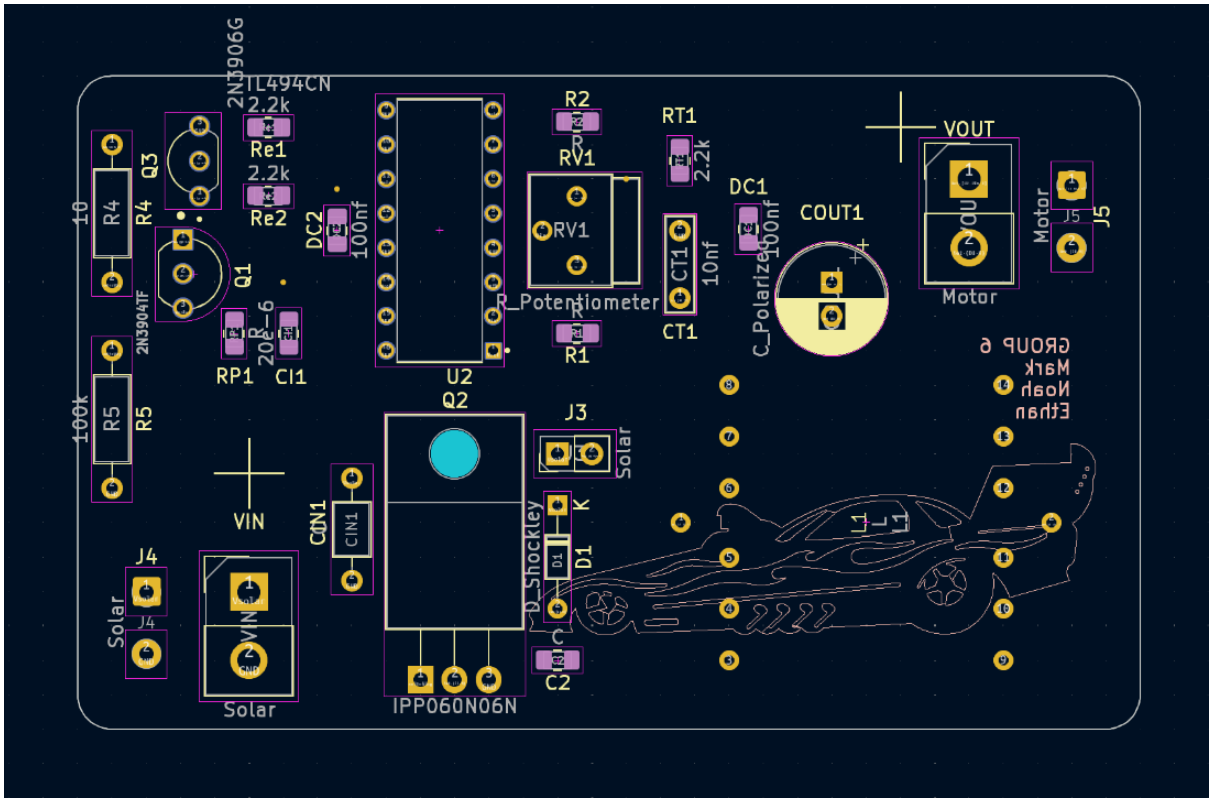
Initially testing various waveforms resulted in improvements to be made before the final demonstration. The PWM signal measured from the gate to source was corrupted by noise as there was a curve in the PWM wave with some unwanted spikes in the waveform. Although this did not affect the switching of the buck converter, the noisy PWM signal that was noisy propagated into other waveforms. Originally the PCB board design had ground and power planes, which reduced noise by reducing loop areas. This can be seen in *Appendix B* below. However, the noise spikes and curviness of the PWM signal were reduces when a decoupling capacitor was added across the diode.

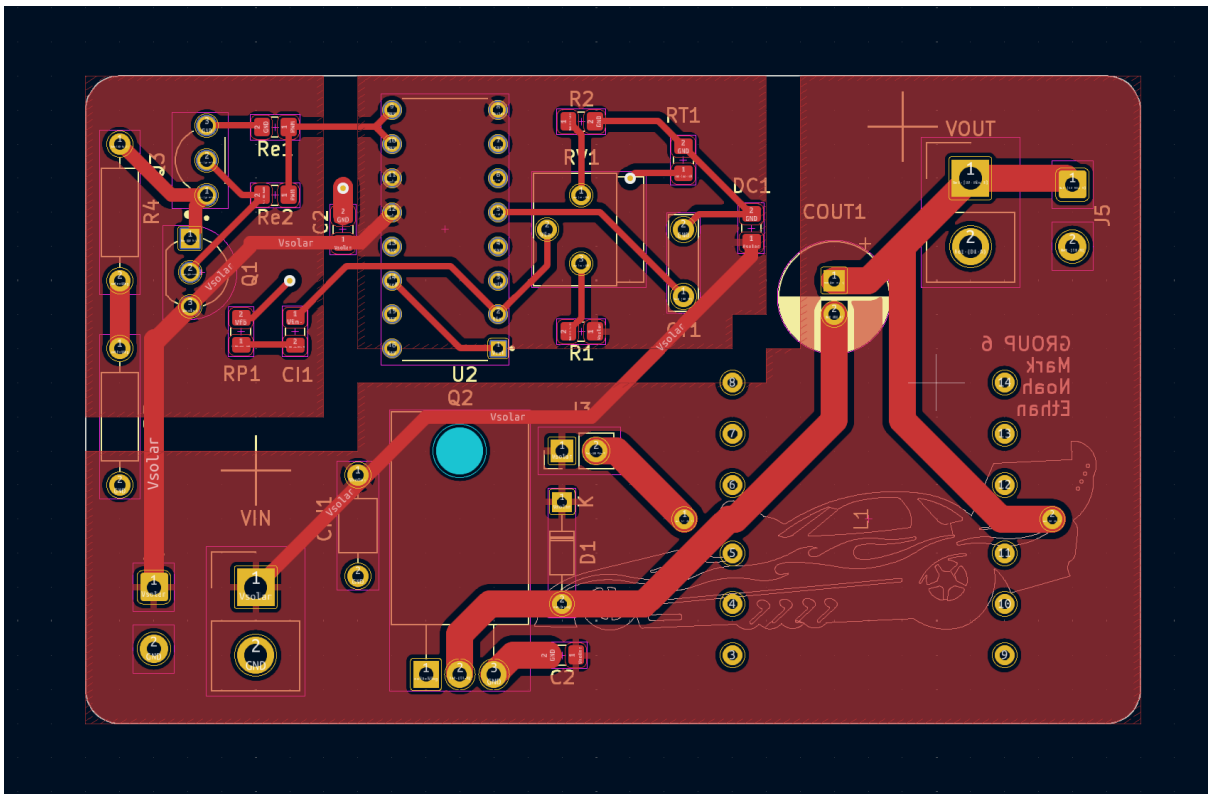
Appendix

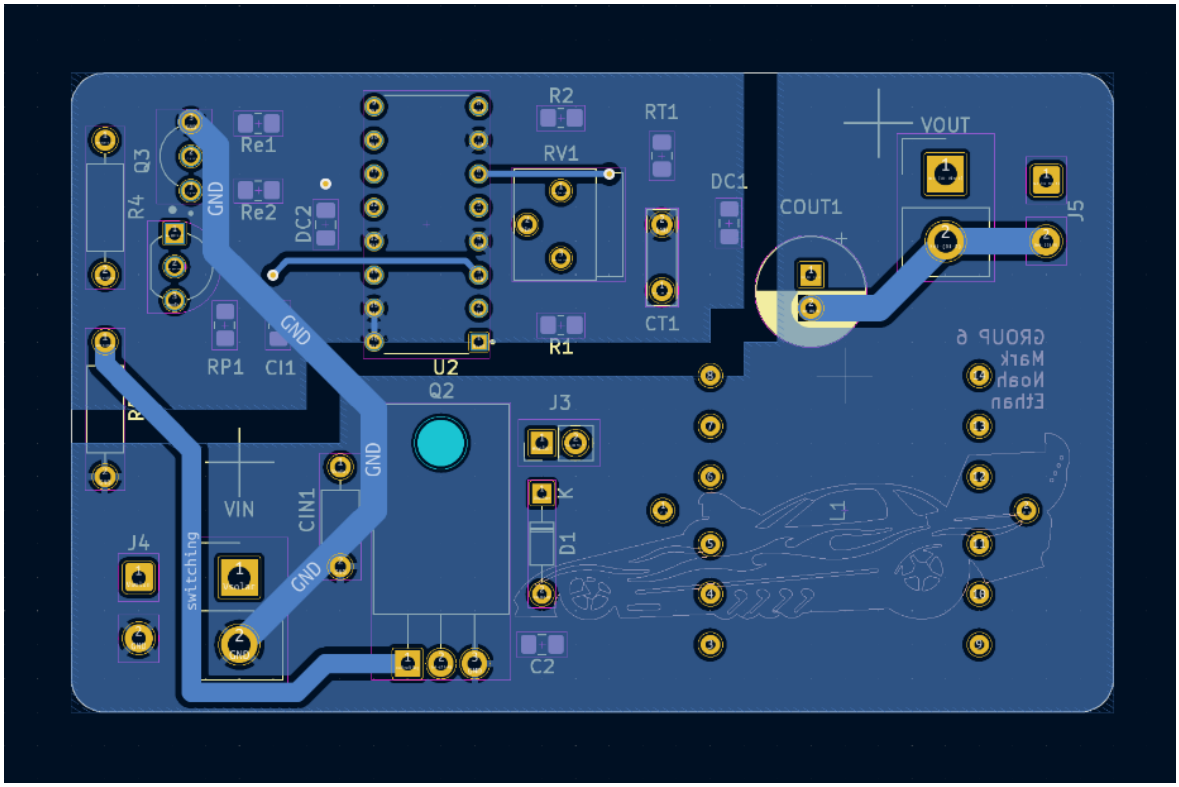
Appendix A: Schematic



Appendix B: PCB Design



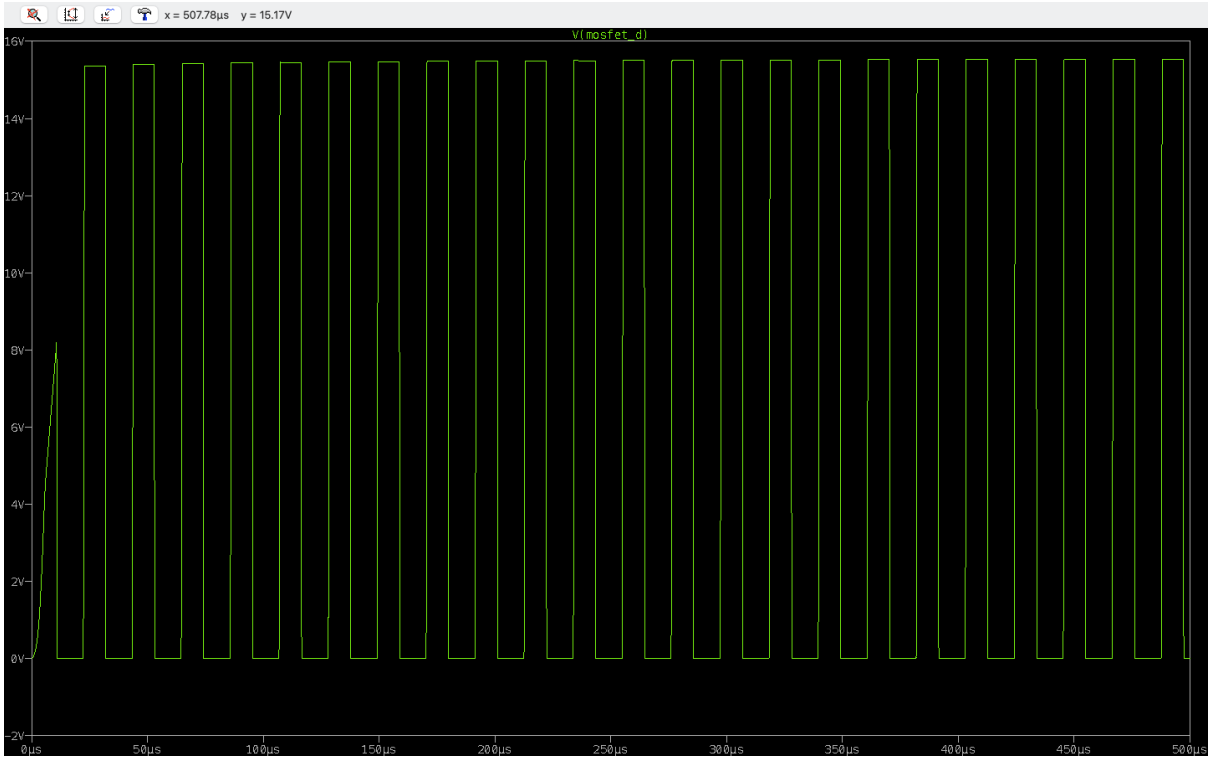



R2
RT1
VOUT
Re1
RV1
DC1
COUT1
J5
Q3
R4
GND
Re2
DC2
CT1
RP1
CI1
R1
U2
Q2
J3
GROUP 6
Mark
Noah
Ethan
VIN
CIN1
GND
J4
switching
D1
L1
C2

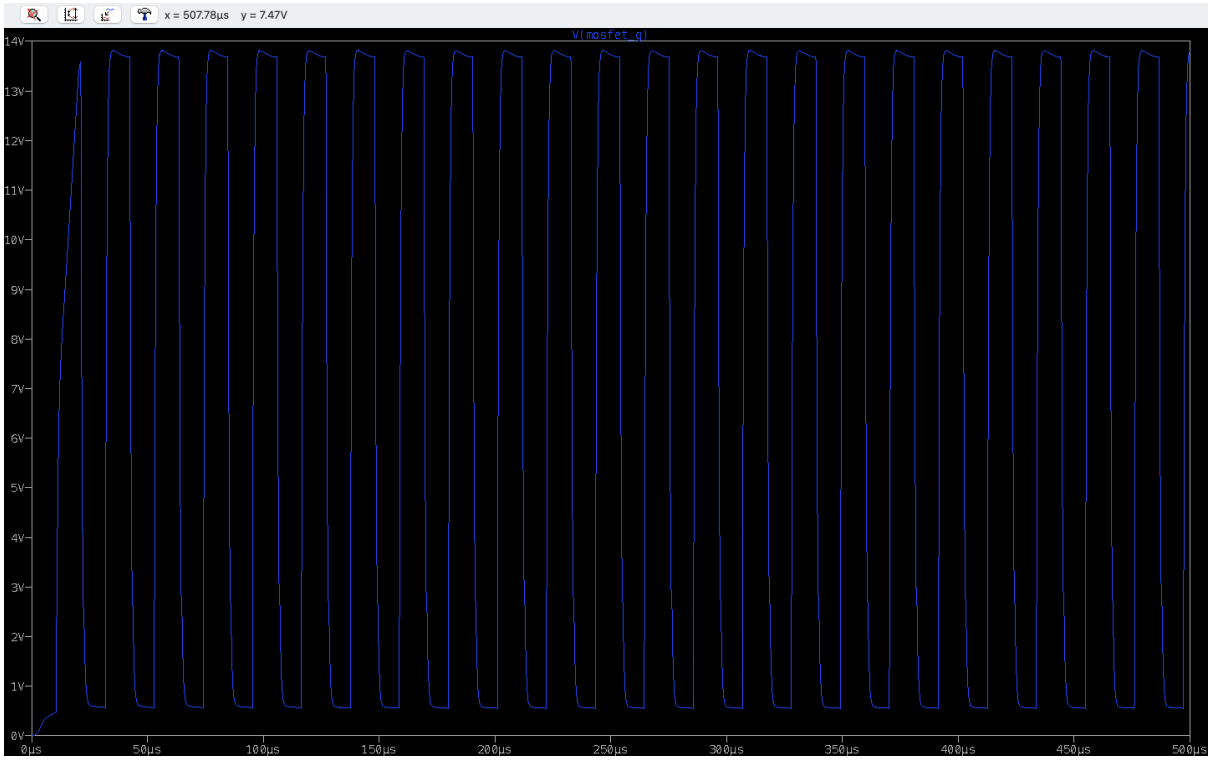
Appendix C: Equations

Inductor calculation	$L > \frac{V_s}{8 f_s I_o}$
Output capacitance	$C_{out} > \frac{V_o}{\Delta V_o} \frac{1 - D}{8 L f_s^2}$
Input capacitance	$C_{in} > \frac{I_o}{4 F_s \Delta V_s}$
Time constant and PI control	$\tau = RC$
Air gap calculations	$NA_{min} = \frac{L i_{max}}{B_{max}}$ $N_{min} = \frac{NA_{min}}{A_{core}} \rightarrow$ rounded up to the nearest integer $R = \frac{N^2}{L}$ $l_{gap} = \frac{R \mu_0 A}{2}$

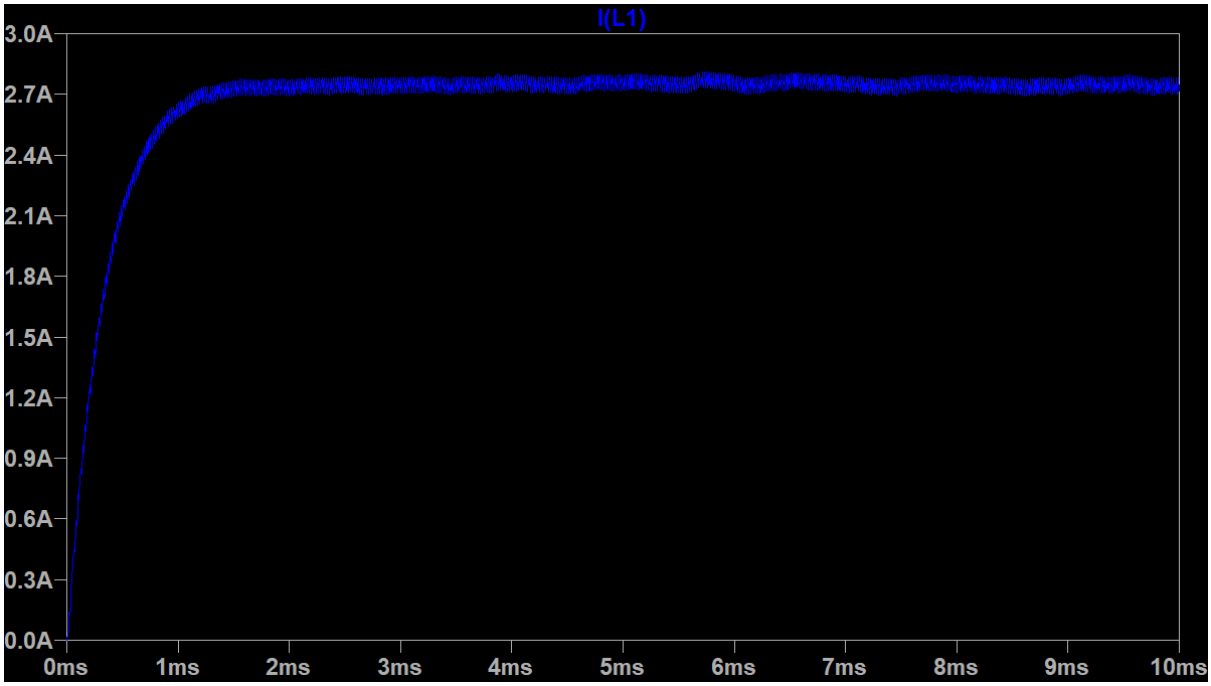
Appendix D: LTspice simulation plots



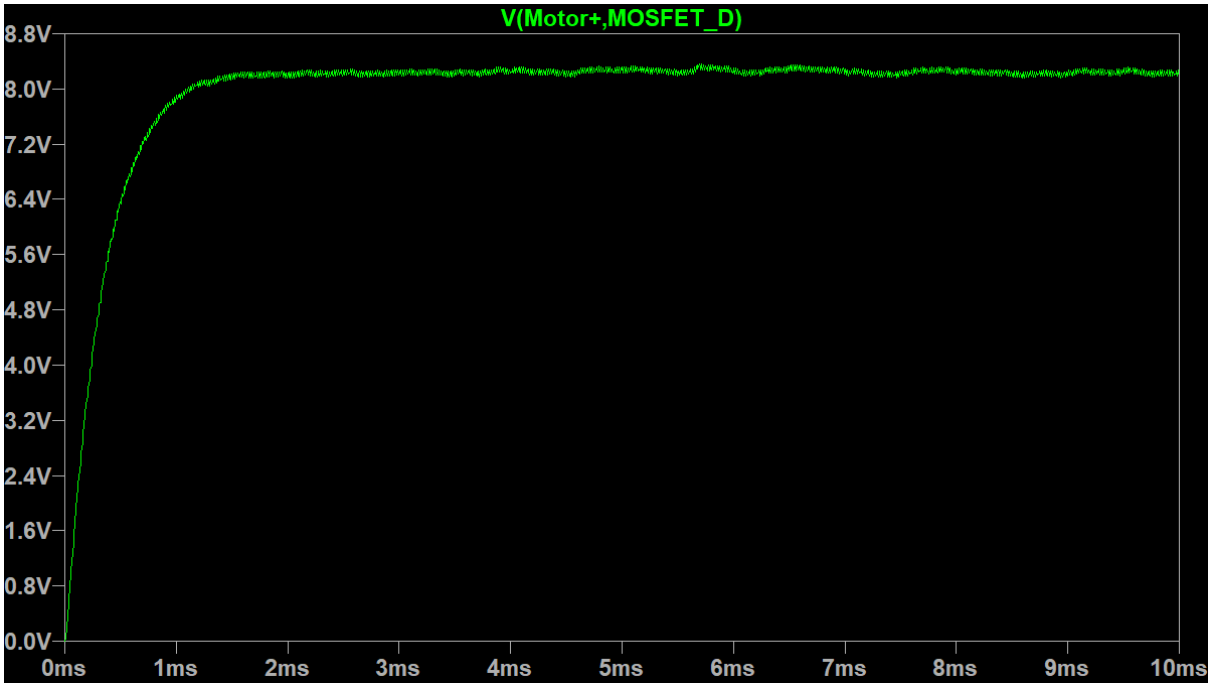
Drain-source voltage across MOSFET



Gate-source voltage across MOSFET



Inductor current



Output voltage