

Mark Ferriss

<https://markferriss.github.io/FerrissPresentation>

History

Work

- 2009-2019: IBM's T.J. Watson Research Lab — *Research Staff Member*
- 2008-2009: University of Michigan — *Postdoctoral Researcher*
- 1998-2002: Analog Devices Inc., Ireland — *Design Engineer*

Education

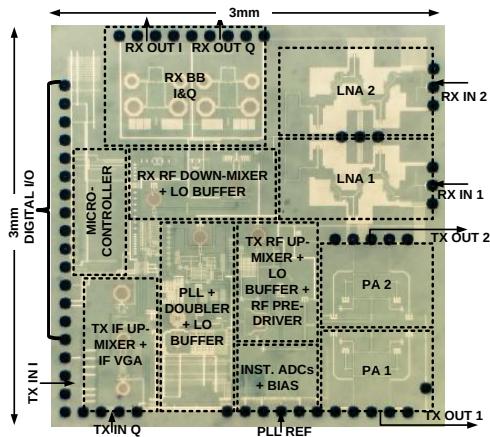
- 2003-2008: *Ph.D.*, University of Michigan
- 1994-1998: *B.E.*, National University of Ireland, Cork (UCC)

Topics

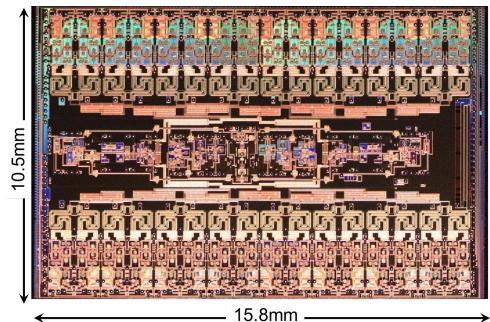
- Self-healing PLLs
- Fractional-N noise cancellation
- Varactor folding
- Flicker noise suppression in VCOs
- Software for phase arrays

IBM's mm-Wave group's big ICs

60GHz Radio



28GHz 32 element phased array

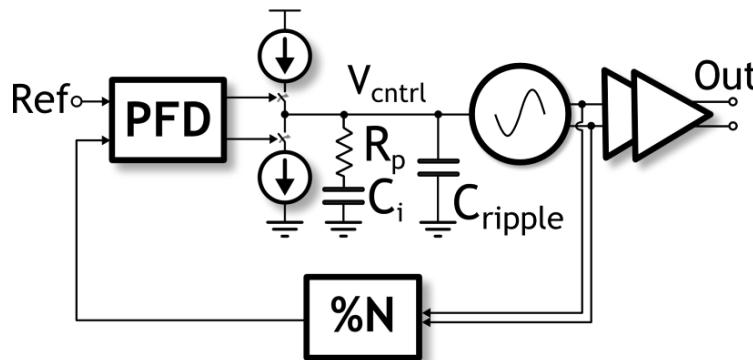


Self-healing PLLs

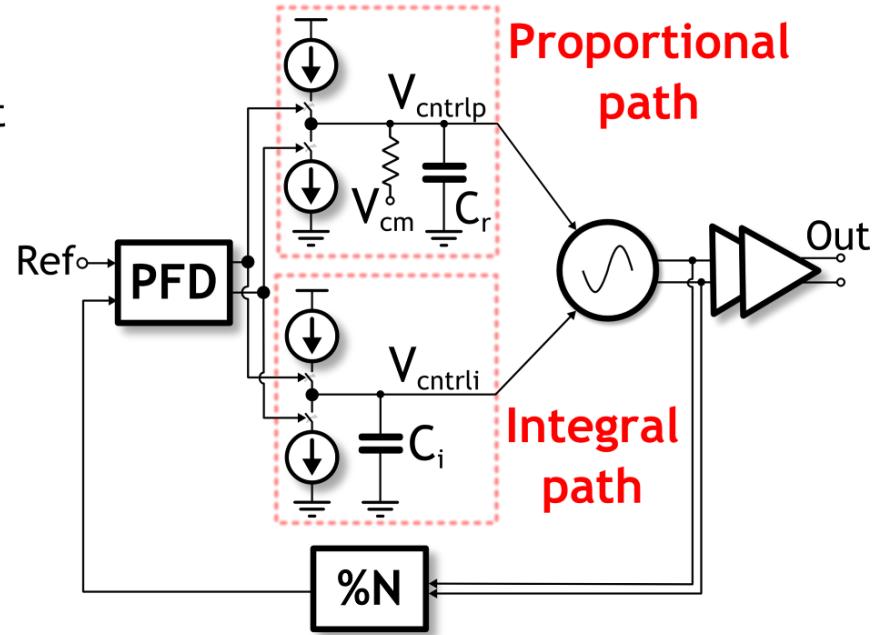
**Ferriss, M.; Plouchart, J.-O.; Natarajan, A.; Rylyakov, A.; Parker, B.;
Babakhani, A.; Yaldiz, S.; Sadhu, B.; Valdes-Garcia, Alberto; Tierno, J.; Friedman, D.,**
"An integral path self-calibration scheme for a 20.1–26.7GHz dual-loop PLL in 32nm SOI CMOS,"
VLSI Circuits (VLSIC), 2012.

Single and dual path PLLs

Single Path PLL



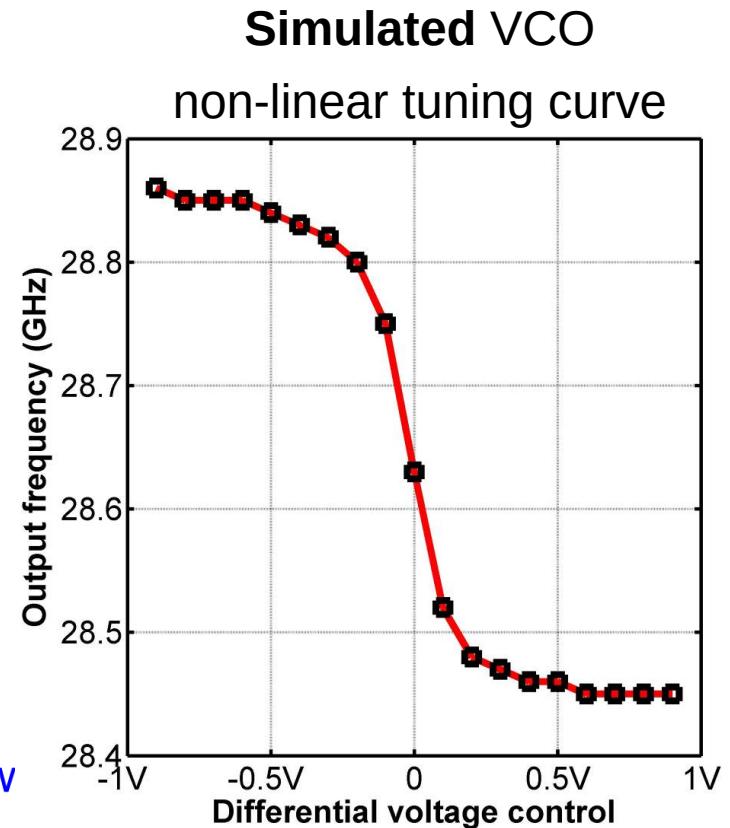
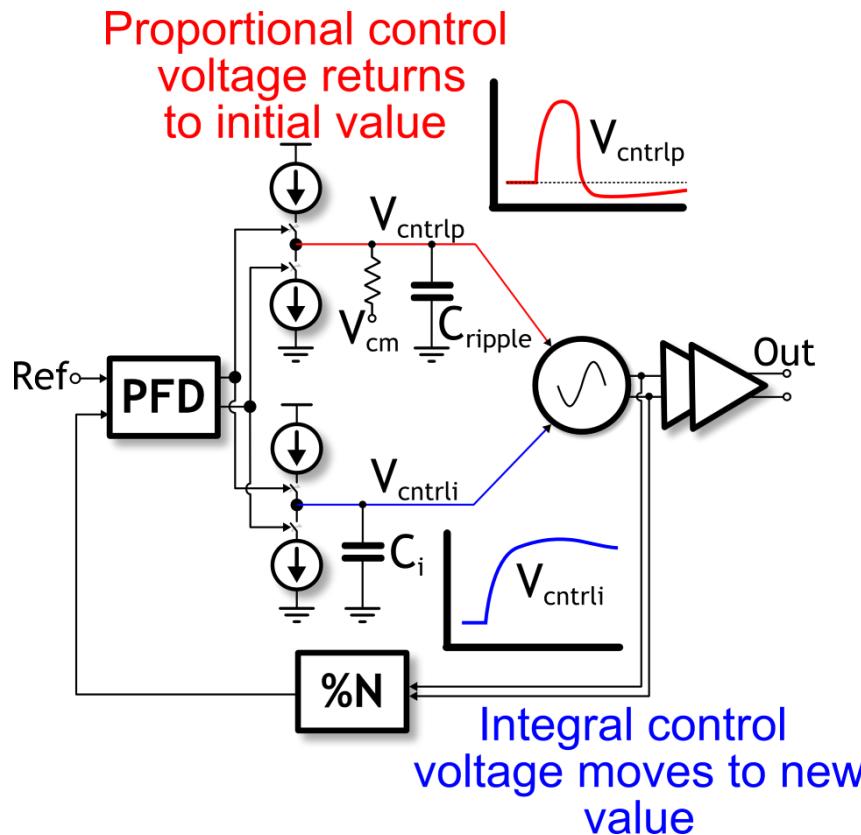
Dual Path PLL



- Split control path into proportional and integral path e.g: [Craninckx, JSSC 1998]
- Requires two charge-pumps and two VCO varactors

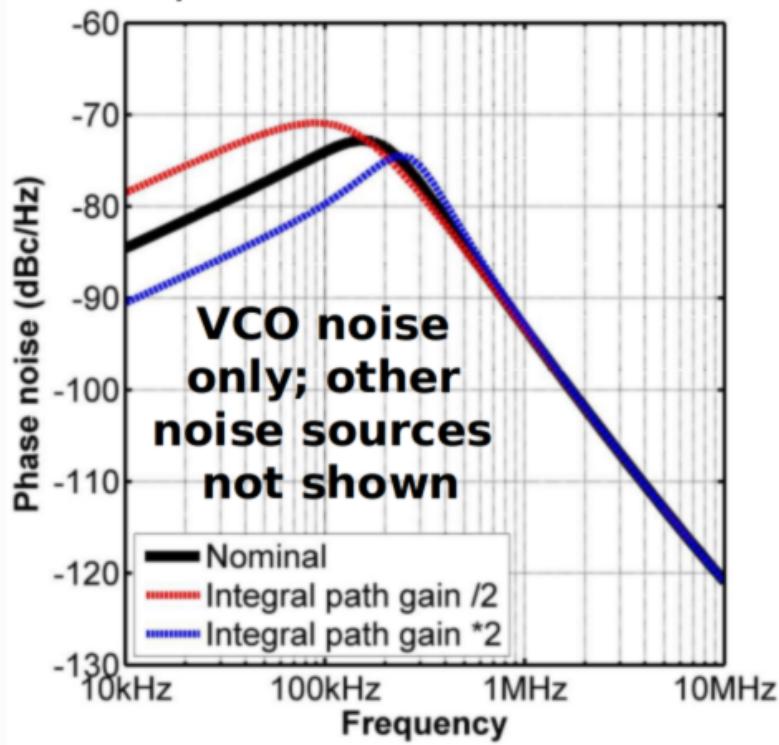
Why use this architecture?

VCO small signal gain variation

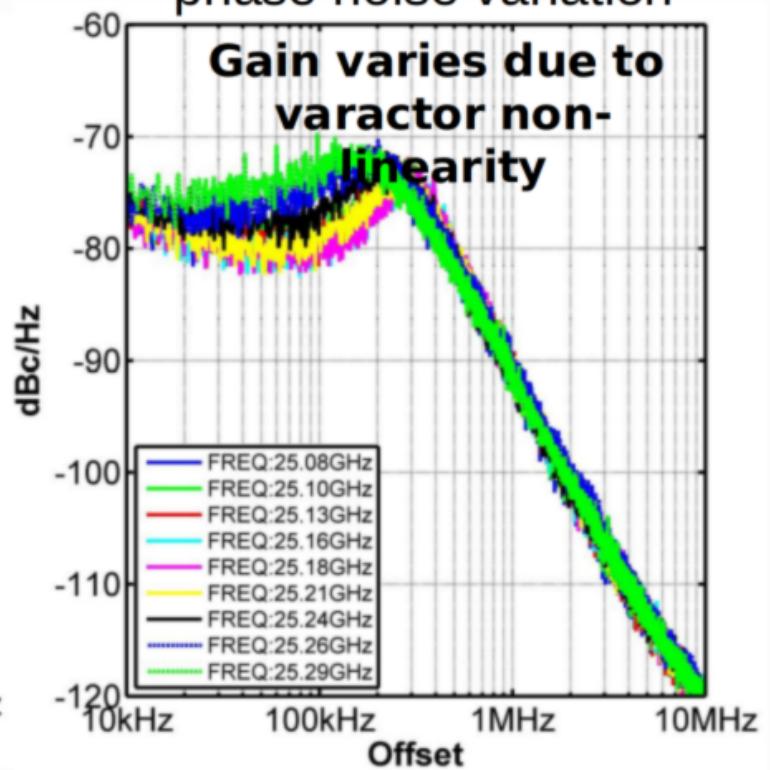


Gain variation affects on PLL phase noise

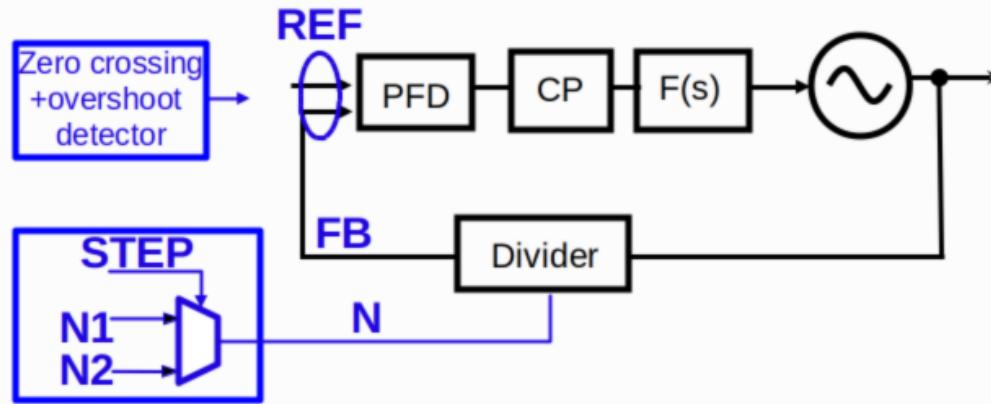
Expected (from Matlab)
phase noise variation



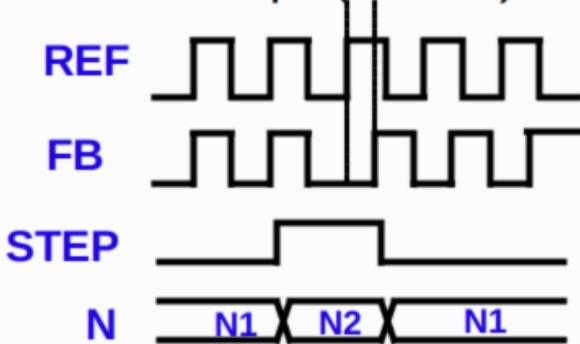
Measured (from hardware)
phase noise variation



Prior-art bandwidth correction



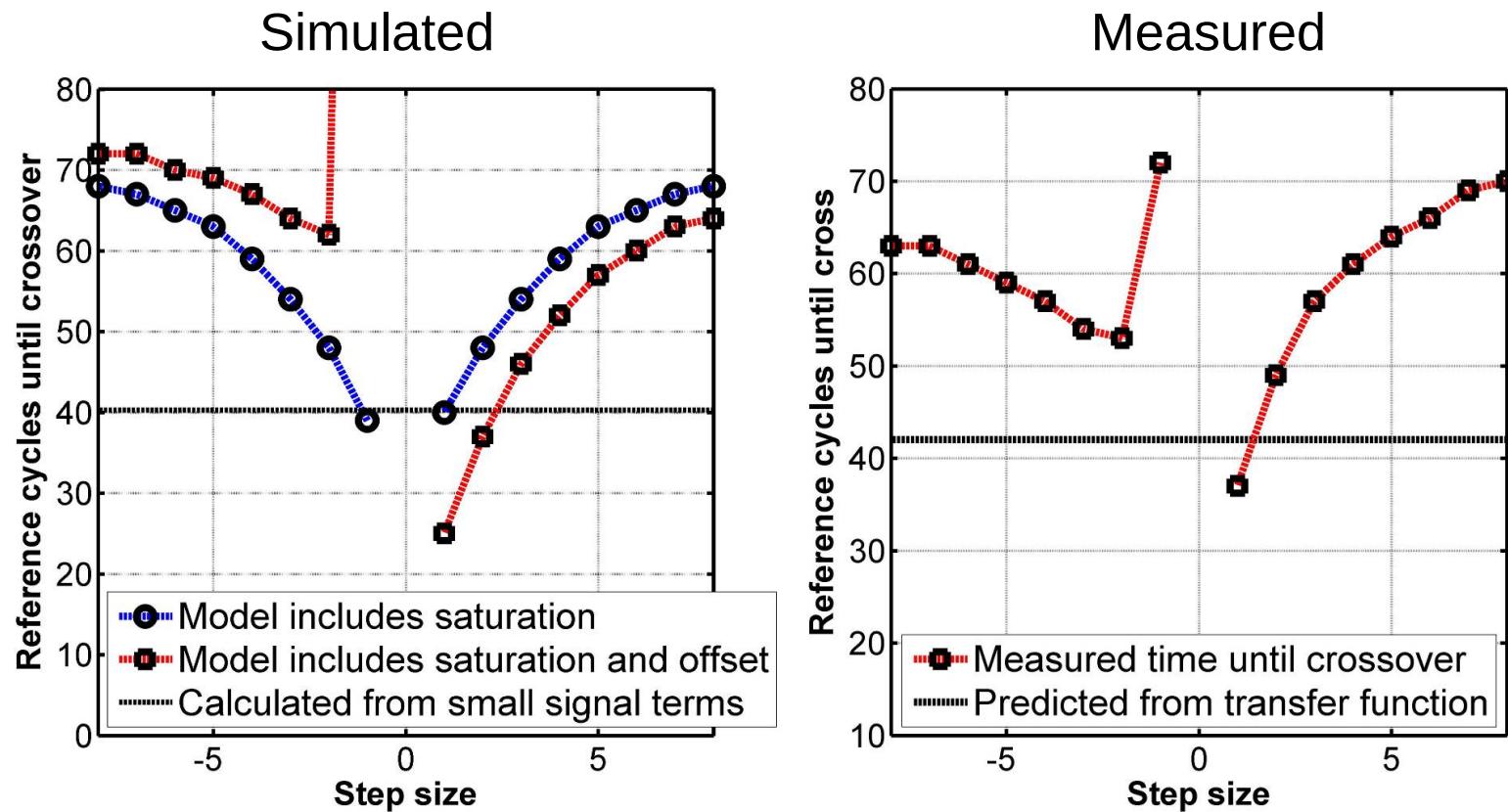
$$\Delta\Phi = 2\pi \cdot (N_2 - N_1) / N_1$$



STEP1: Inject phase step into loop by changing the divide ratio

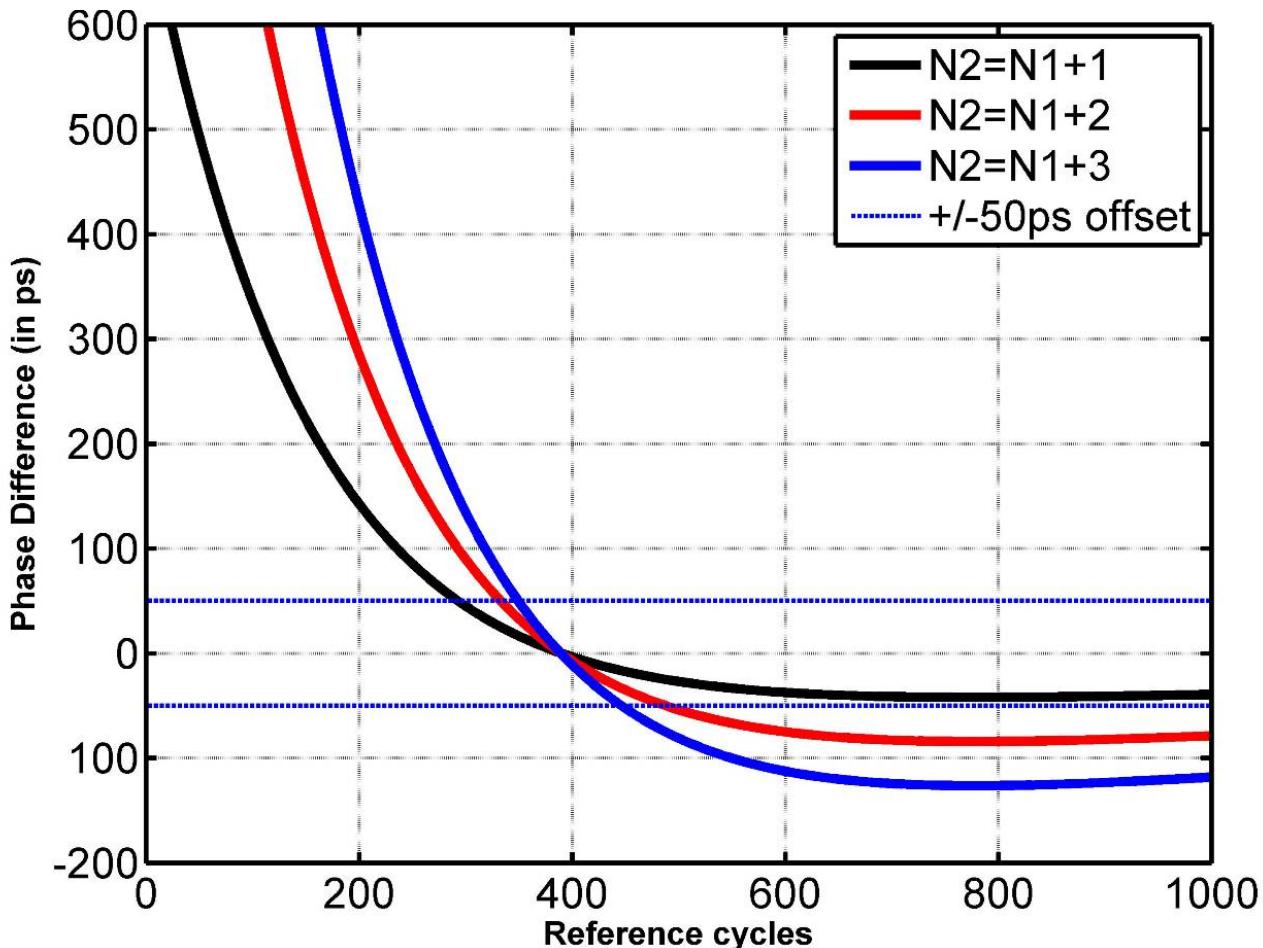
STEP2: Measure time to cross over
[D. Fischette, et al, CICC 2009]

Effects of non-linearity and offsets



- Saturation corrupts measurement when step is large
- Offset corrupts measurement when step is small

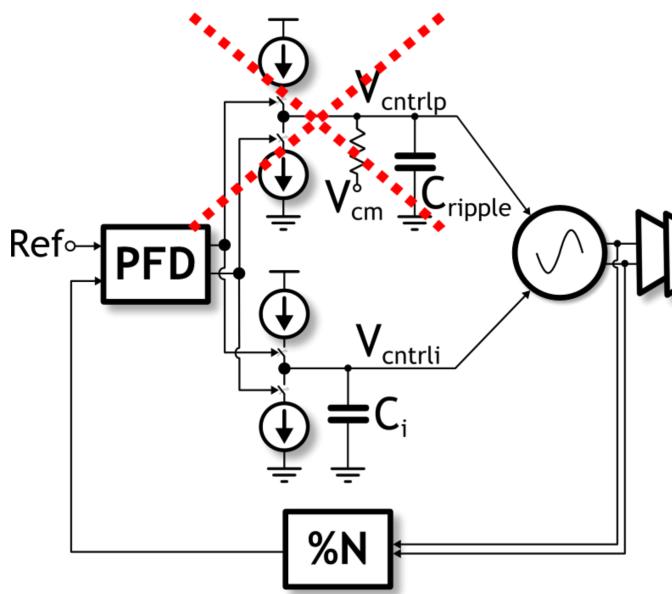
Time-to-crossover in presence of offsets



Real measurement has offsets caused by: Charge pump current mismatch, capacitor leakage, BB-PFD offset, etc.

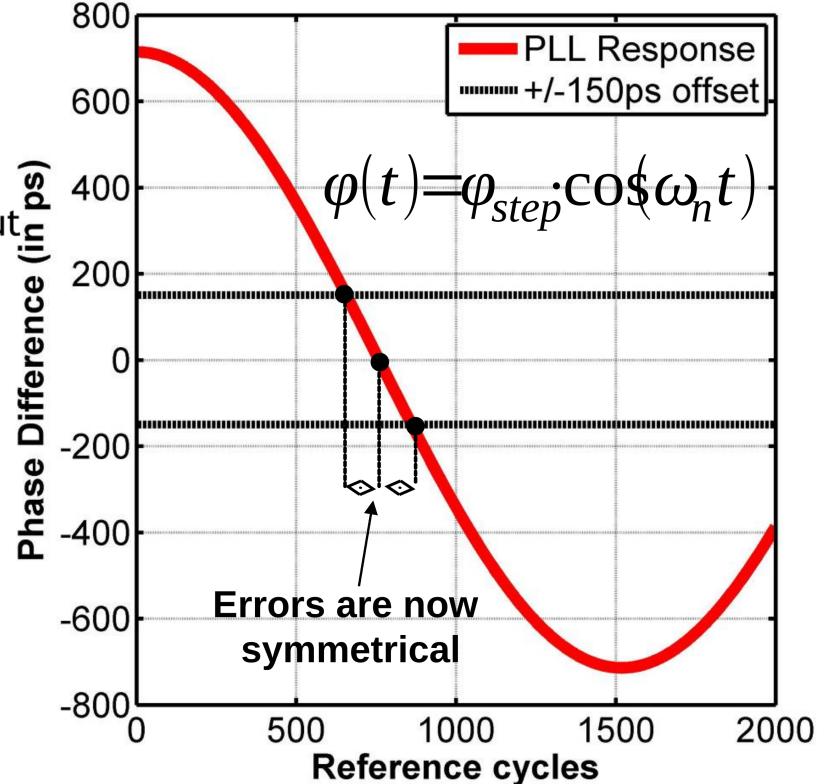
PLL response to a phase step, with no proportional path

Disable proportional path



Proportional path can be
temporarily disabled.

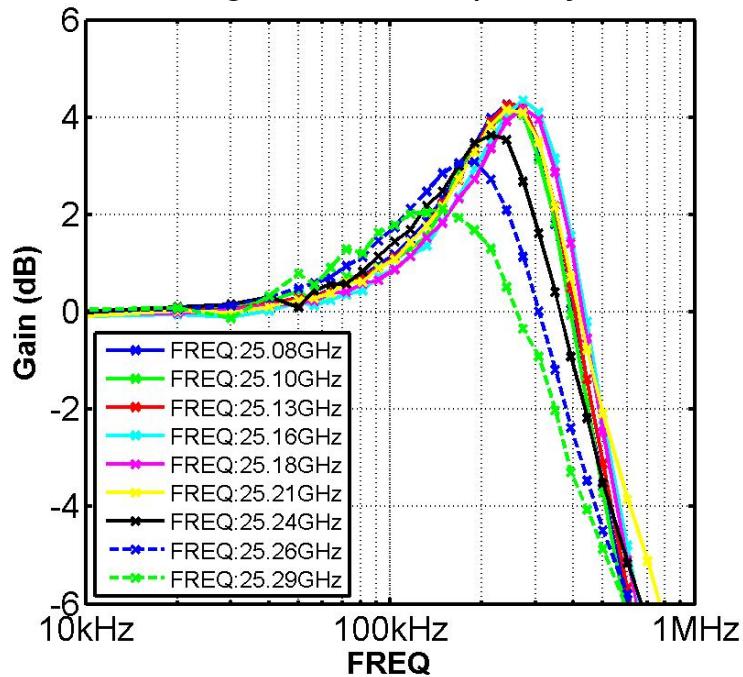
Response to phase step



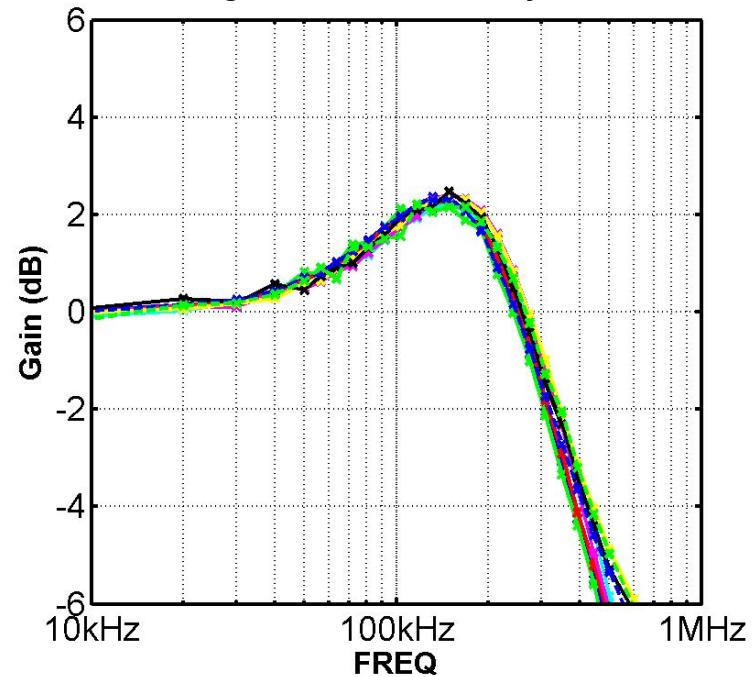
- Saturation corrupts measurement when step is large
- Offset corrupts measurement when step is small

Transfer function before/after calibration

Measured PLL transfer function
in a single coarse frequency band



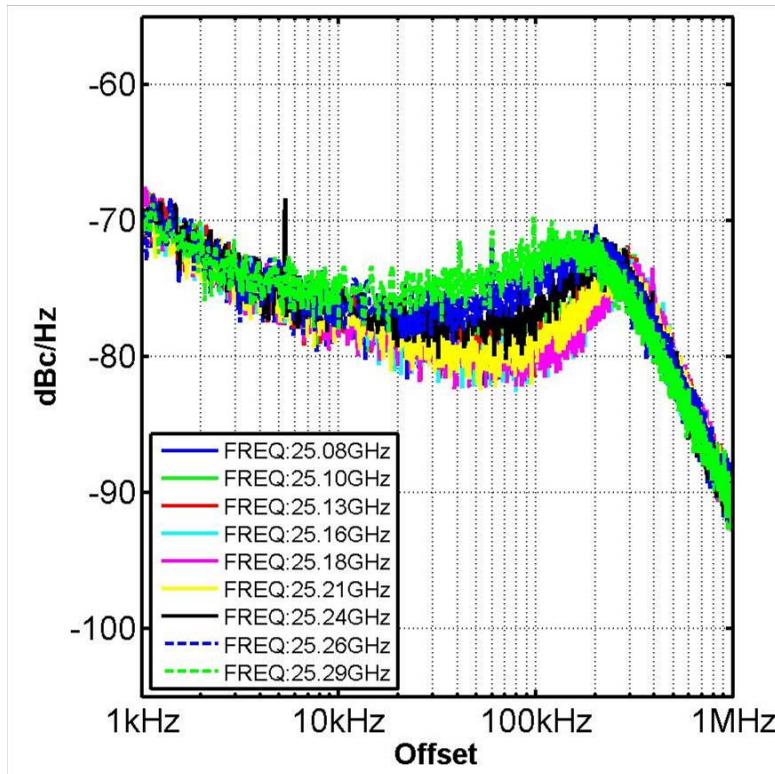
Measured PLL transfer after
enabling the calibration system



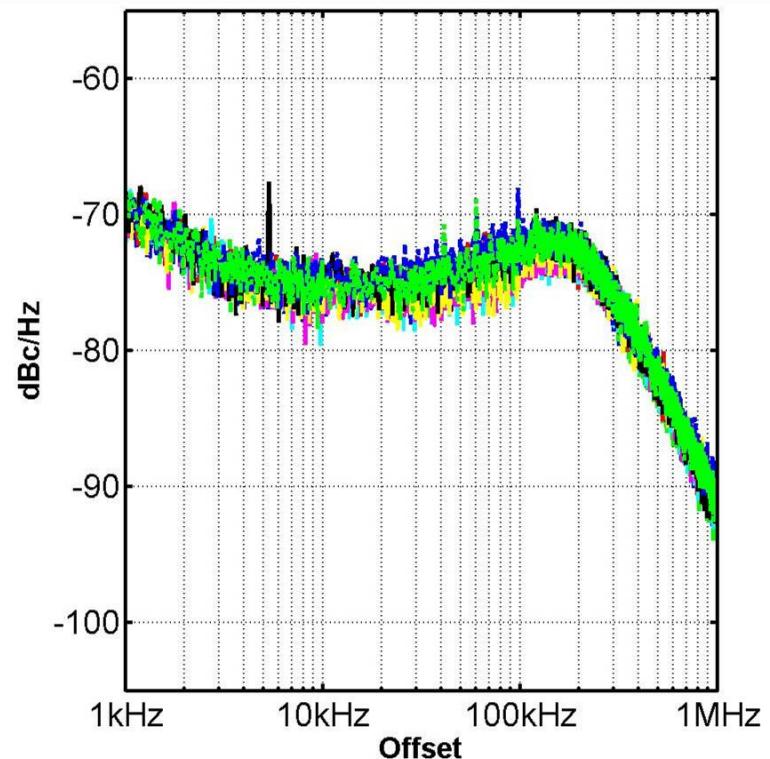
Calibration system stabilizes transfer function

Phase noise before/after calibration

Measured phase noise

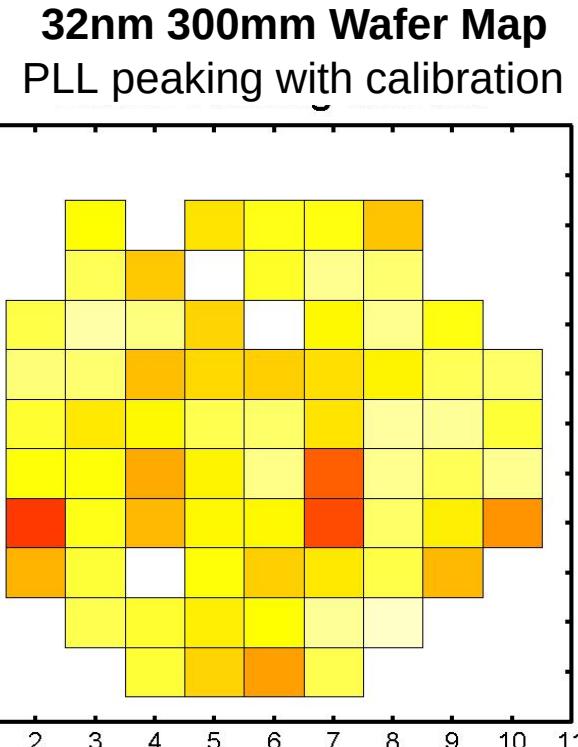
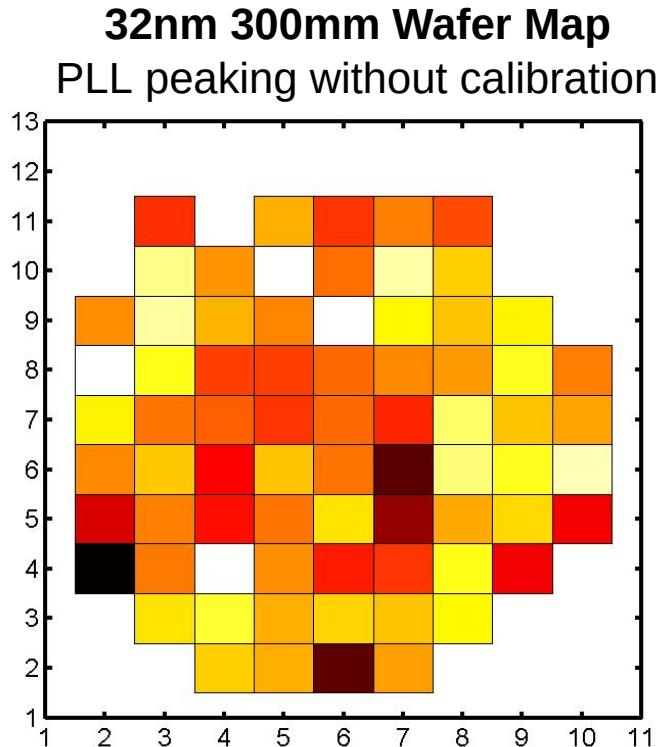


Measured phase noise after enabling the calibration system



Stabilized transfer function leads to phase noise uniformity

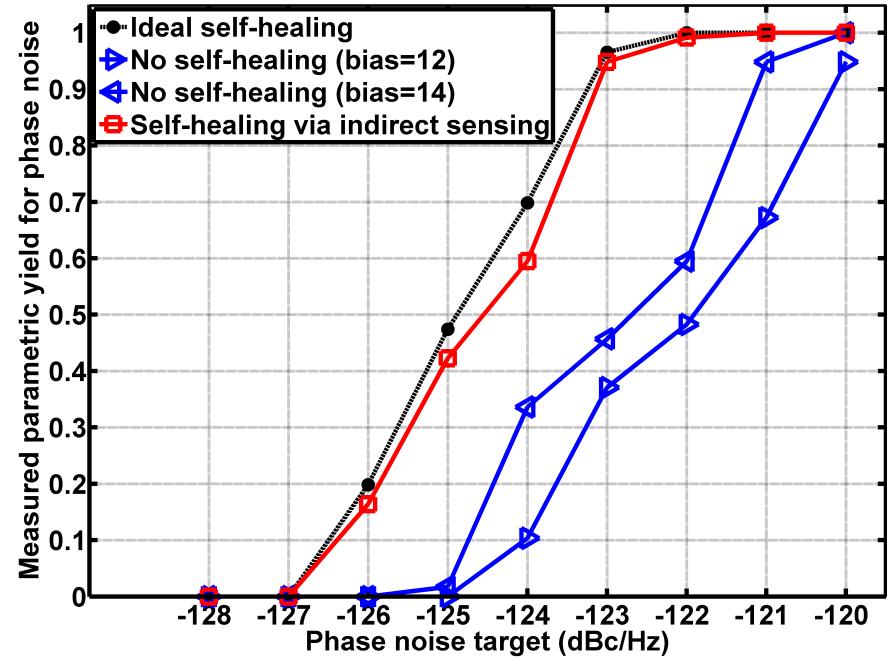
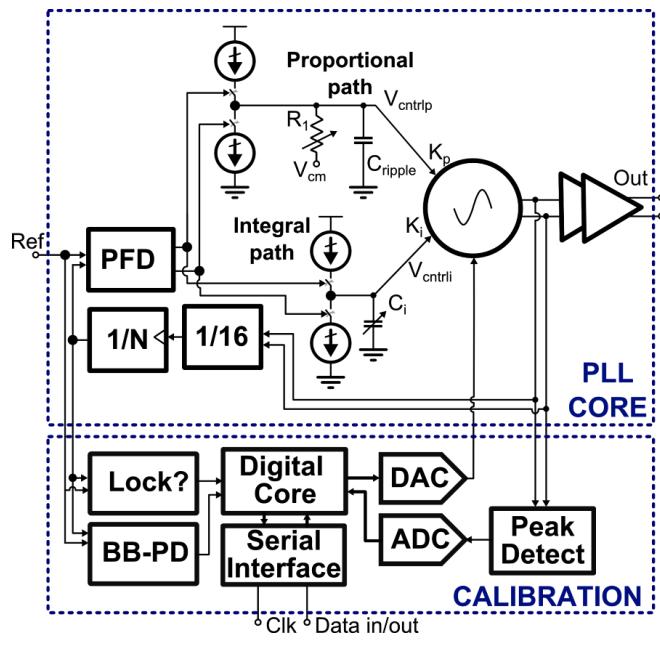
Wafer level test



Measured jitter peaking (in dB) before/after calibration. Tested every die on a 300mm wafer at 25GHz

Improved uniformity shown across wafer

Parametric phase noise healing



Noise @10MHz = f(VCO f_{nom}, Amplitude, Bias Voltage and Current, VCC, Band)

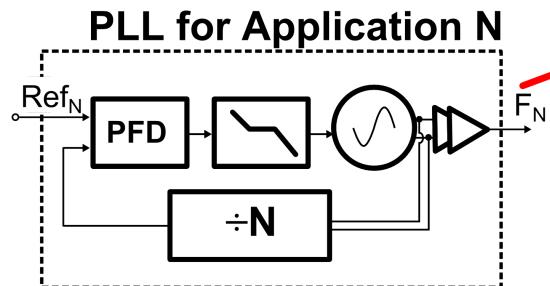
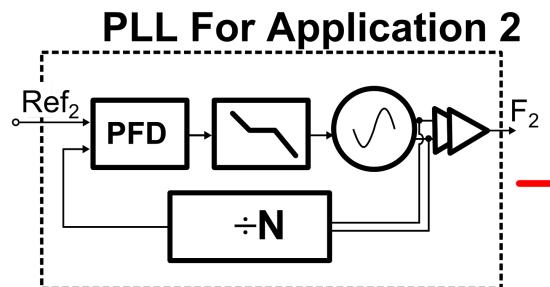
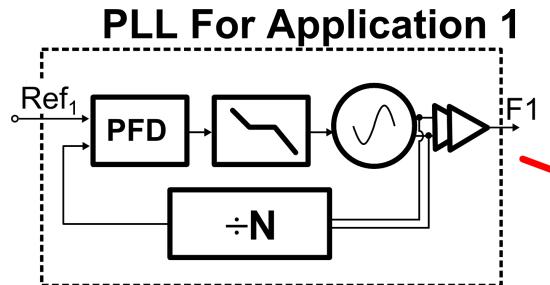
Methodology described in: S. Yaldiz, V. Calayir, X. Li, L. Pileggi, A. Natarajan, M. Ferriss and J. Tierno, “Indirect Phase Noise Sensing for Self-Healing Voltage Controlled Oscillators,” IEEE CICC, Mar. 2011.

Fractional-N noise cancellation

Ferriss, M.; Sadhu, B.; Rylyakov, A.; Ainspan, H.; Friedman, D.,

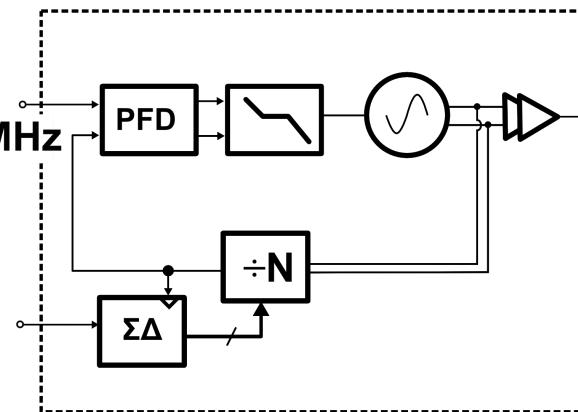
"A 13.1-to-28GHz fractional-N PLL in 32nm SOI CMOS with a $\Delta\Sigma$ noise-cancellation scheme,"
IEEE International Solid-State Circuits Conference (ISSCC), 2015.

Objective



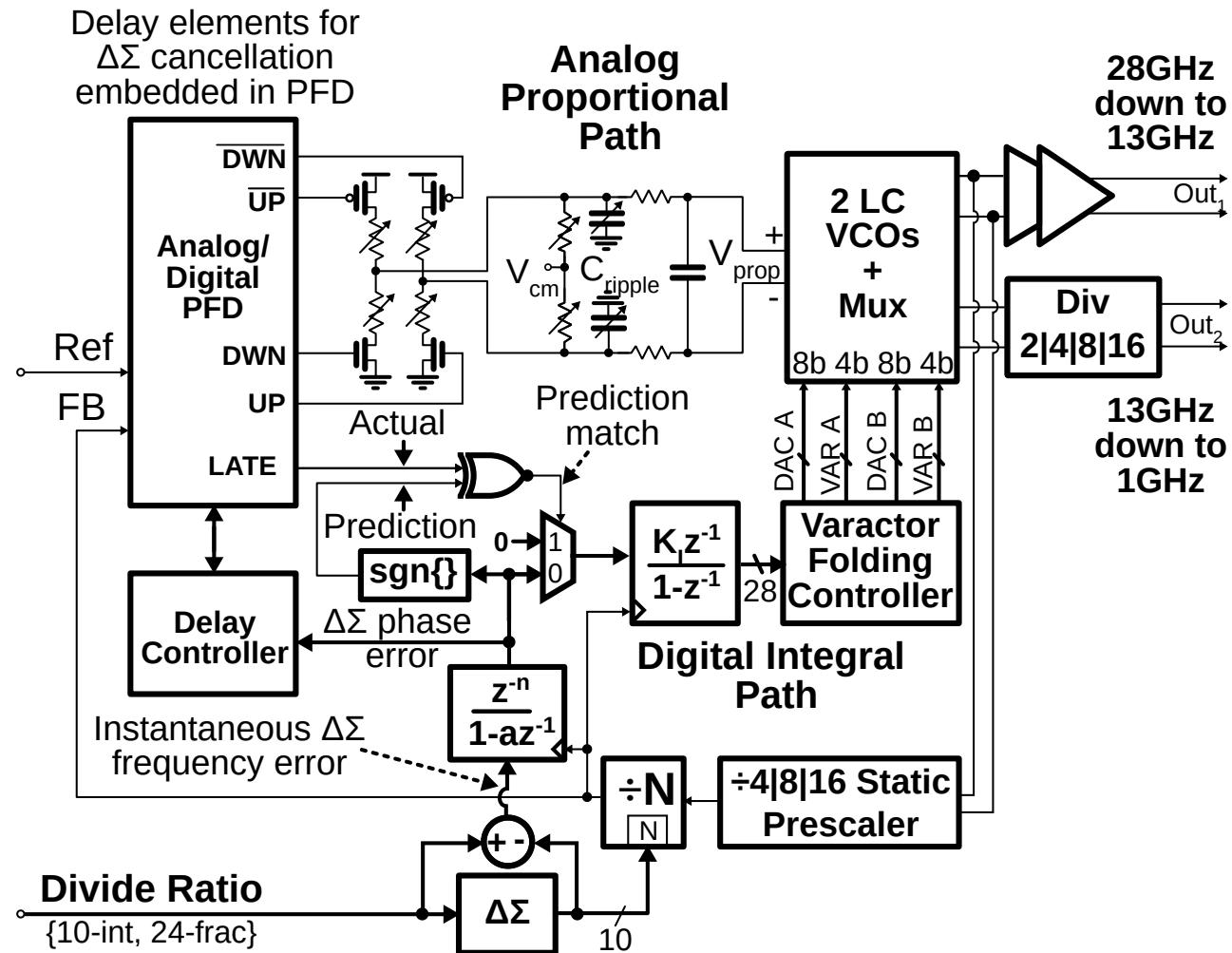
Flexible PLL For Multiple Applications

Any
reference
rate from
15Mz to 400MHz



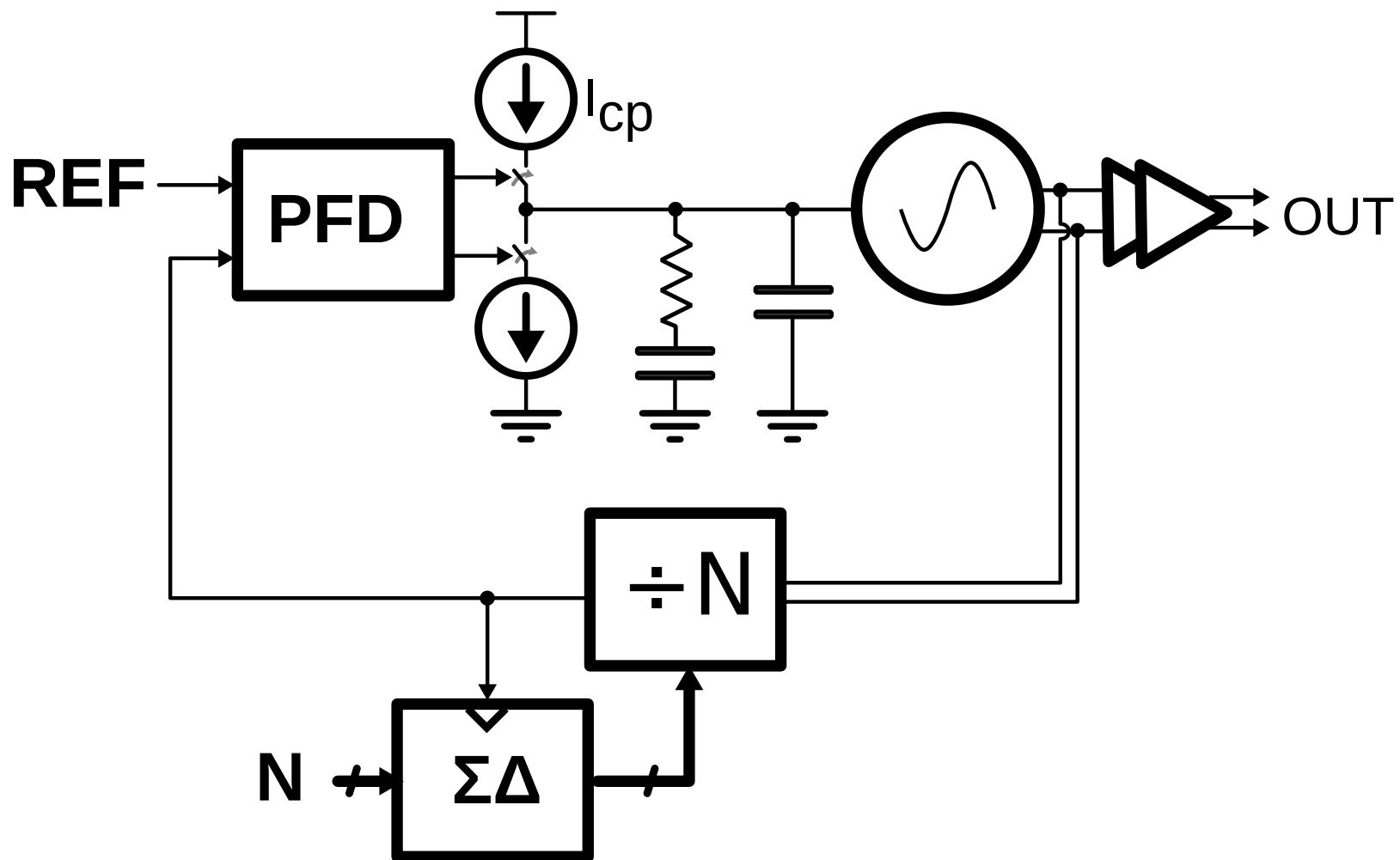
Generate
any
frequency
from
28GHz
down to
1GHz

Hybrid PLL Architecture

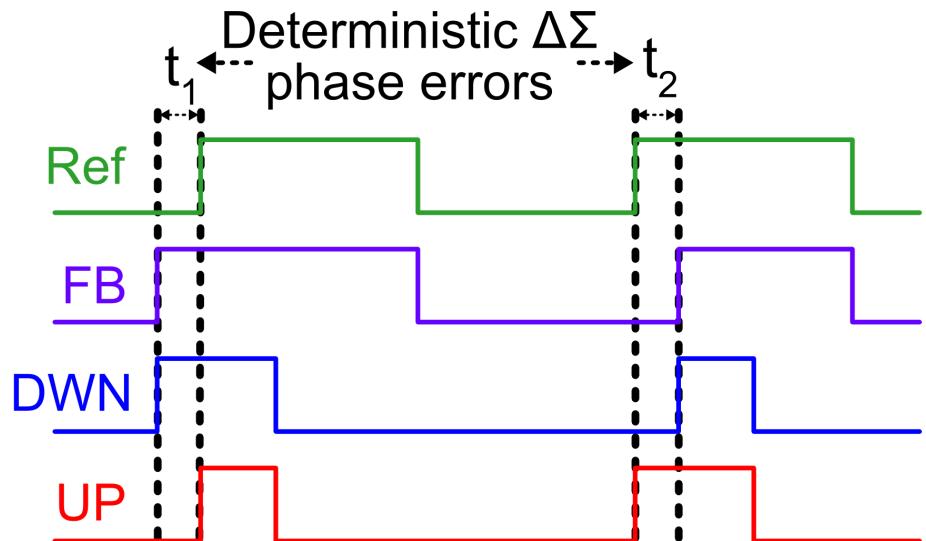
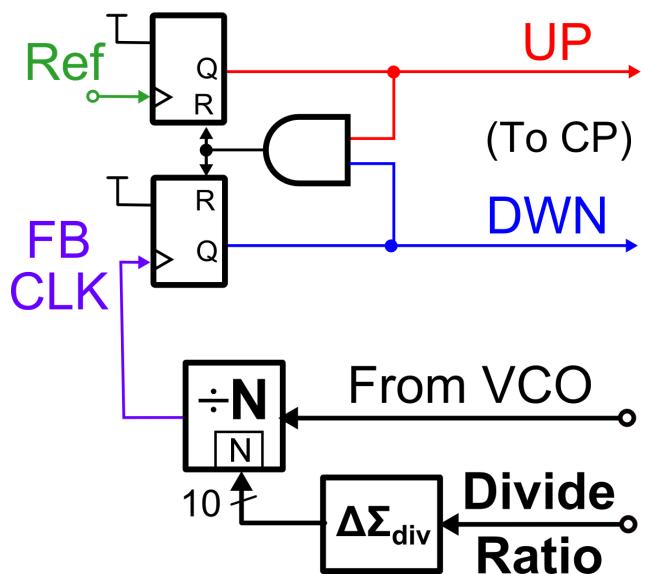


Baseline integer-N Hybrid PLL from [Ferriss, et al., JSSC 2014]

Classic Fractional-N PLL

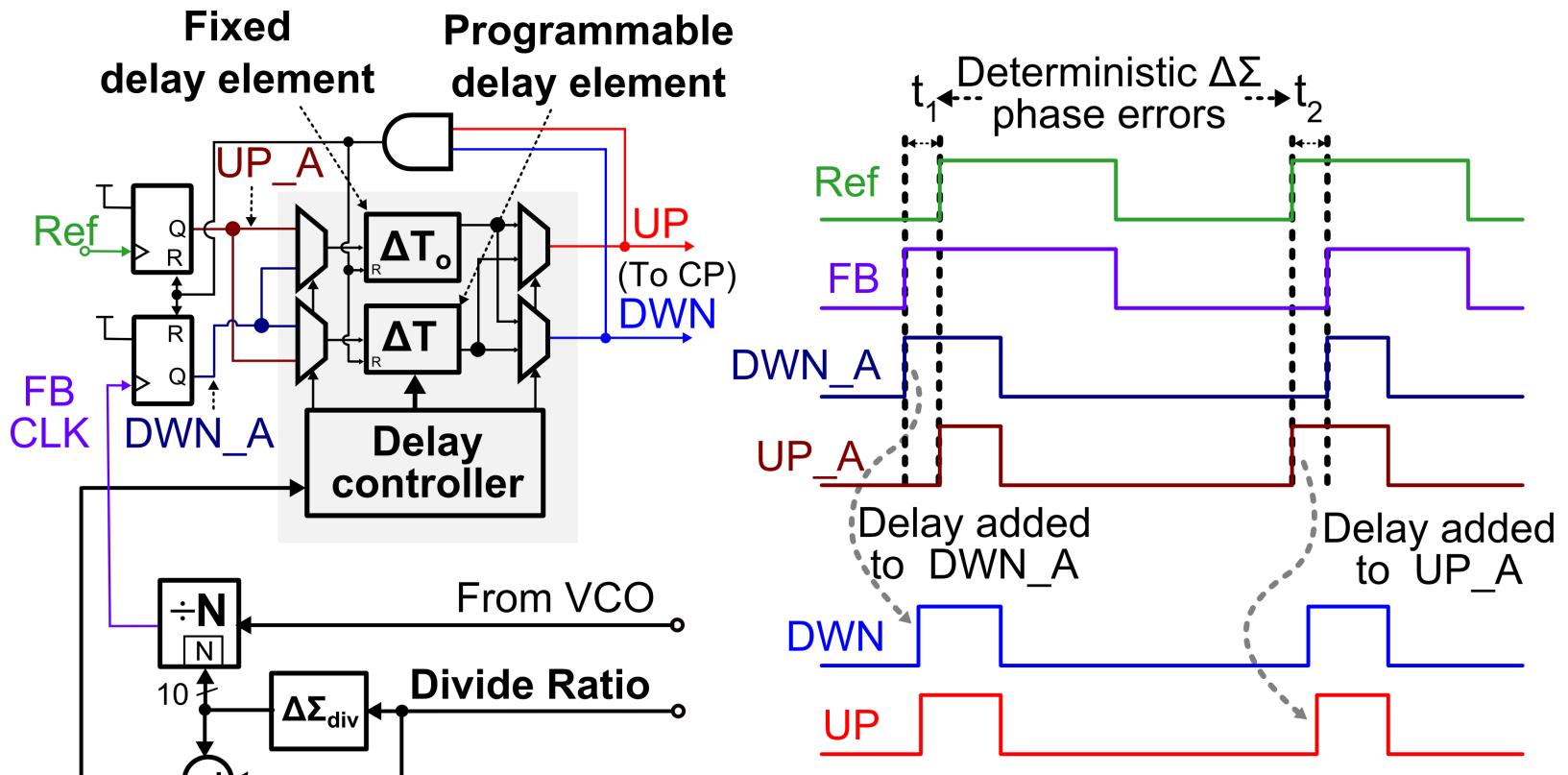


Classic $\Delta\Sigma$ Problem



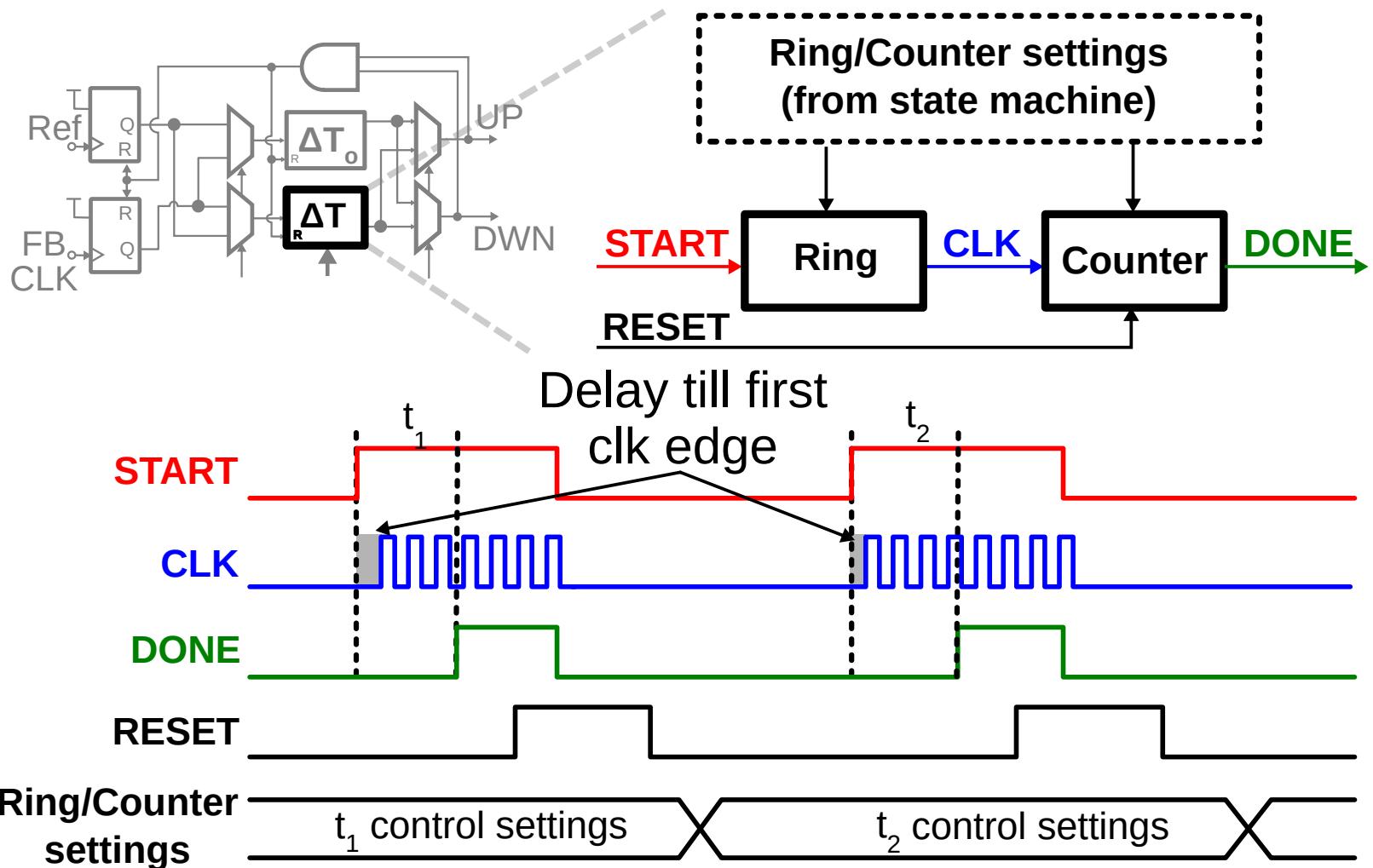
- Divider's $\Delta\Sigma$ dithers PLL's feedback (FB) clock
- $\Delta\Sigma$ noise contributes to PLL's phase noise

Time-based Cancellation Concept

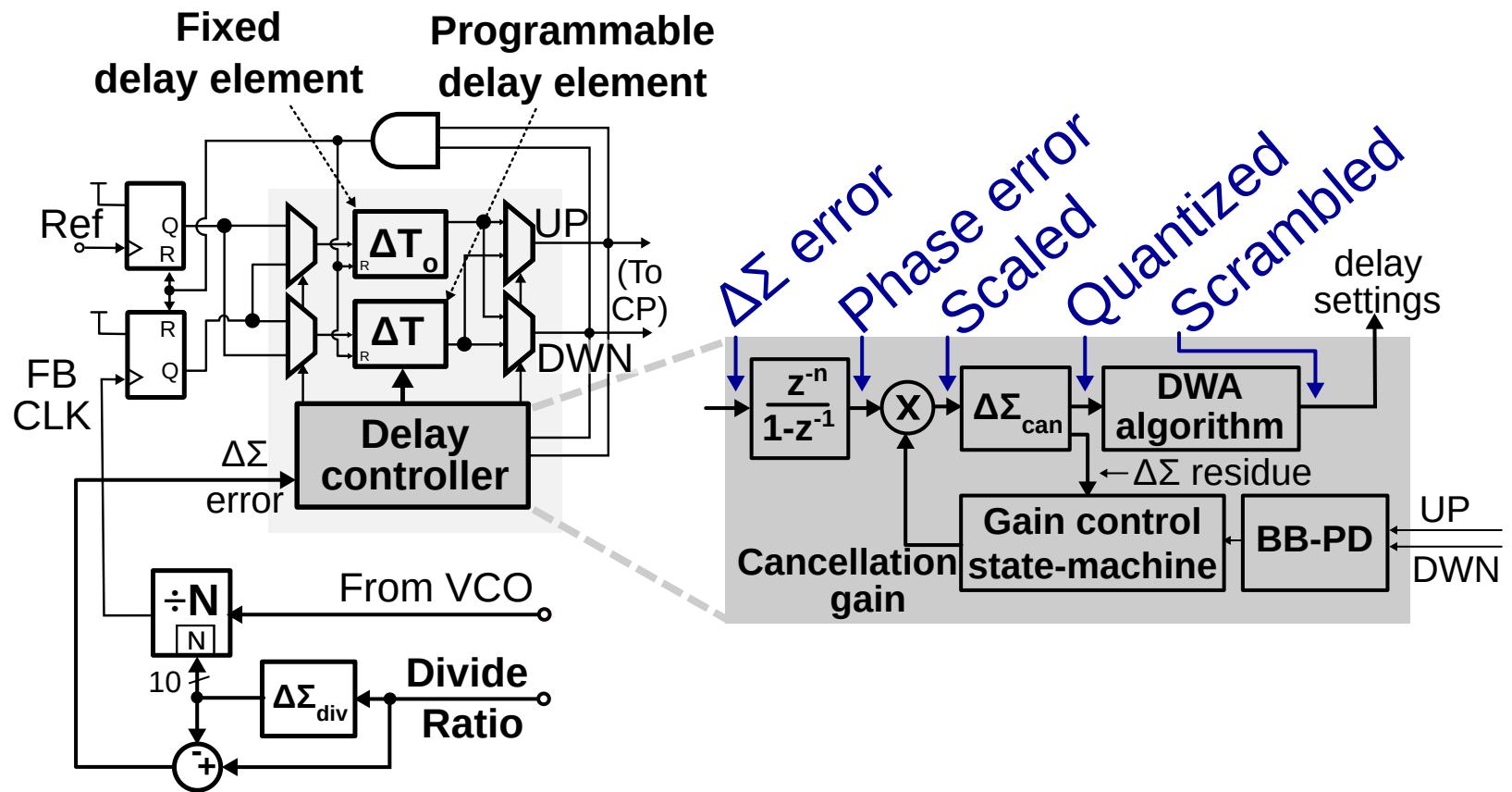


- Digital-to-time based delay scheme used on analog path
 - Utilizes loop filter's low pass response to remove delay path quantization noise -> Don't need fine quantization step.

Components of delay generation



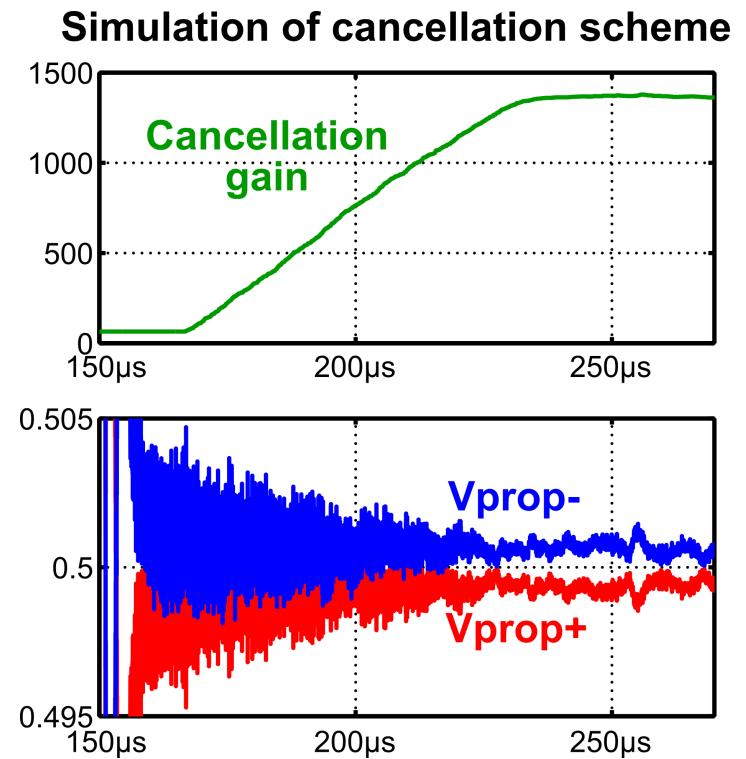
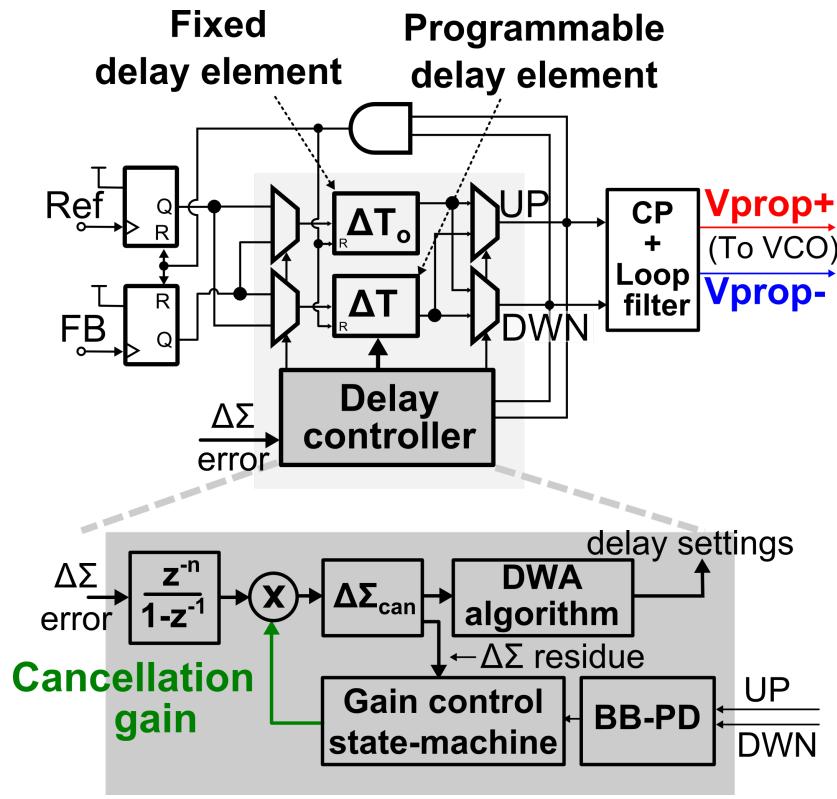
Delay Controller Architecture



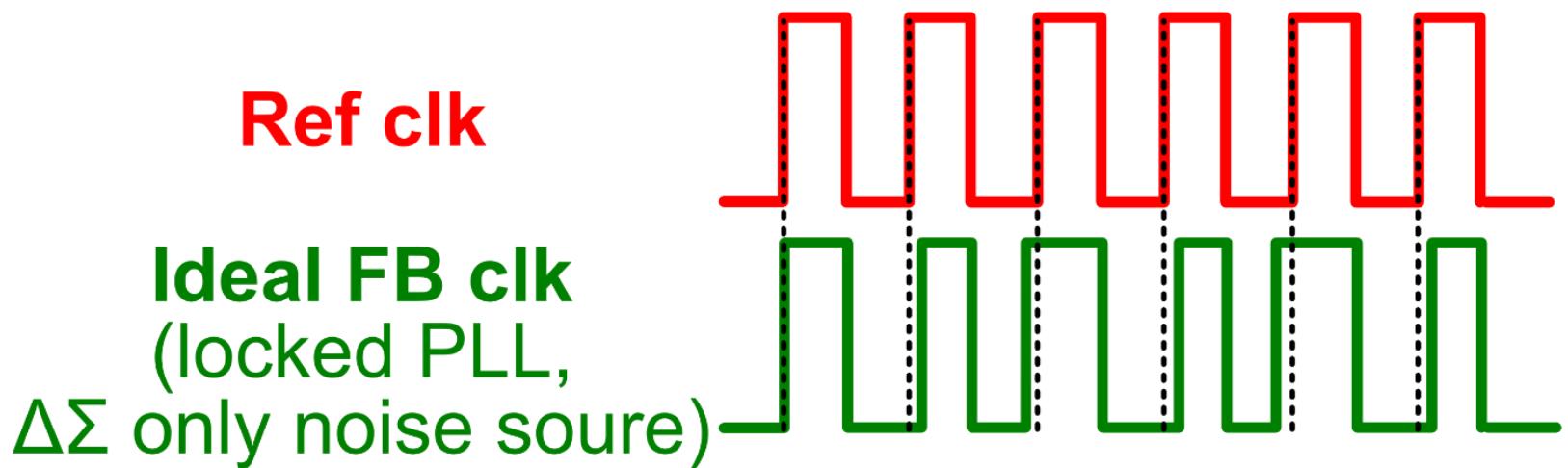
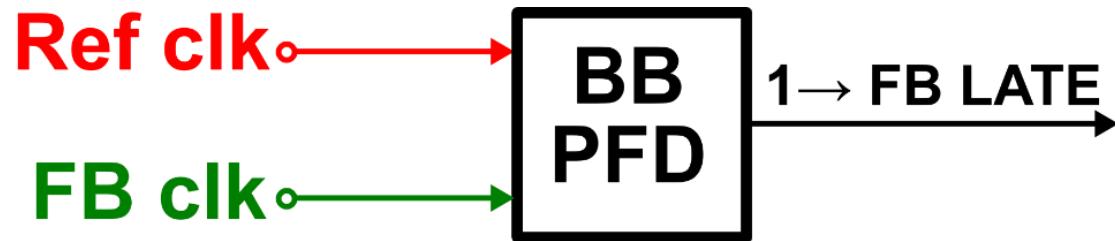
Controller's function is to:

- (1) Background calibrate DTC gain, (2) Shape ΔT quantization error, and (3) Shape the mismatch error

Delay Controller Operation Simulation

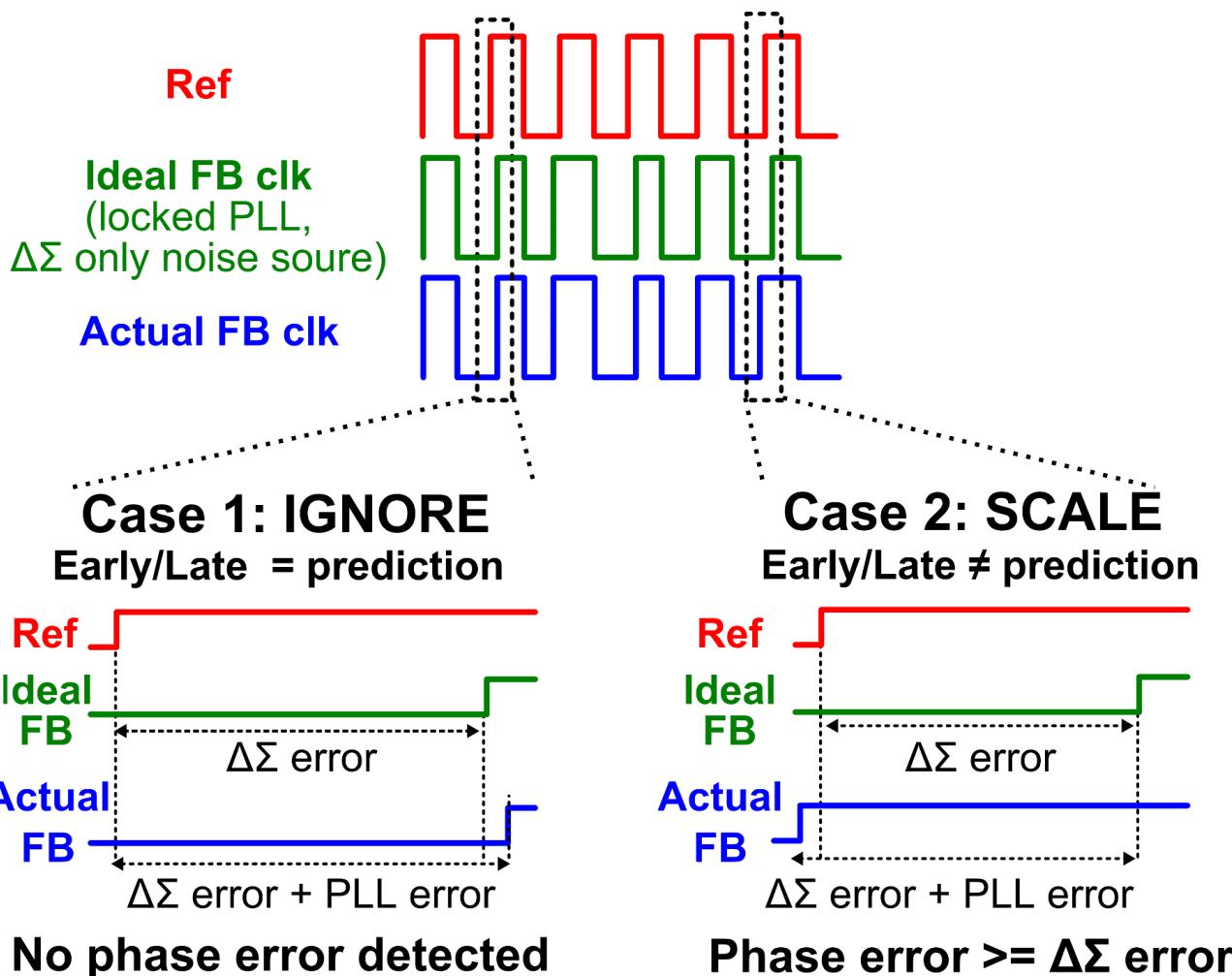


Integral Path Introduction

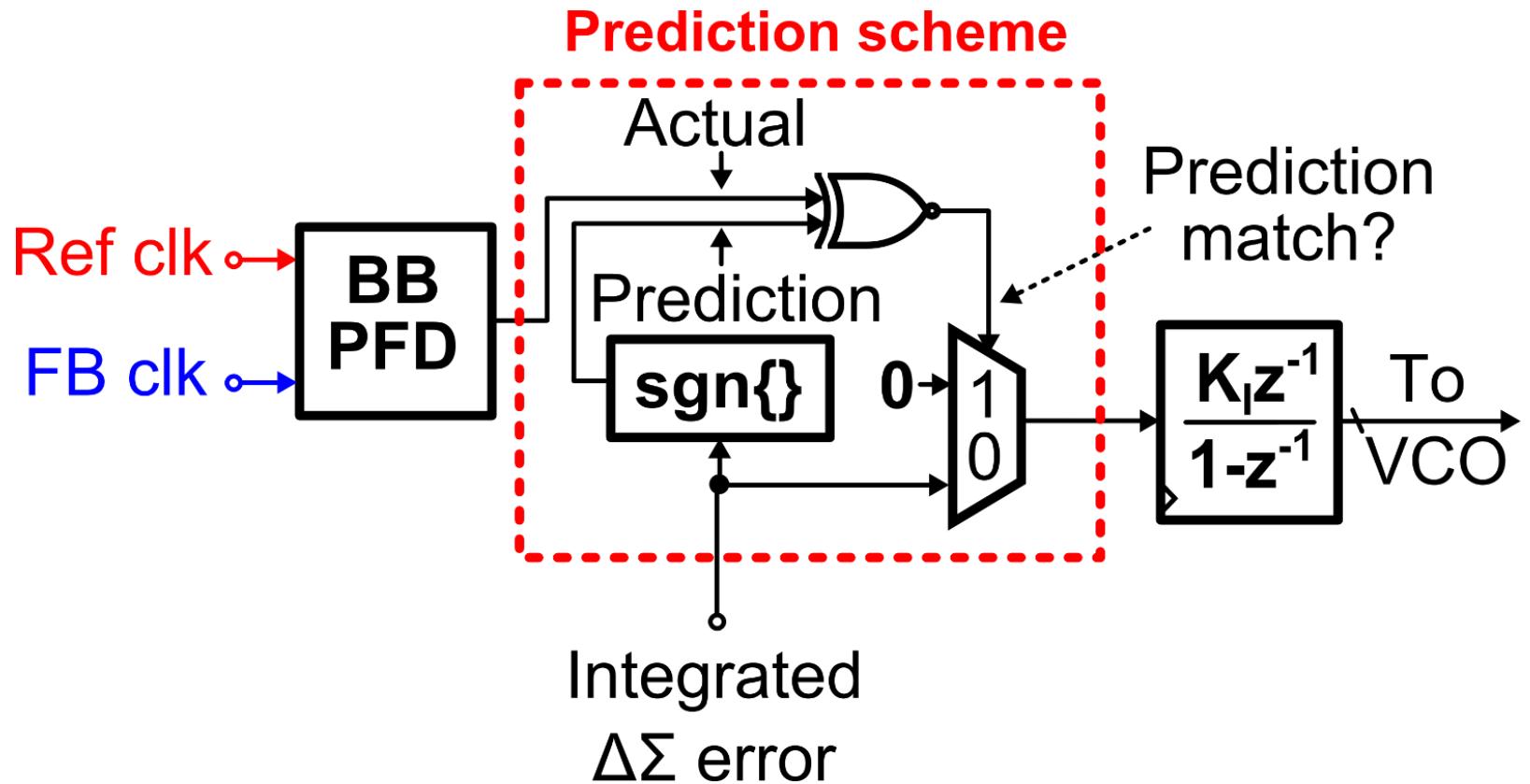


How do we interpret early/late information?

Integral Path Prediction Concept

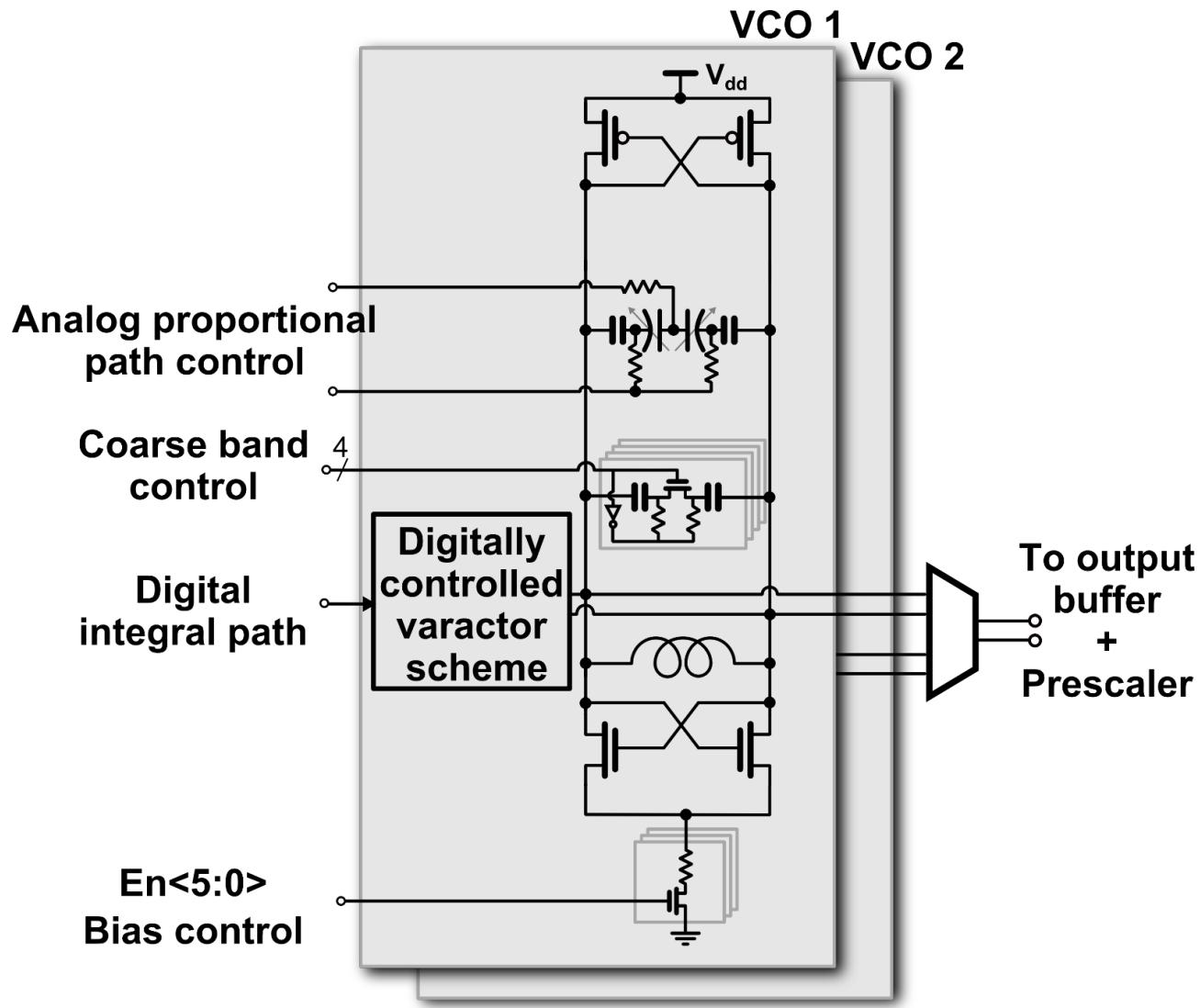


Integral Path Prediction Circuit

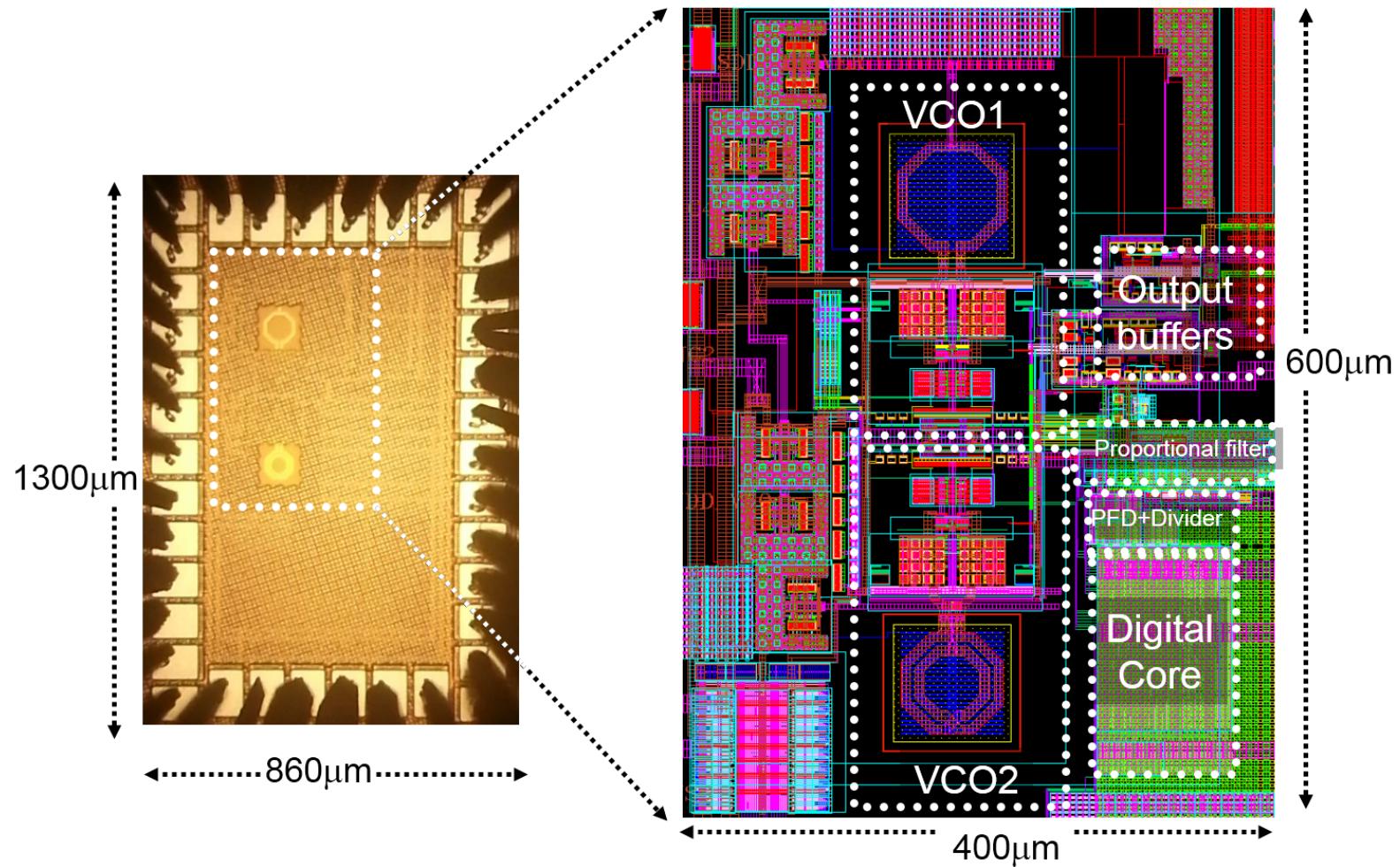


- Integral path operates from single BB phase detector
 - Works in parallel with the analog proportional path
- Ignores BB results that match prediction

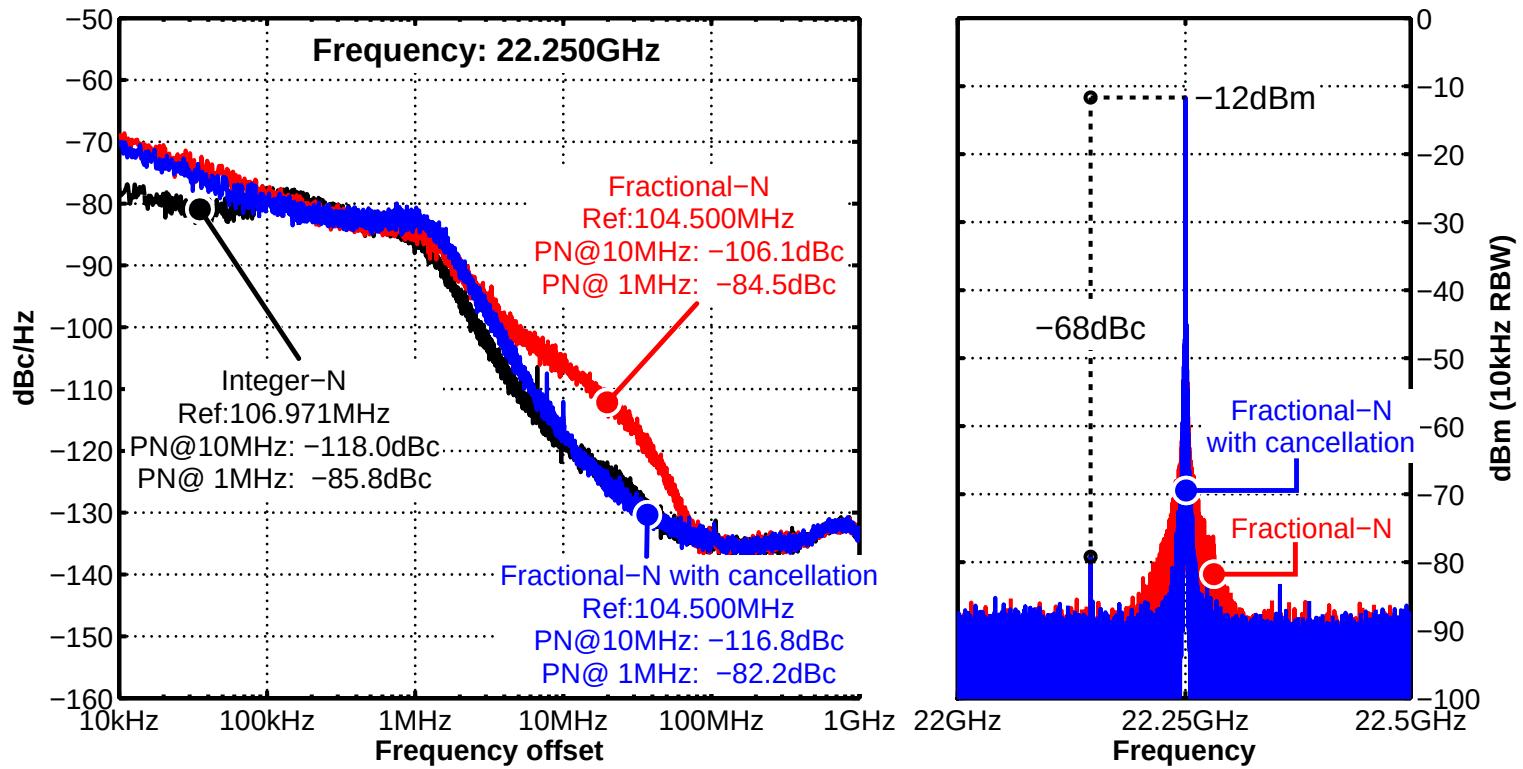
Dual D/VCO Scheme



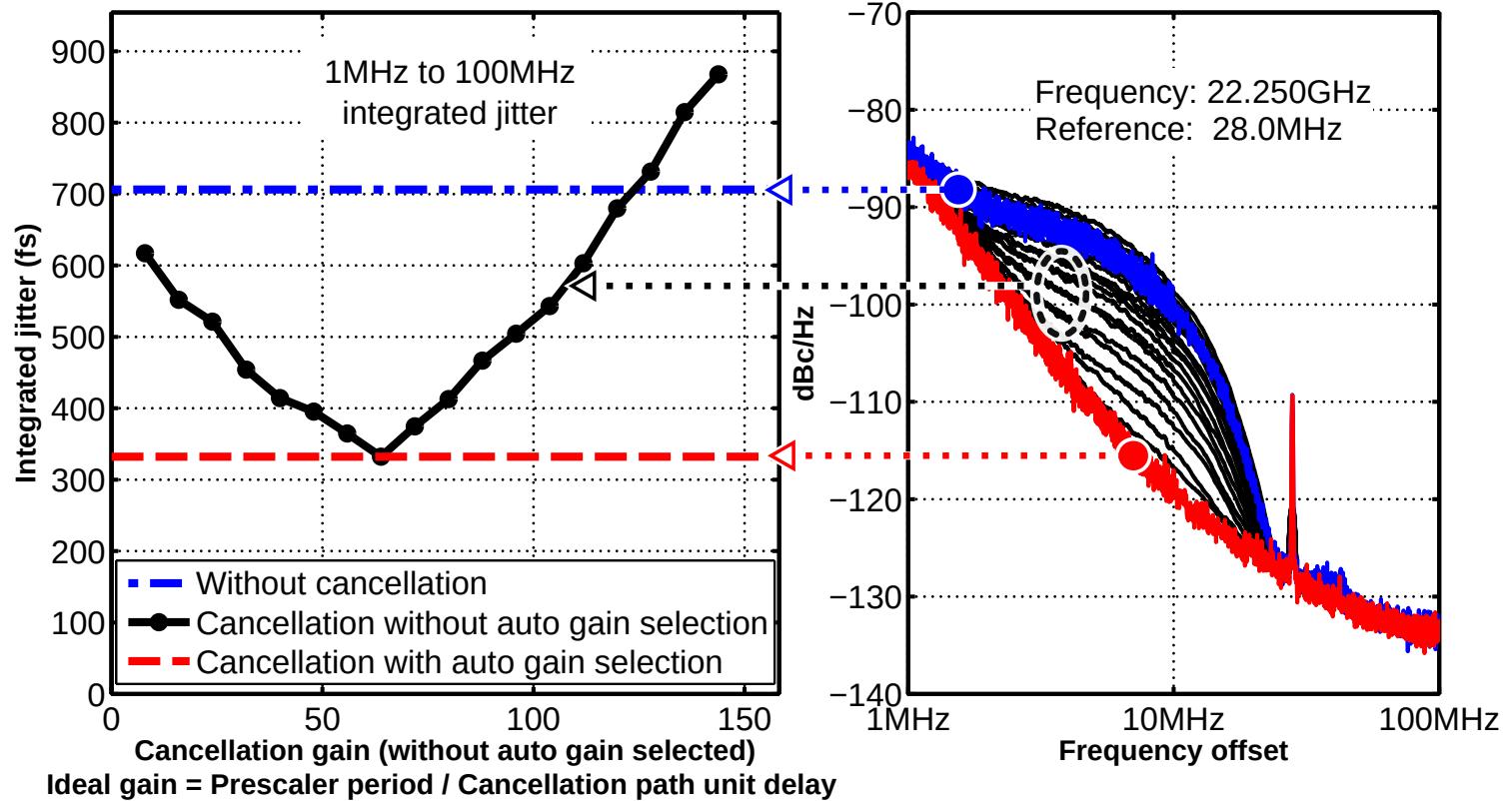
Die Photo with Layout



Measured Phase Noise and Output Spectrum

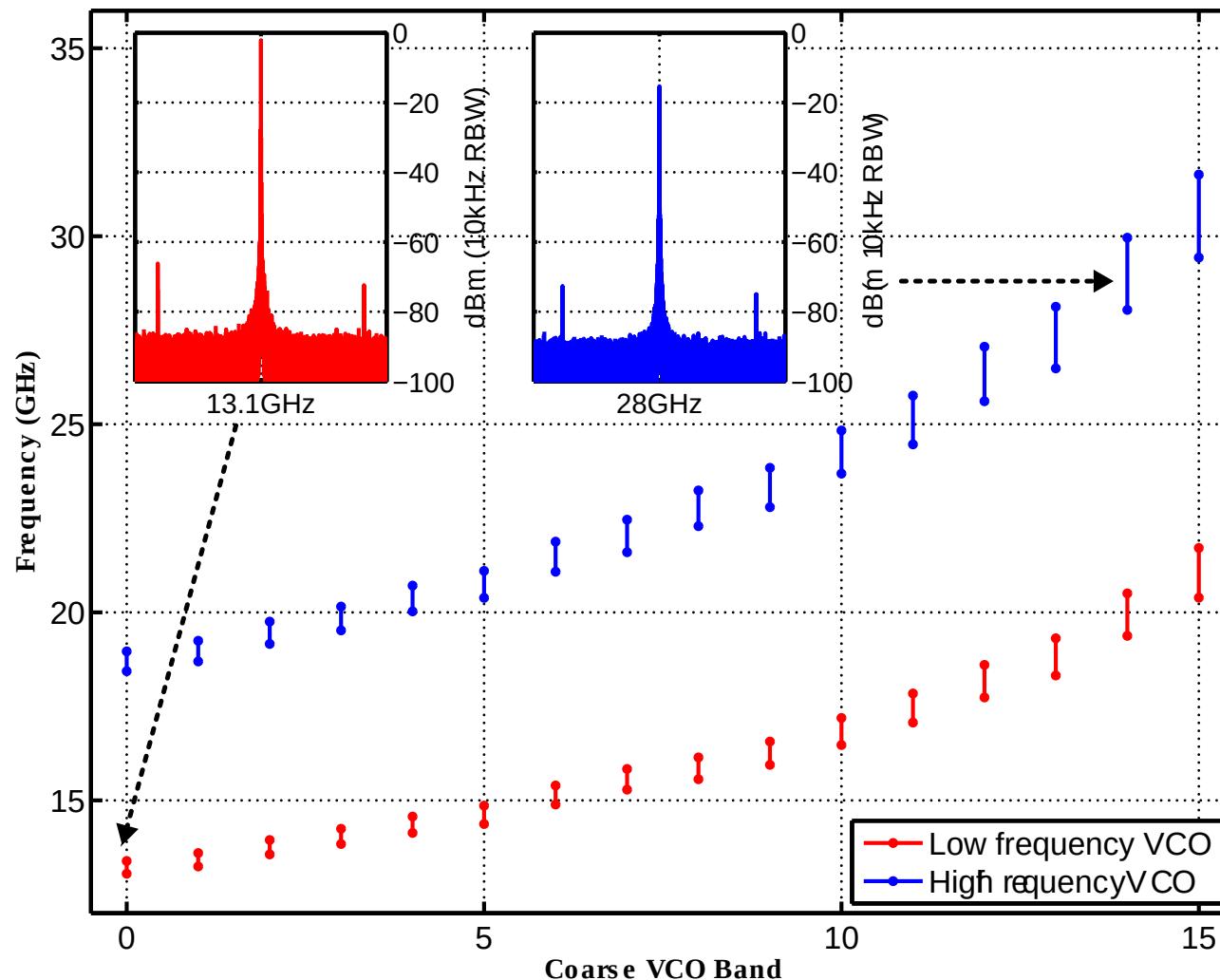


Demonstration of DTC Background Cal

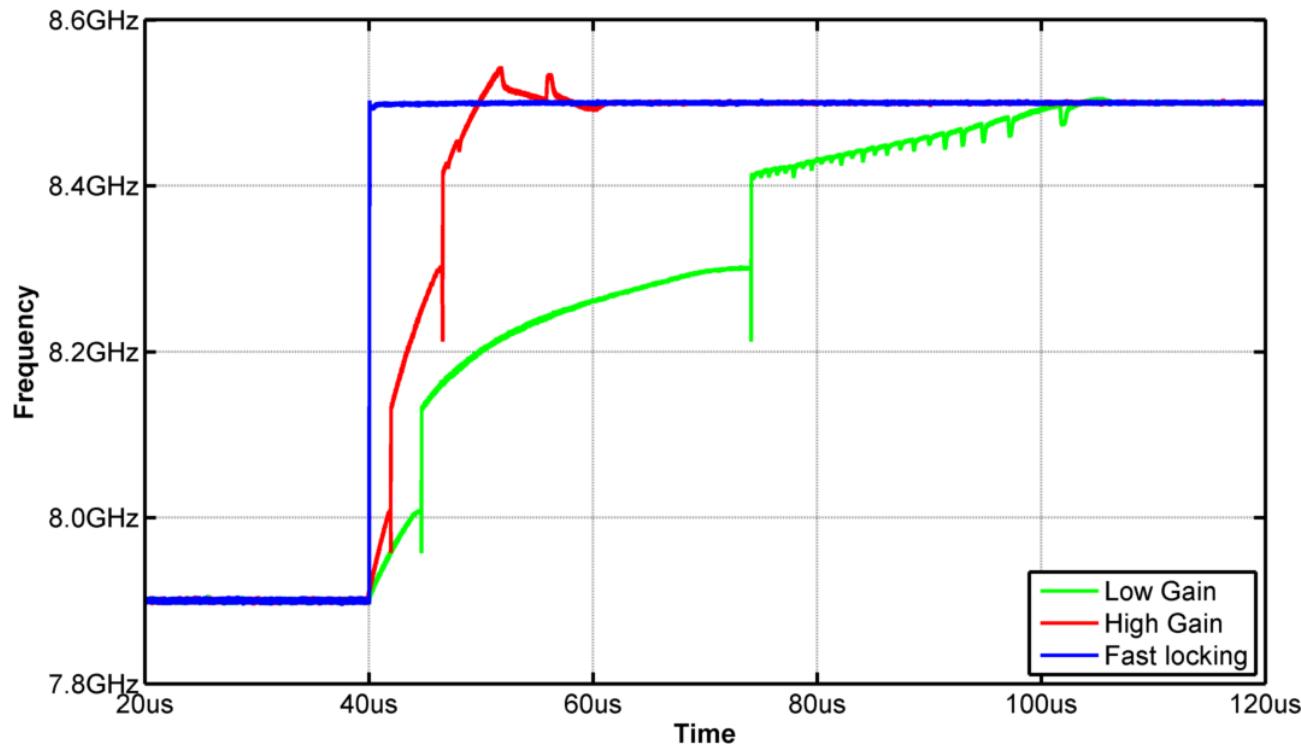


Background calibration engine finds the optimum setting

Dual D/VCO Tuning Characteristic



Transient Locking



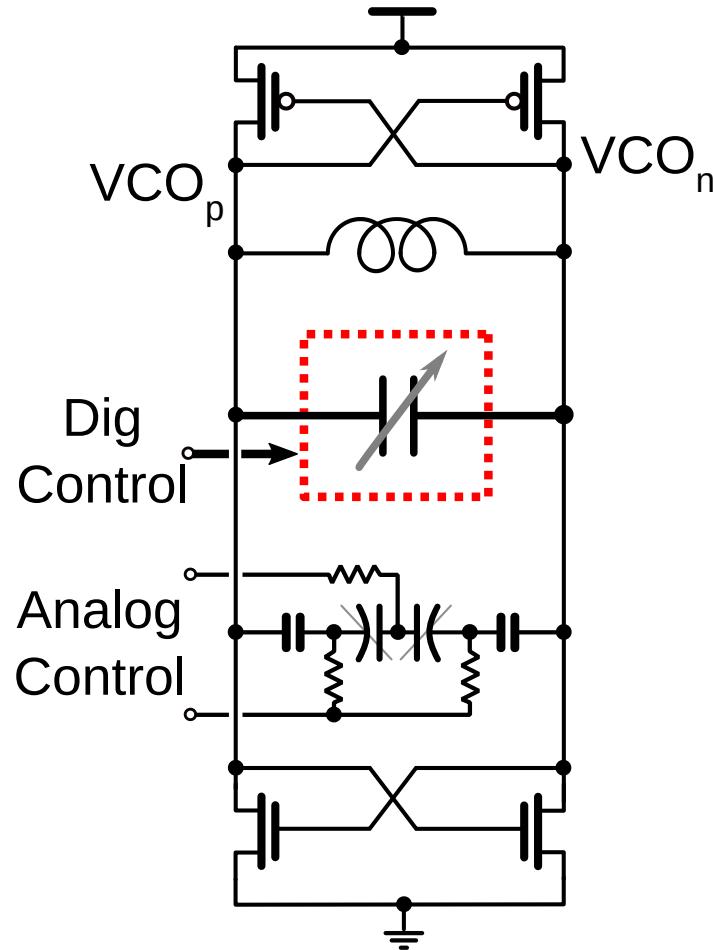
Response to step in division ratio measured with sampling scope.

Measured with different integral path gain settings (green, red), and with direct loading of digital control word (blue).

Varactor Folding

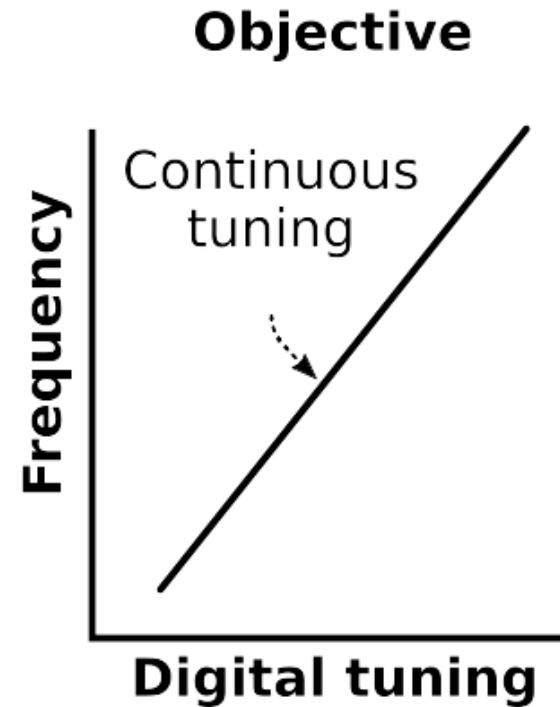
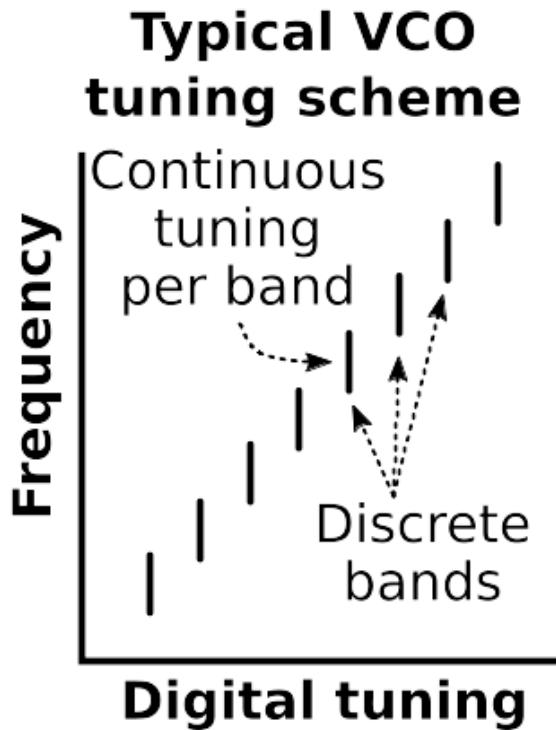
Ferriss, M.; Sadhu, B.; Rylyakov, A.; Ainspan, H.; Friedman, D.,
“A 12-to-26GHz fractional-N PLL with dual continuous tuning LC-D/VCOs,”
IEEE International Solid-State Circuits Conference (ISSCC), 2016.

Oscillator Frequency Control

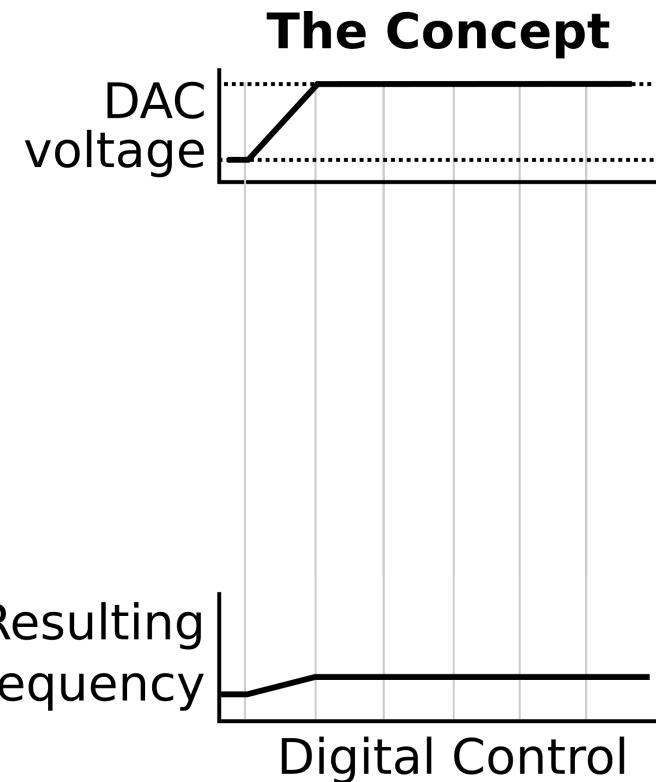
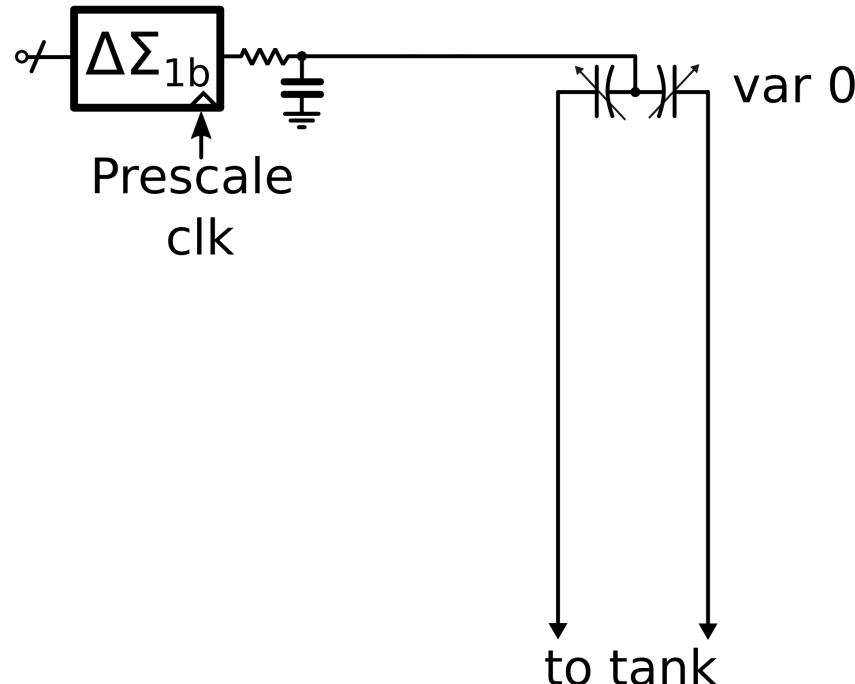


Motivation

- Objective: Remove coarse bands of CMOS oscillators
- Utilize entire tuning range to generate frequency chirps

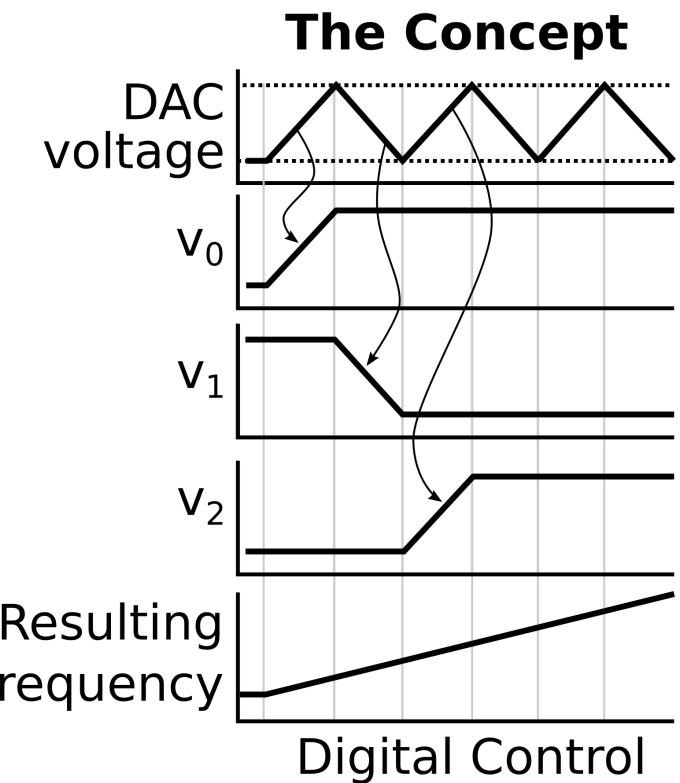
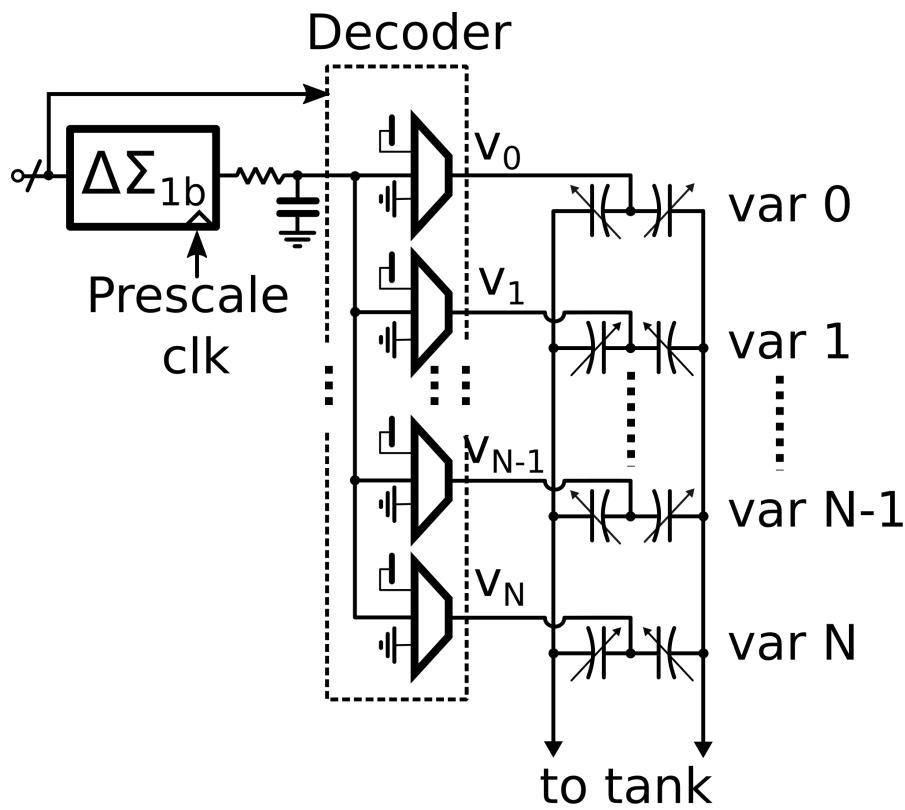


Digital control of a varactor



Trade off between SD noise and Gain/Tuning range

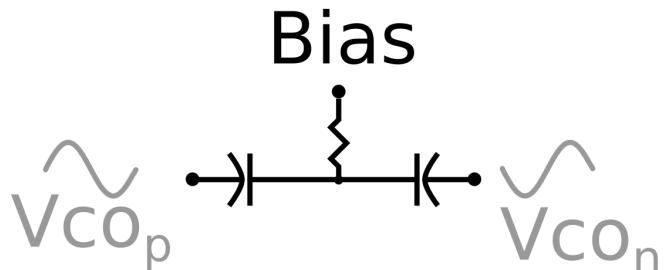
Extending the range: varactor folding



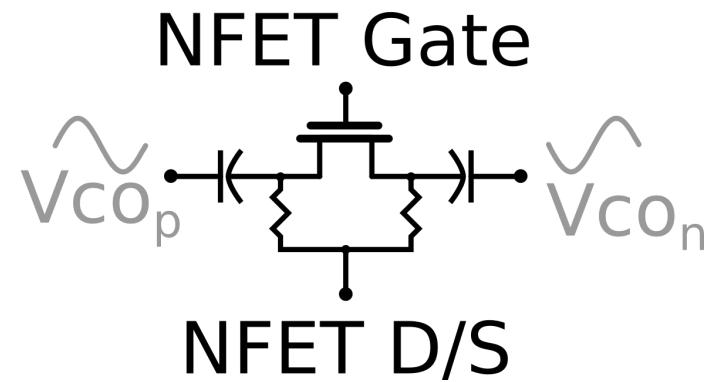
Similar concept used in [P. Wang, et al., JSSC 2009]

Comparing typical tuning mechanisms

Continuous tuning:
Varactor

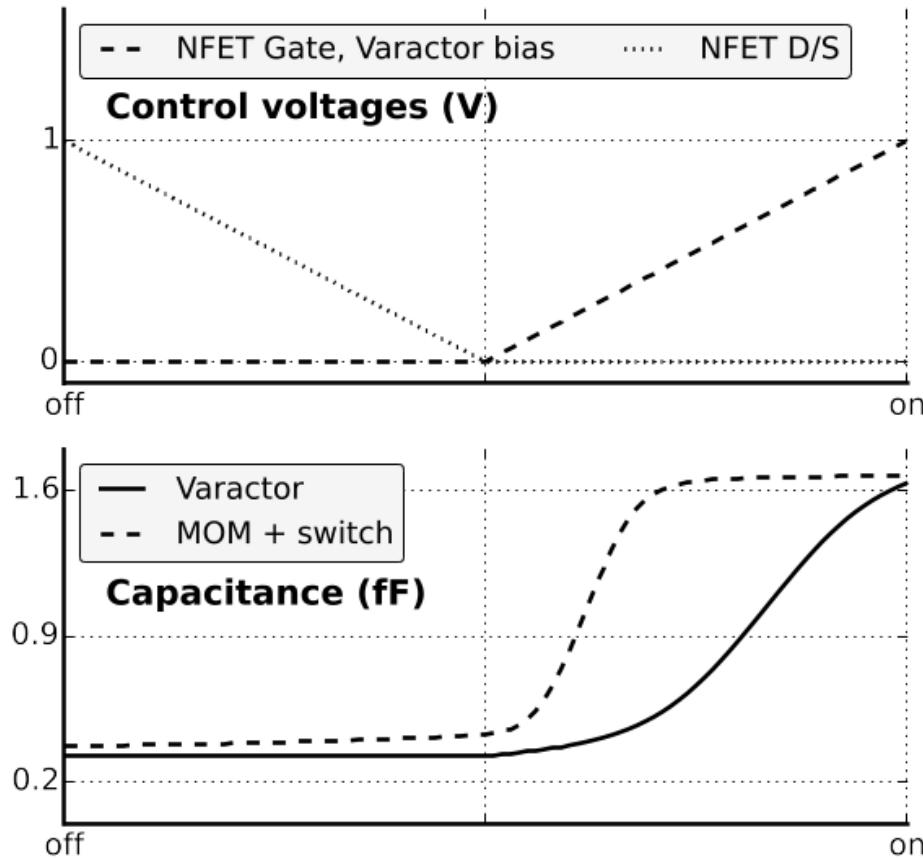


Discrete tuning:
MOM + Switch

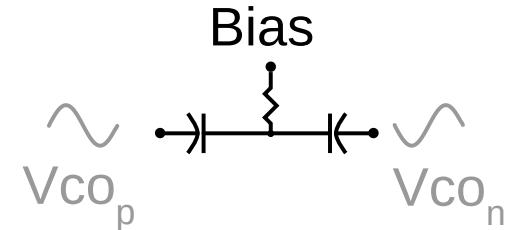


Can we use MOM+switch for continuous tuning?

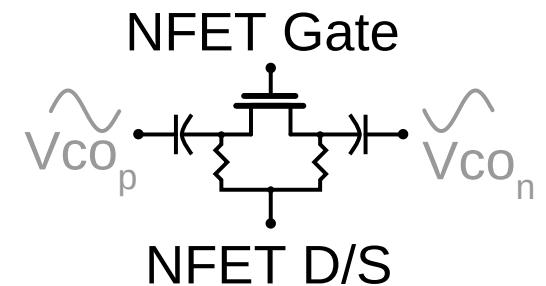
Varactors vs MOM+switch (Cap)



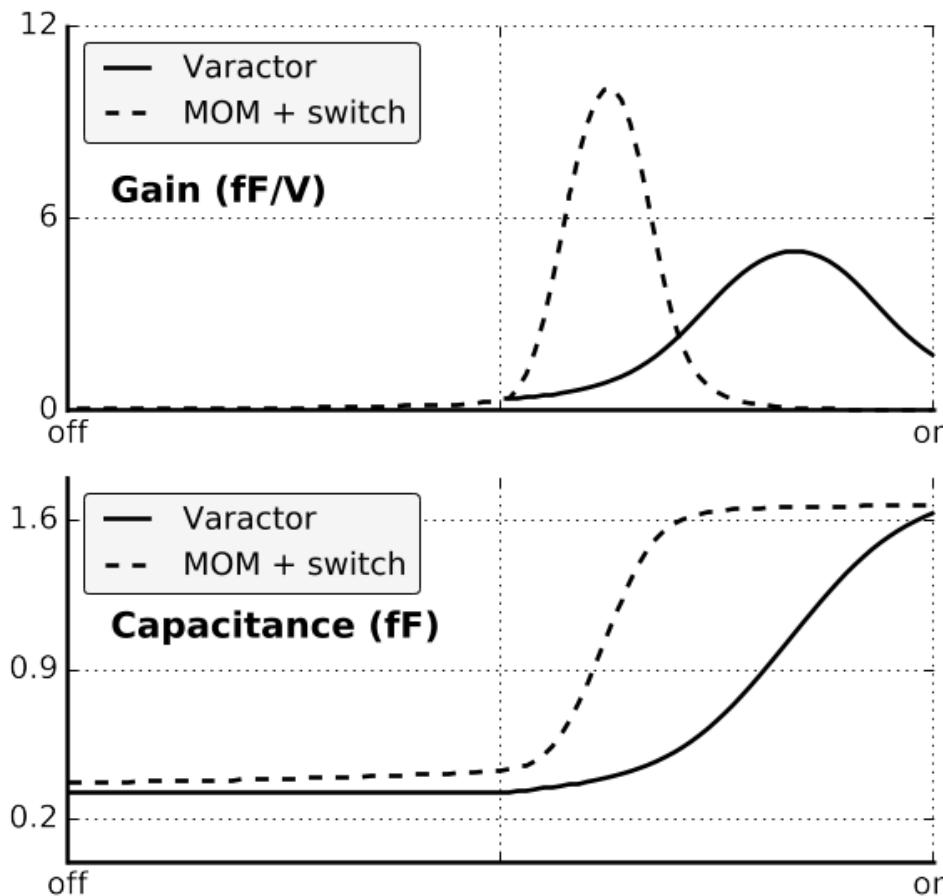
Varactor



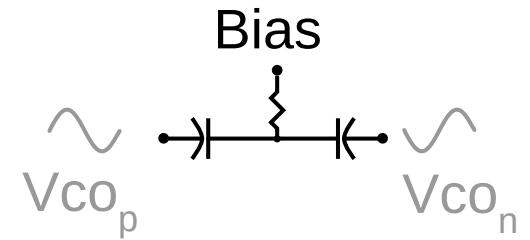
MOM + Switch



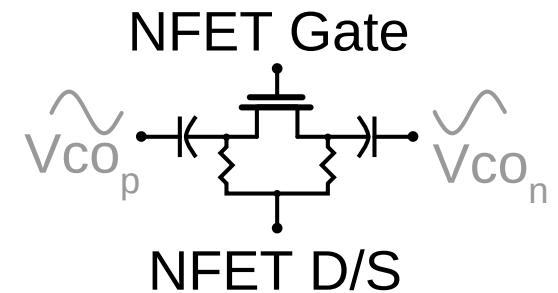
Varactors vs MOM+switch (Gain)



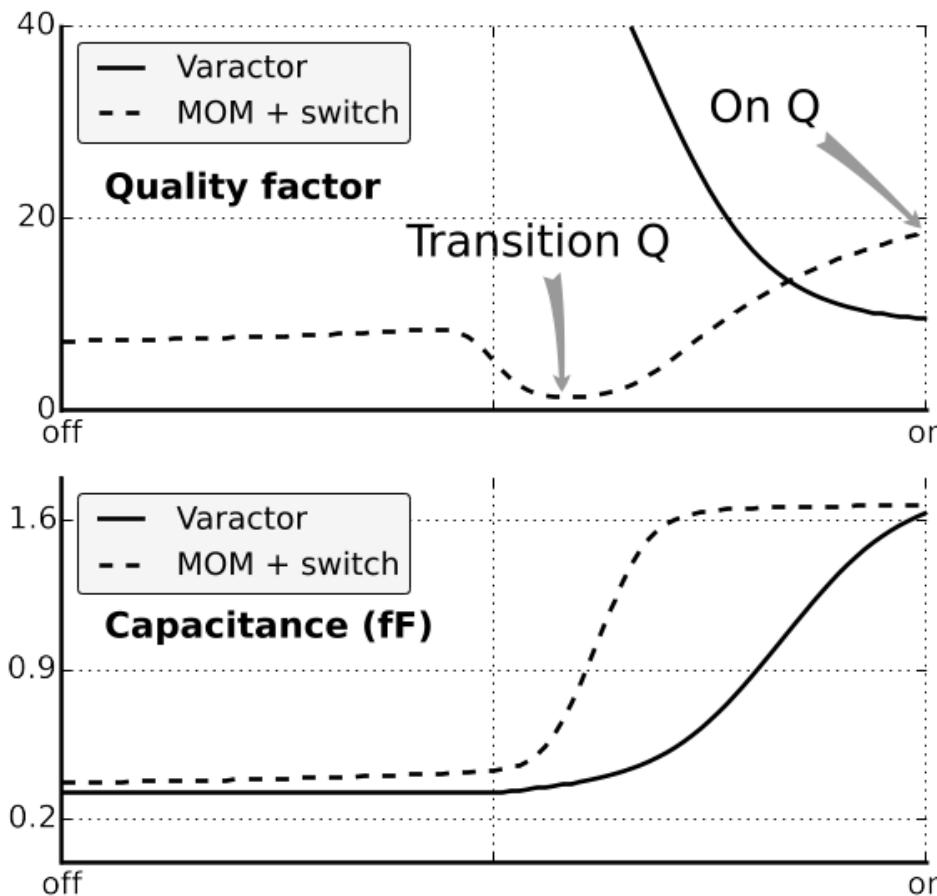
Varactor



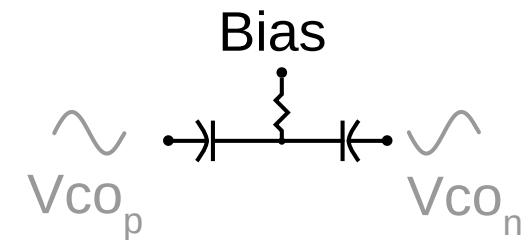
MOM + Switch



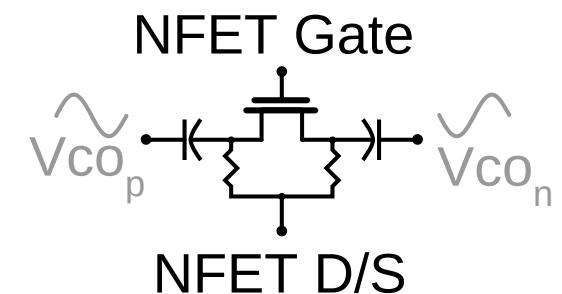
Varactors vs MOM+switch (Q)



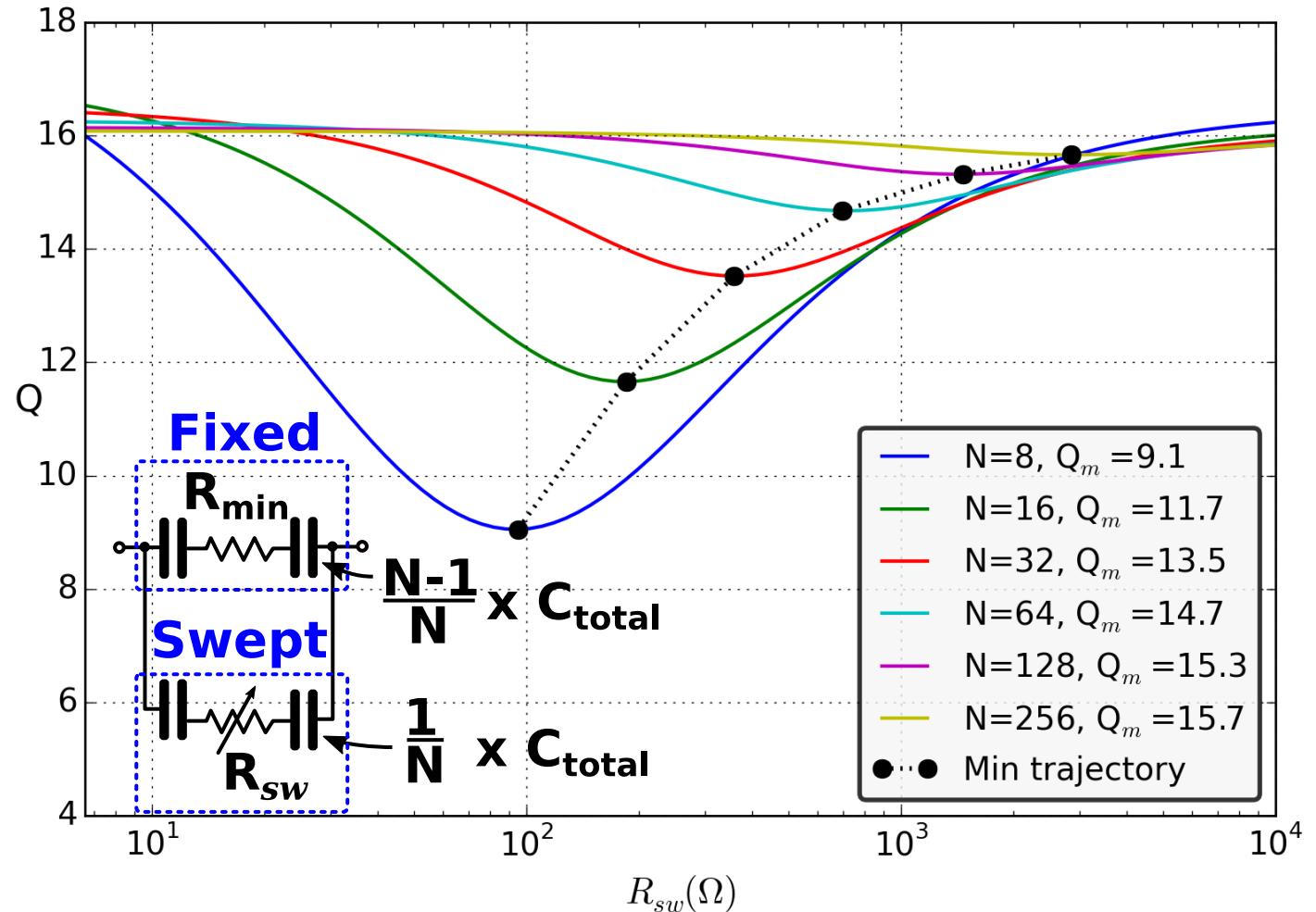
Varactor



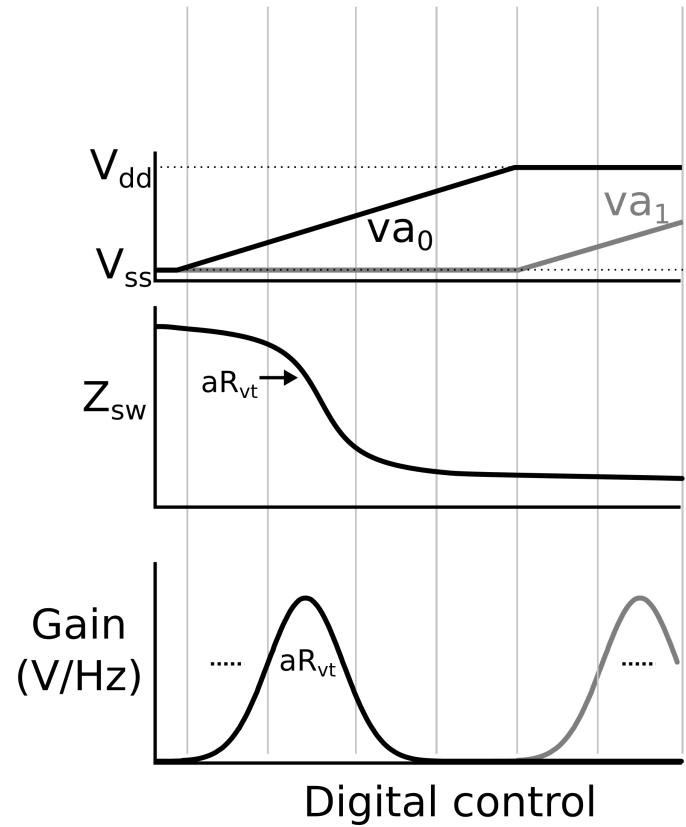
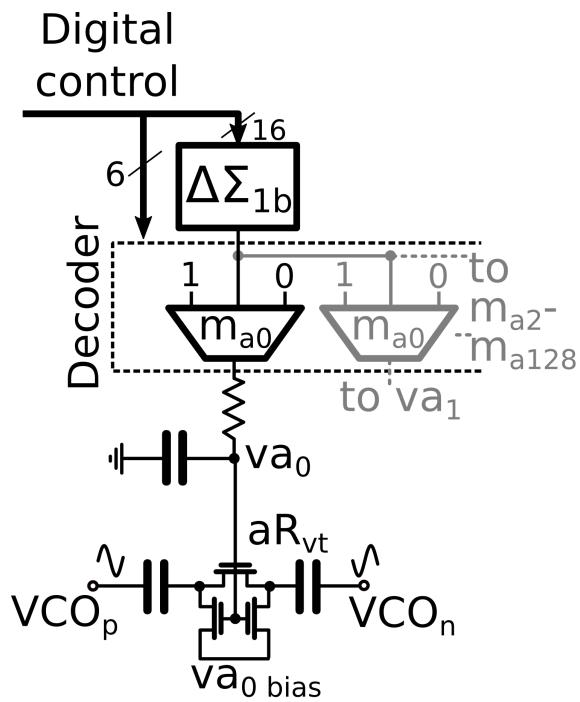
MOM + Switch



Q degradation versus # of elements

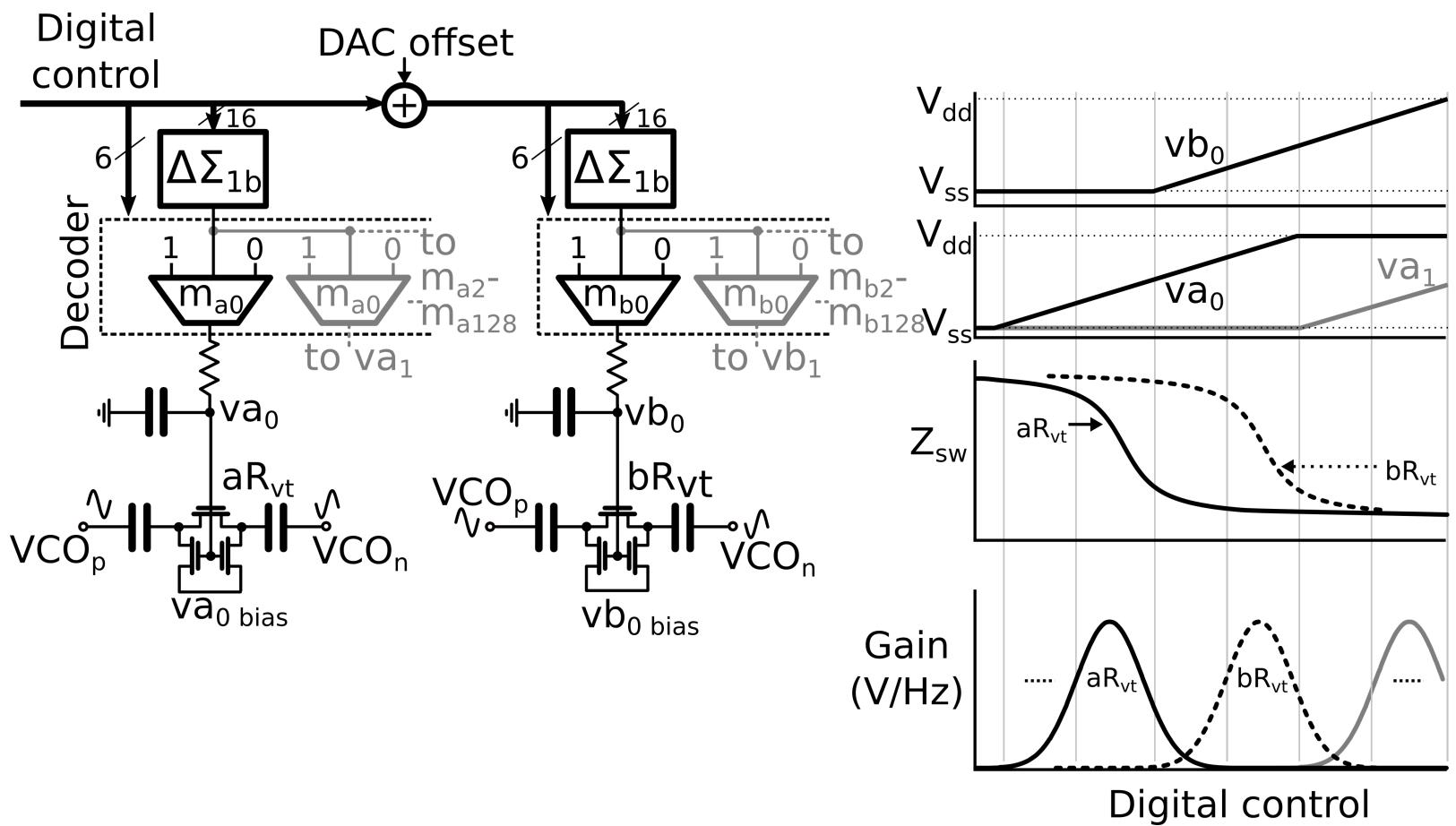


Single band



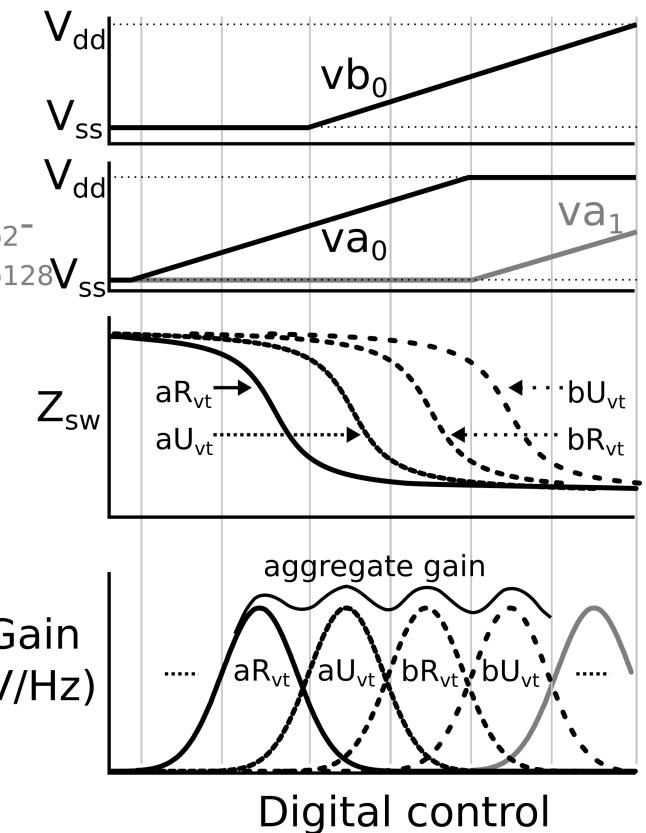
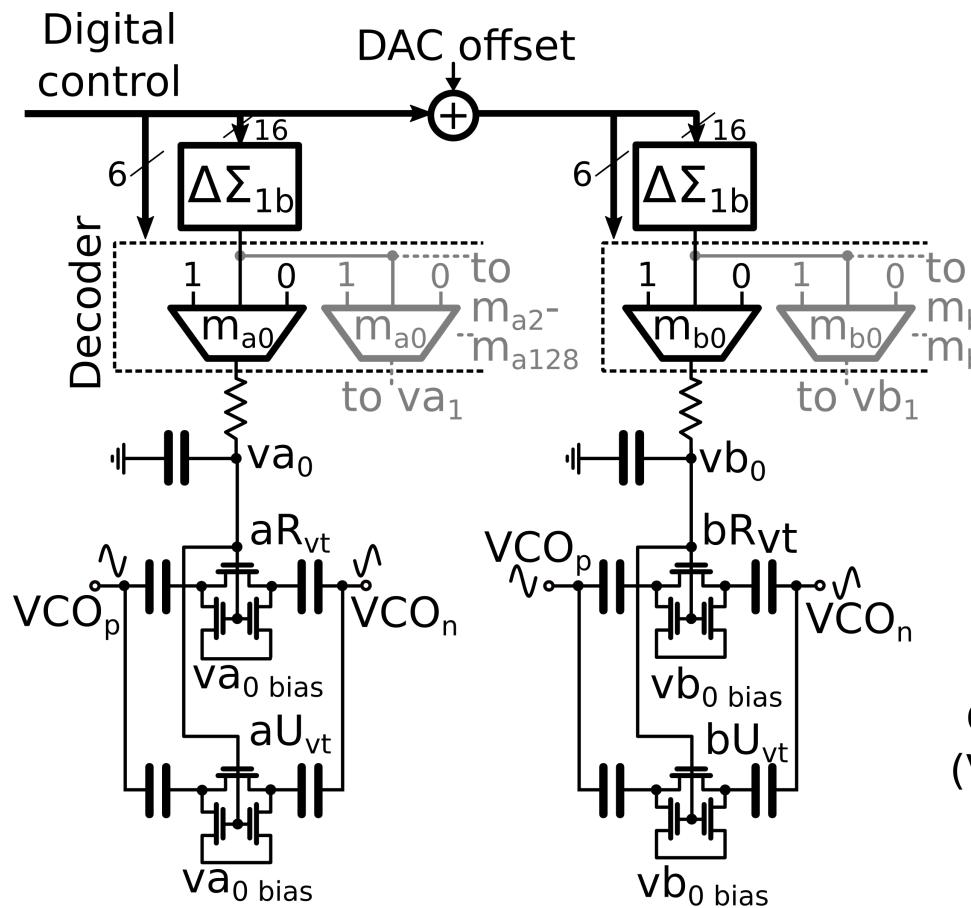
*Connections for va_0 bias omitted for simplicity

Two bands with offset



*Connections for v_{a_0} bias, v_{b_0} bias omitted for simplicity

Two bands and two thresholds

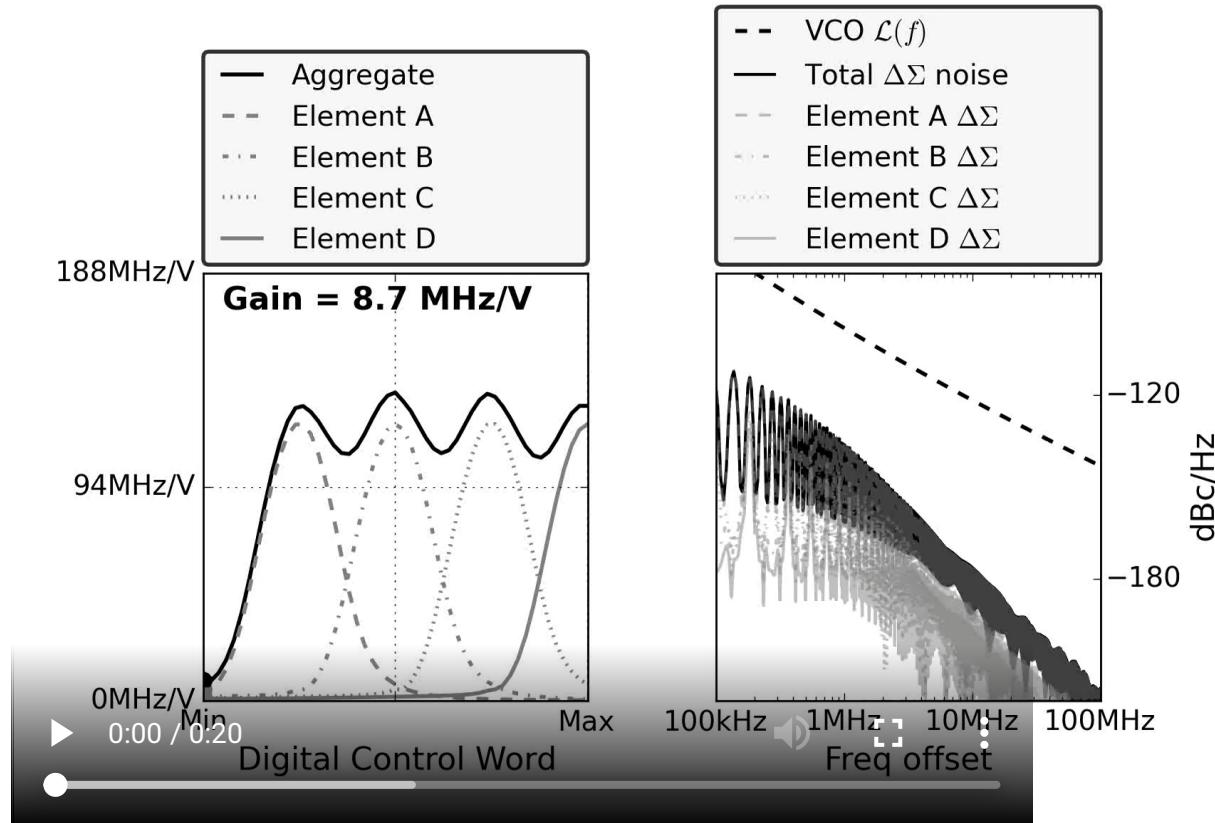


*Connections for va_0 bias, vb_0 bias omitted for simplicity

Varactor gain versus frequency

In [1]:

```
%%HTML
<div align="middle"><video width="100%" controls><source src="Inkscape/Folding/m
edialb.m4v" type="video/mp4"></video>
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Patent contains a few alternative configurations

U.S. Patent

Apr. 24, 2018

Sheet 10 of 14

US 9,954,486 B2

FIG. 15

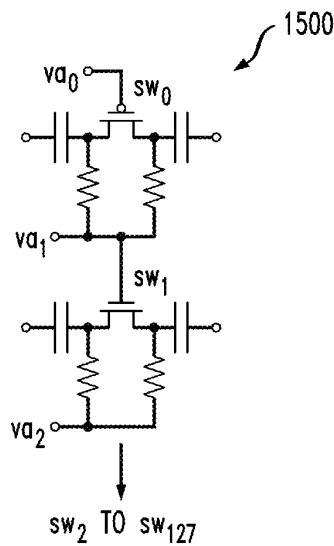
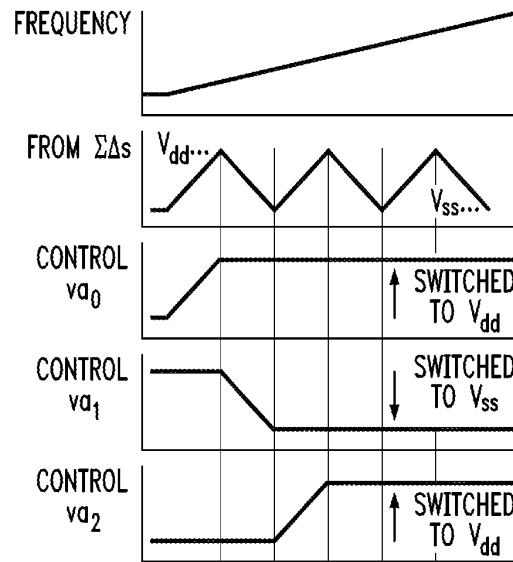
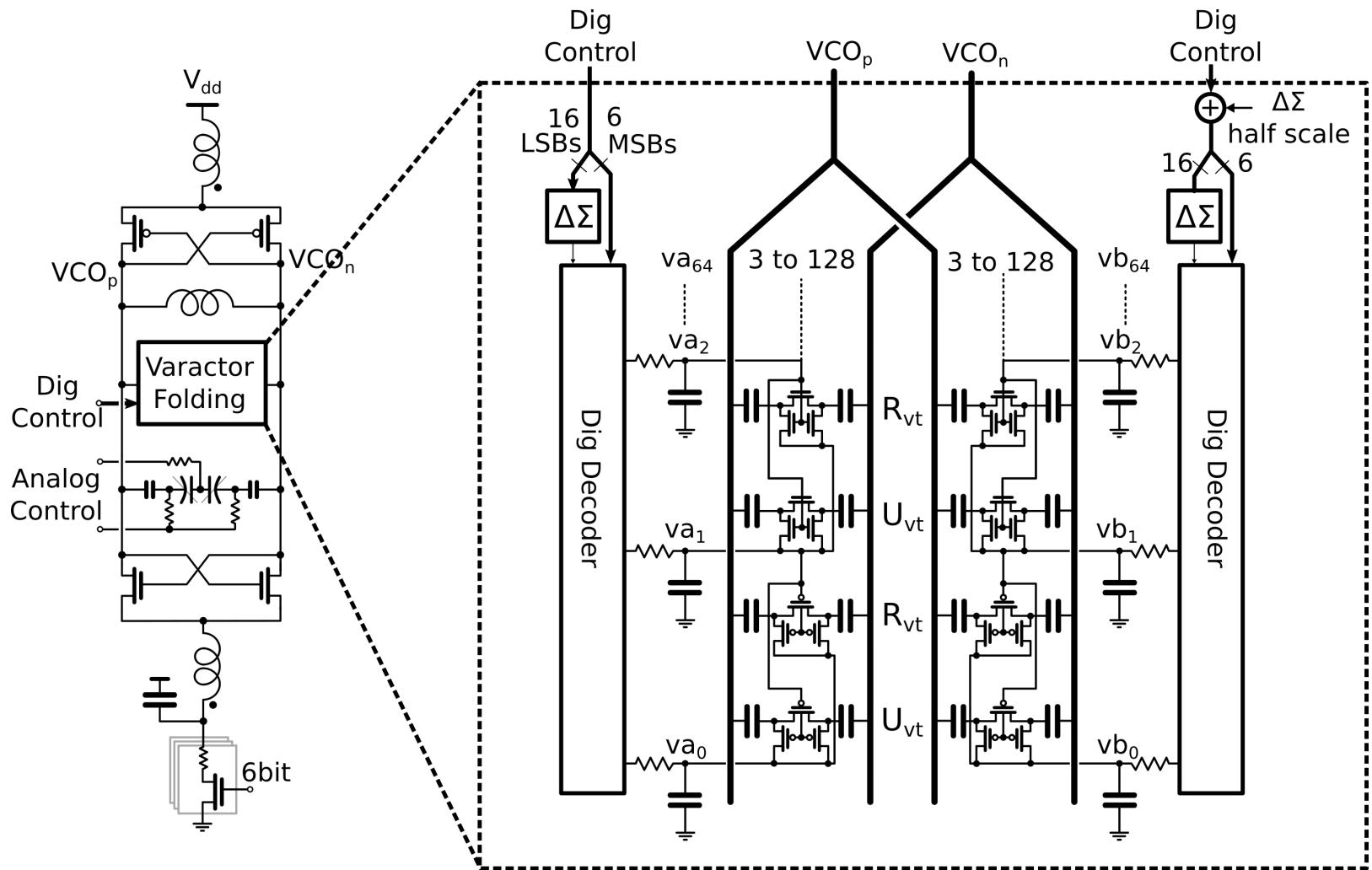


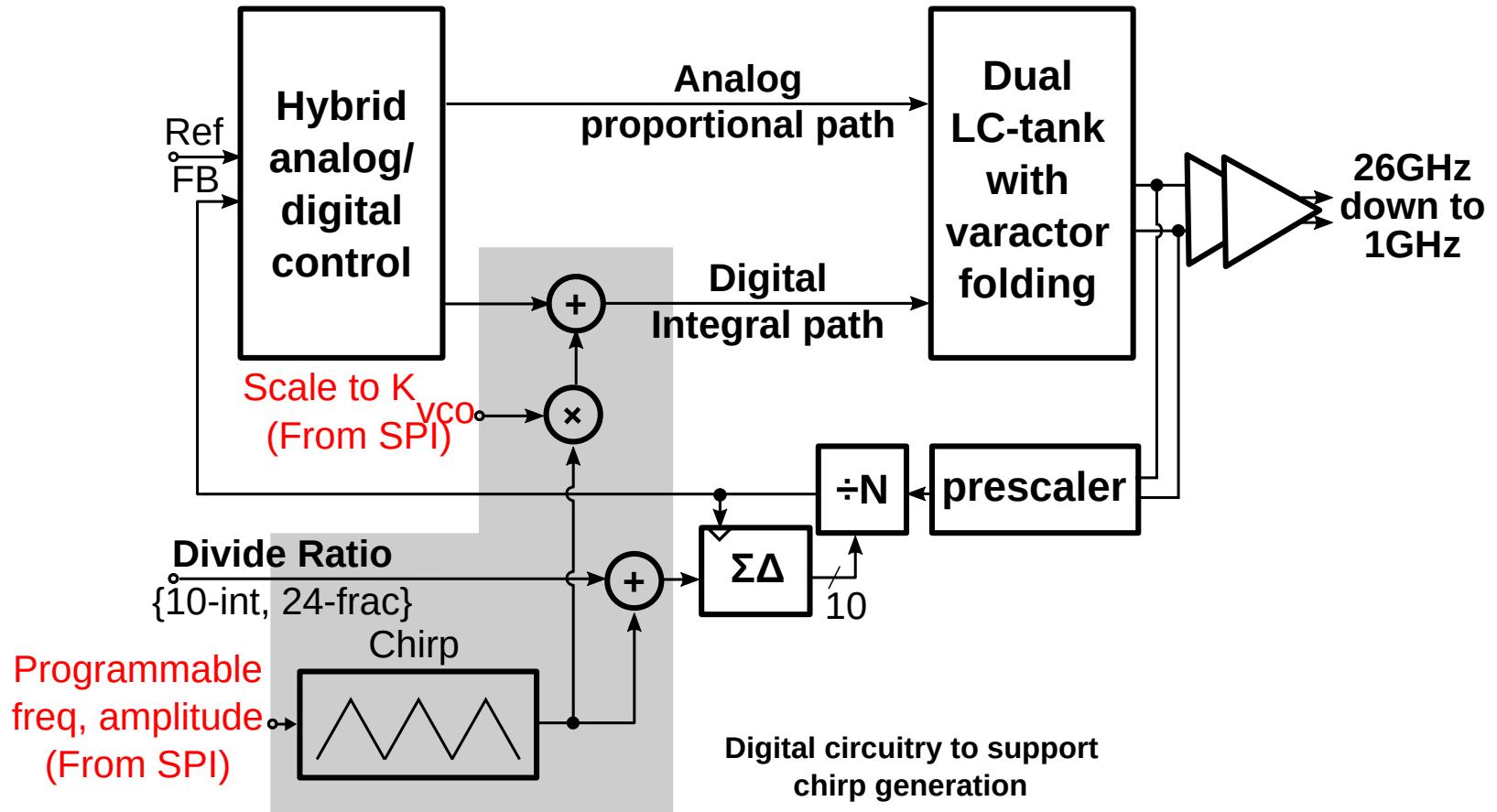
FIG. 16



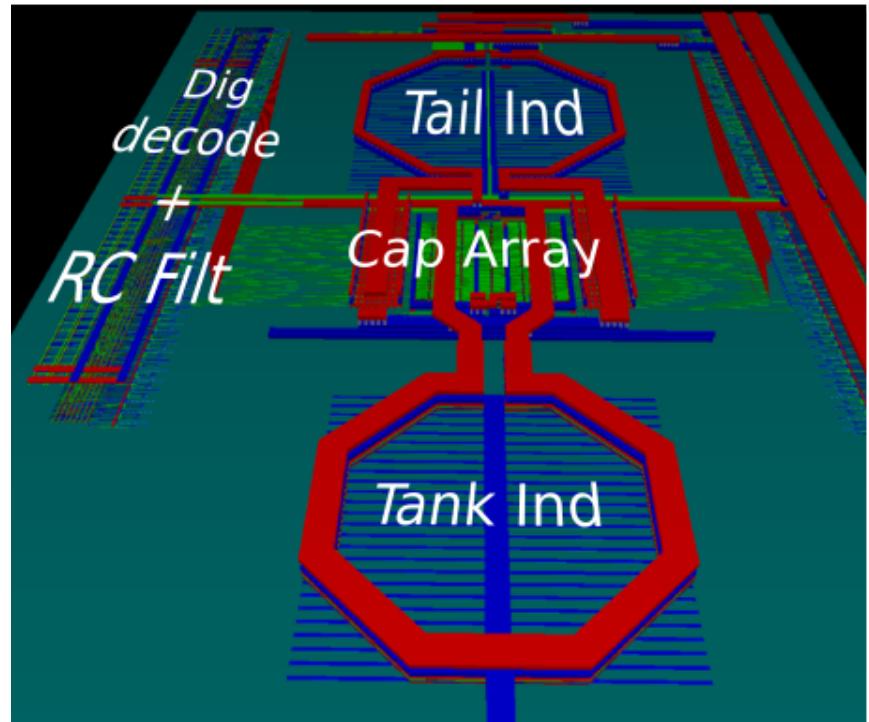
The VCO



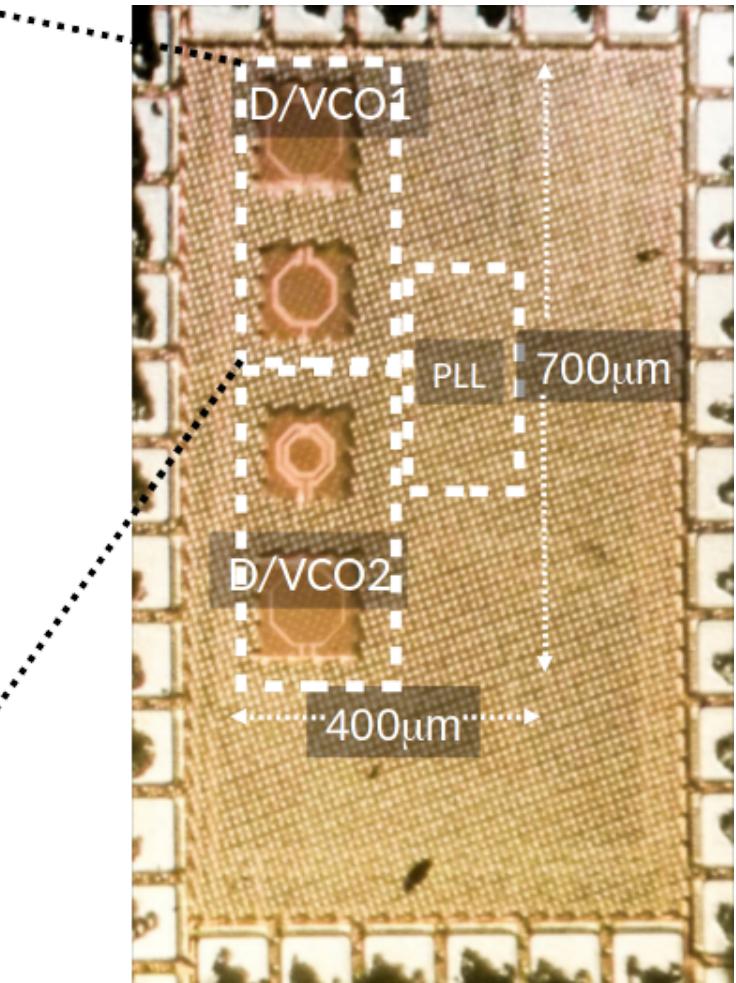
PLL architecture



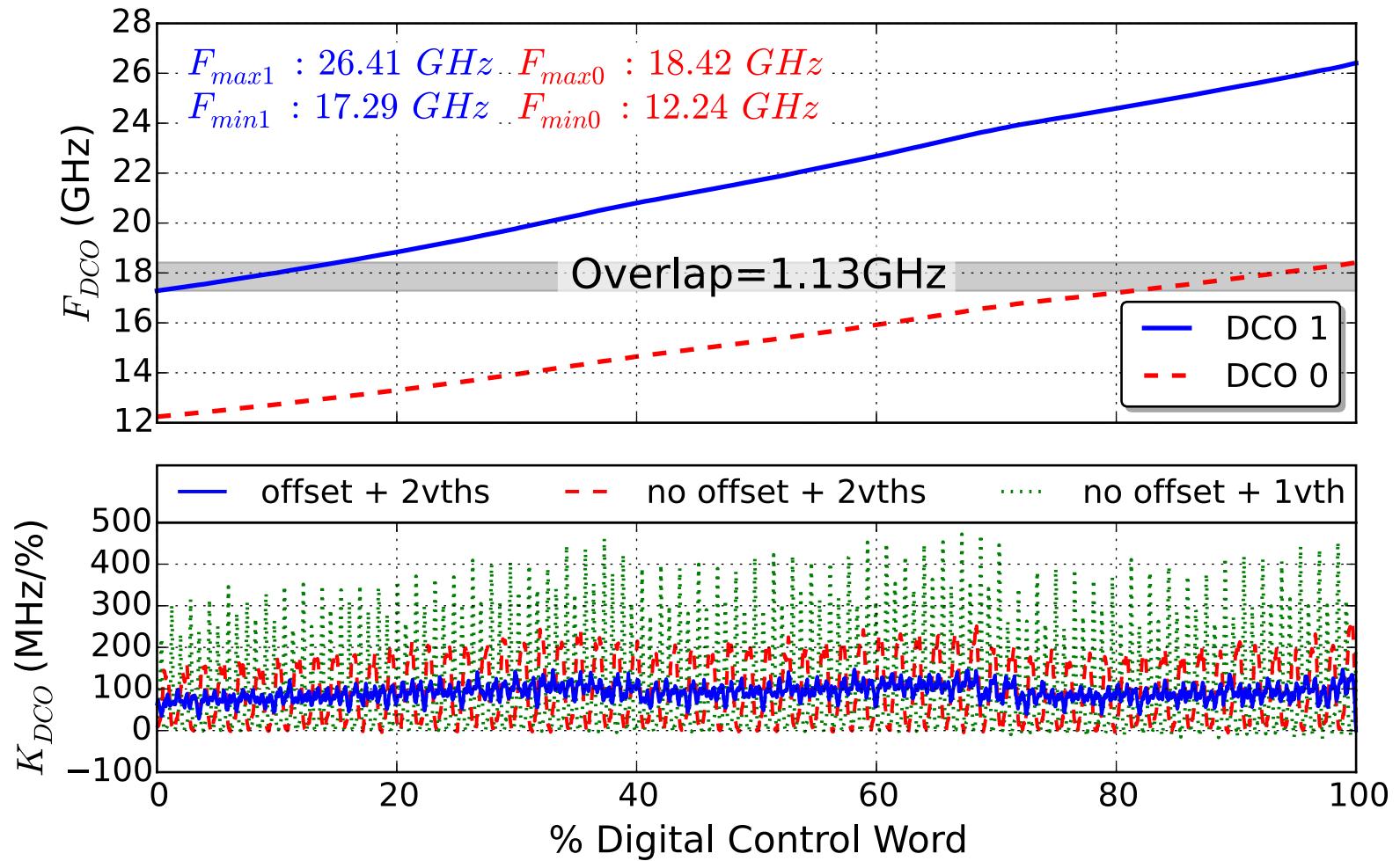
32nm CMOS prototype



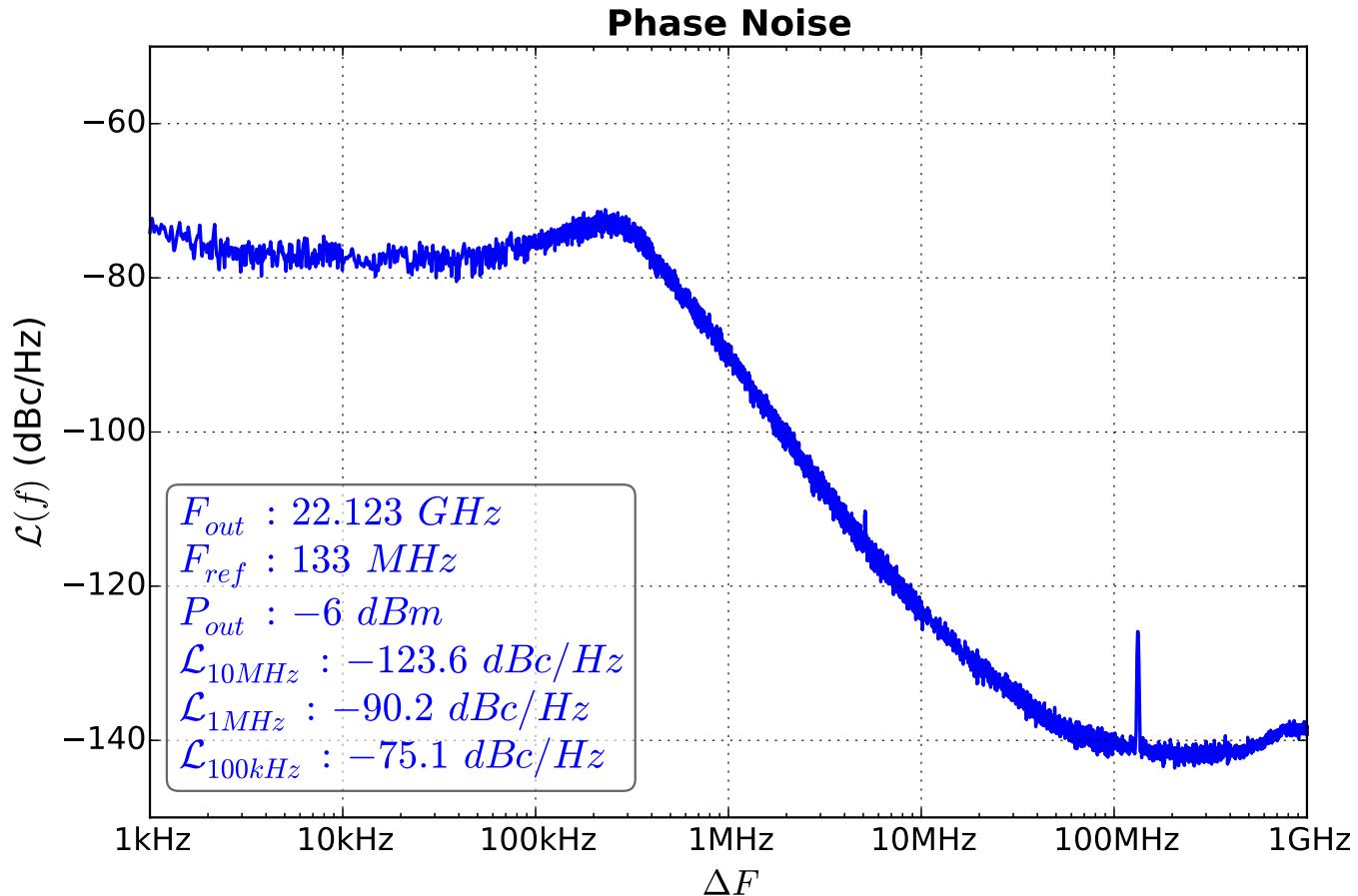
Visualization with GDS3D



Measured tuning range

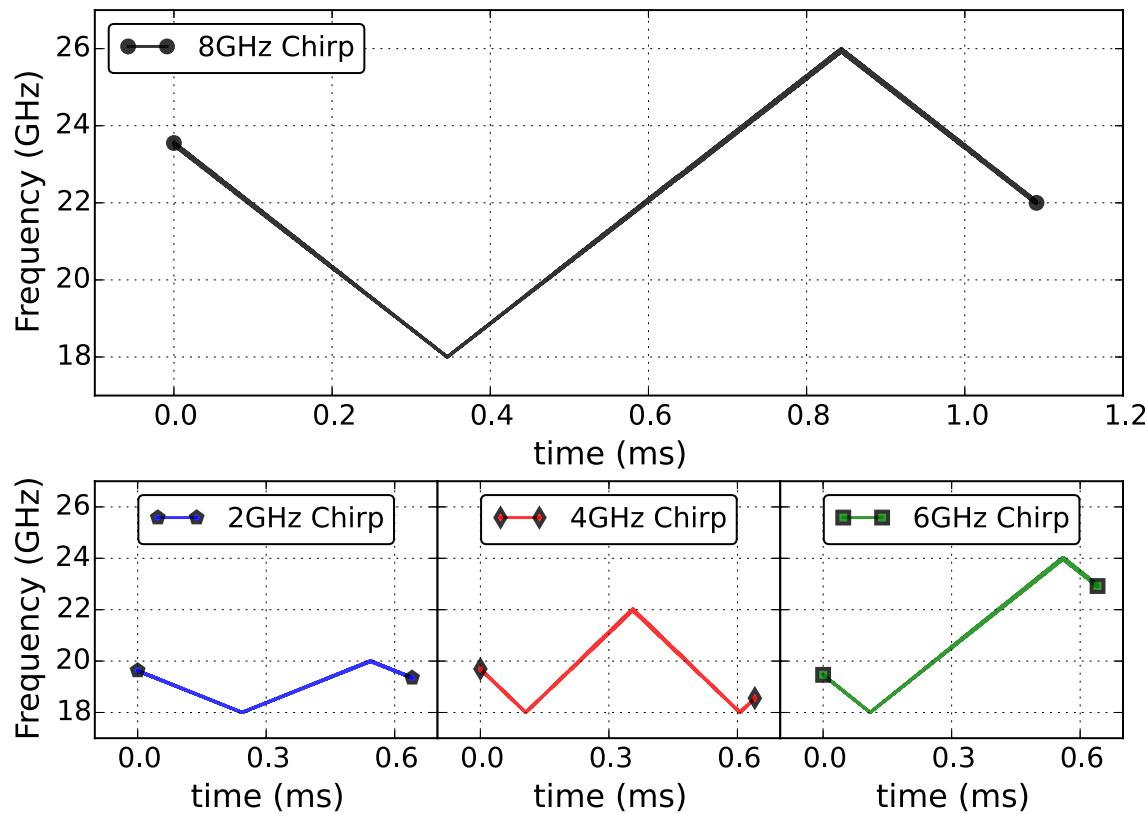


Measured phase noise



VCO's FOM = 181dBc/Hz, FOMT = 188dBc/Hz @10MHz offset

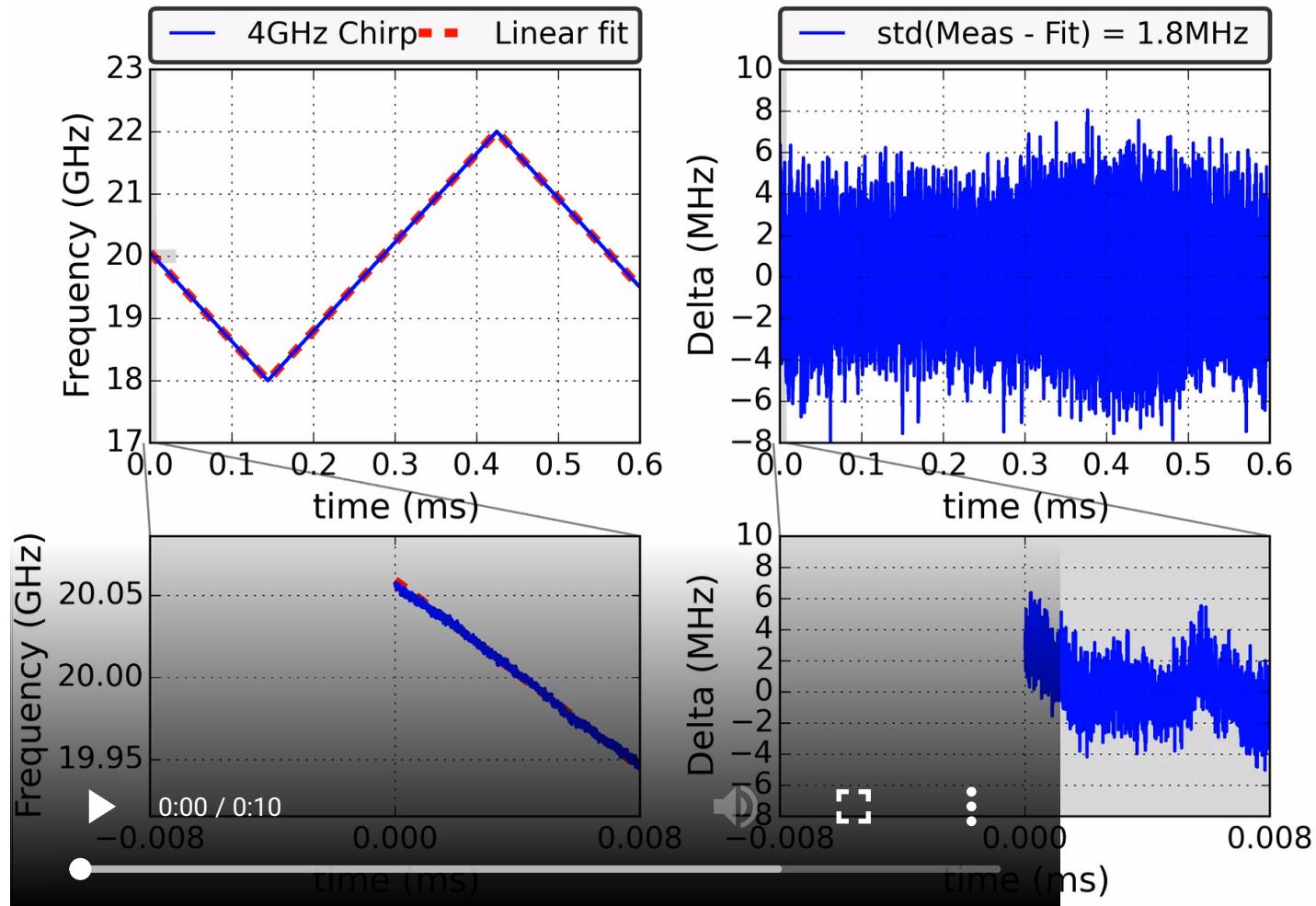
Transient frequency measured with 80GHz oscilloscope



In [3]:

%%HTML

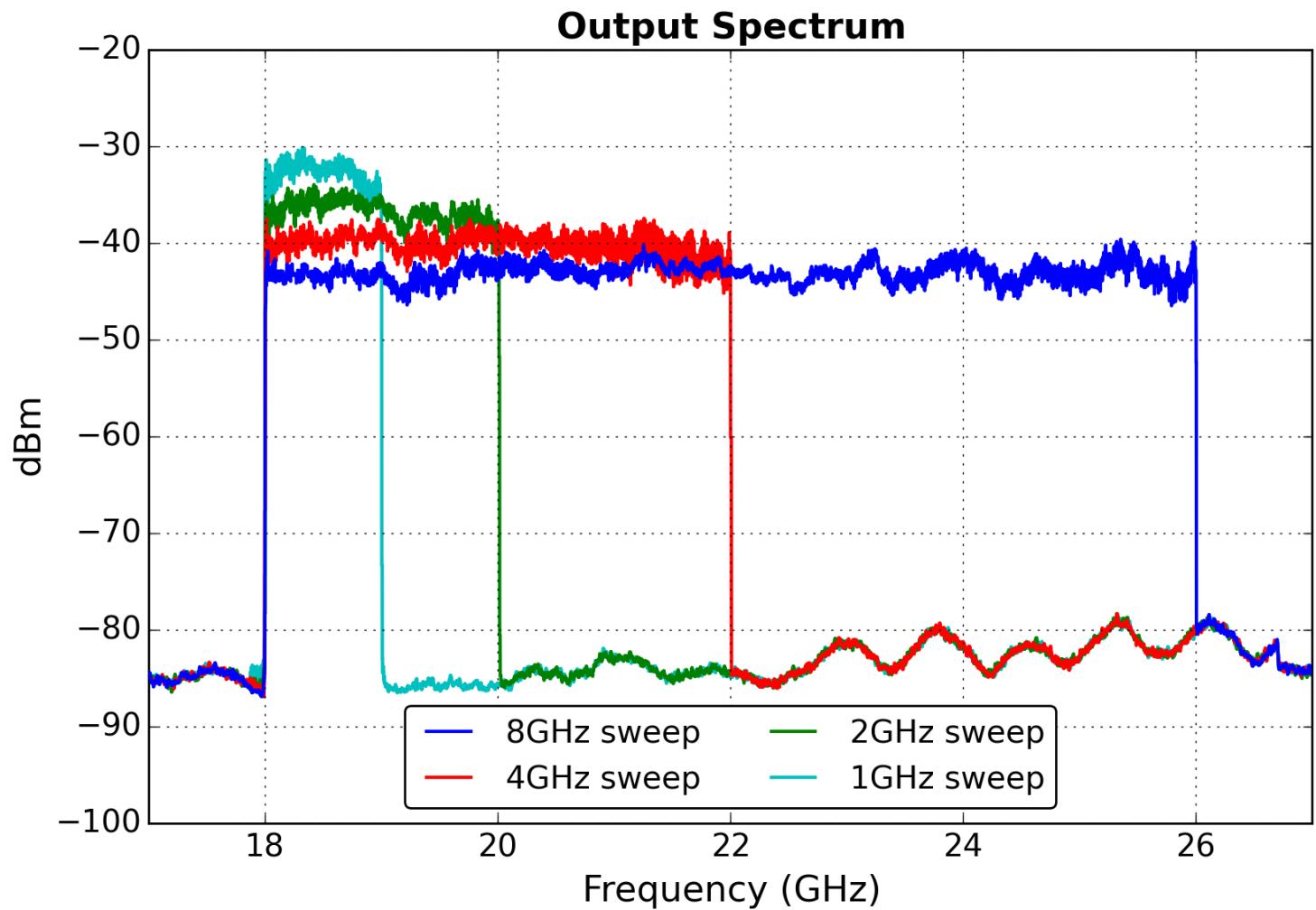
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Chirp generation comparison

	This work	JSSC 14 W. Wu, et al.	ISSCC 11 H. Sakurai, et al.	JSSC 10 T. Mitomo, et al.	ISSCC 10 Y.-A. Li, et al.
Total PLL range (GHz)	12.3-26.4[†]	56.4-63.4	82.1-83.8	78.1-78.8	75.6-76.3
Phase noise (dBc/Hz)	-124 @ 10MHz from 22GHz	-90 @ 1MHz from 60GHz	-84 @ 1MHz from 82GHz	-120 @ 10MHz from 78GHz	-85 @ 10MHz from 76GHz
PN normalized to 10Mz offset from 22GHz*	-124	-119*	-116*	-130*	-115*
Chirp freq. range (GHz)	8GHz	1GHz	1.5GHz	0.6GHz	0.7GHz
Modulation slope (GHz/ ms)	11.4	4.76	1.5	1.2	0.5

Spectrum when generating chirps



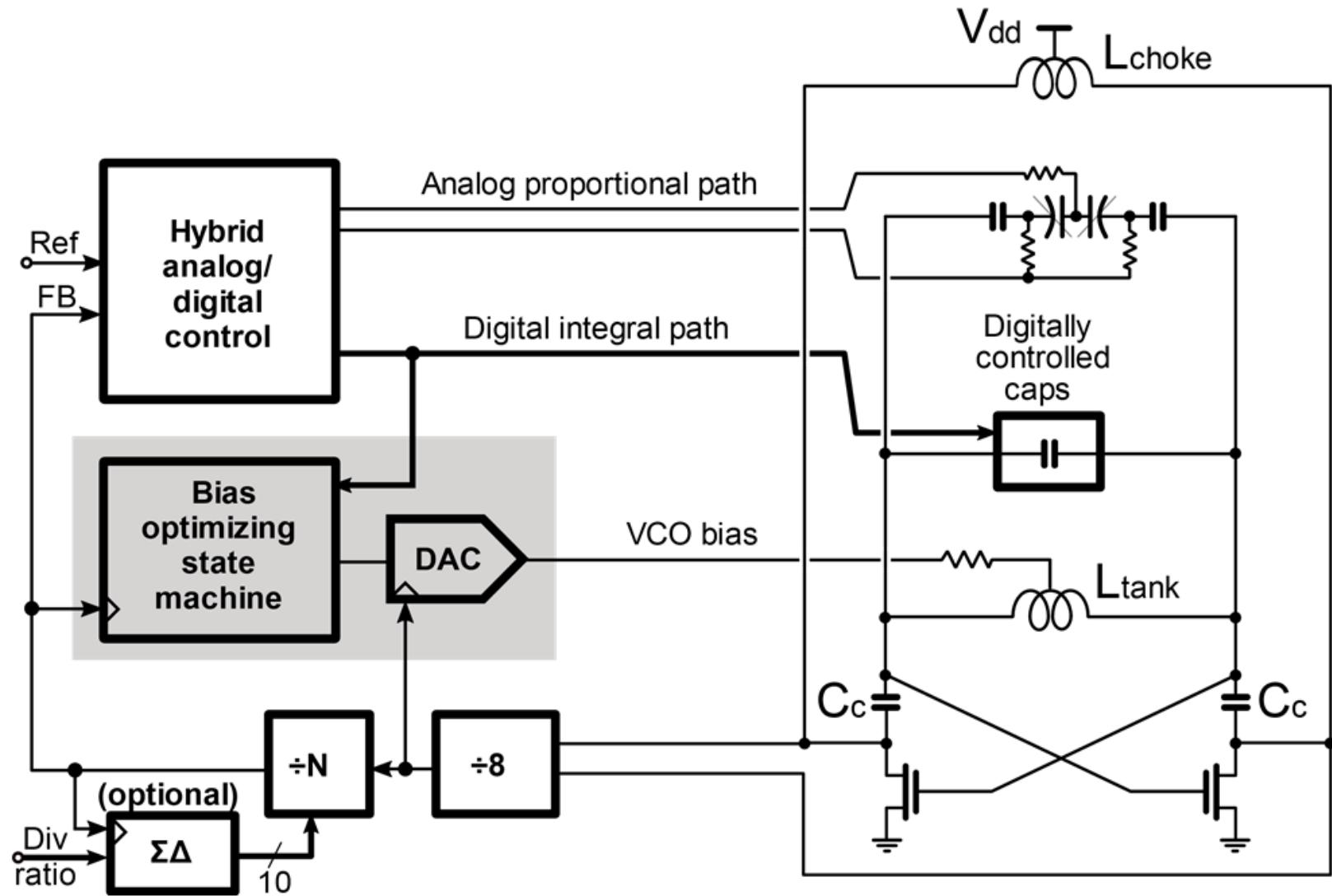
Flicker noise suppression in VCOs

Ferriss, M.; Sadhu, B.; Friedman, D.;

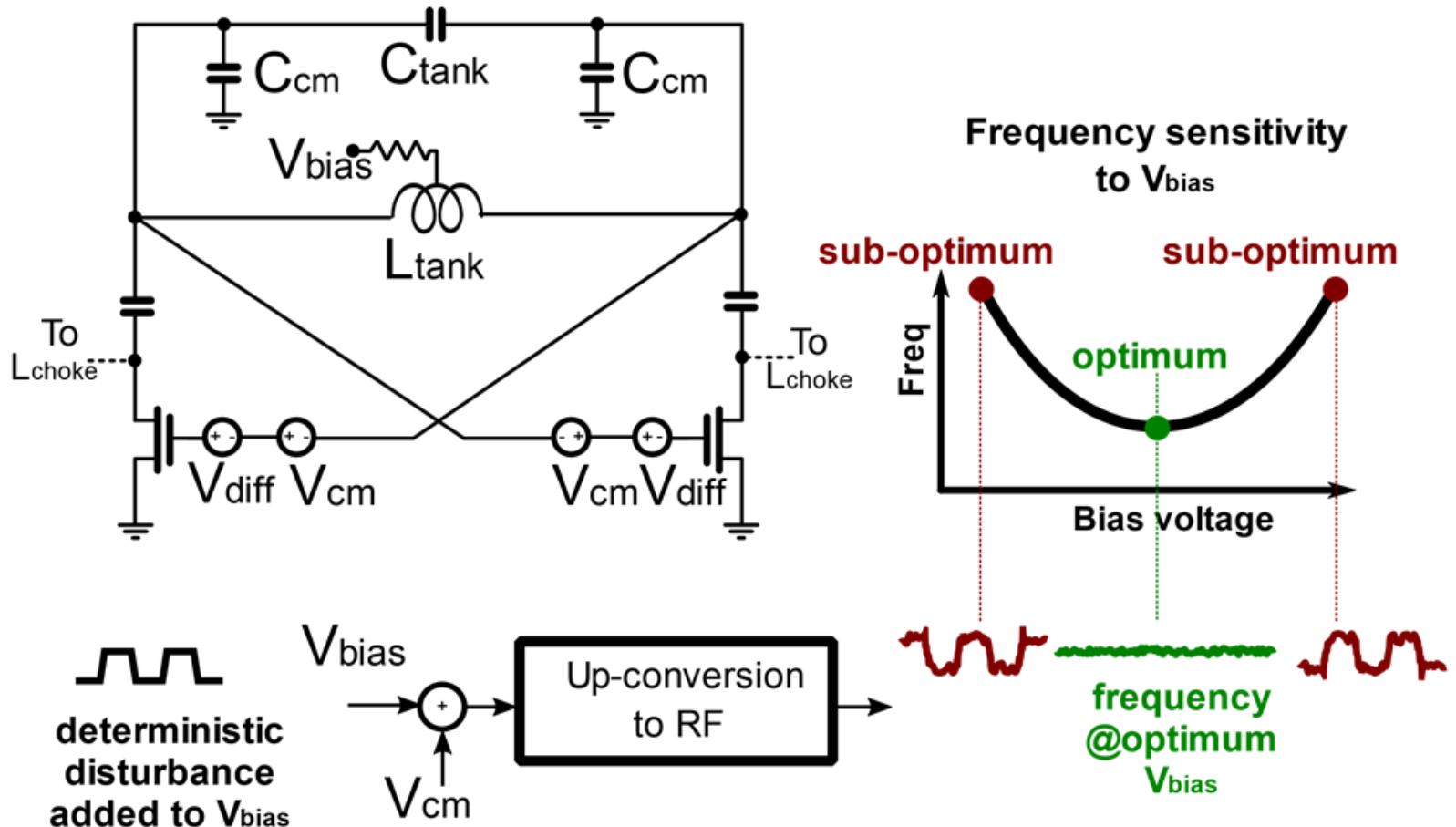
"A Gradient Descent Bias Optimizer for Oscillator Phase Noise Reduction Demonstrated in 45nm and 32nm SOI CMOS,"

IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2018.

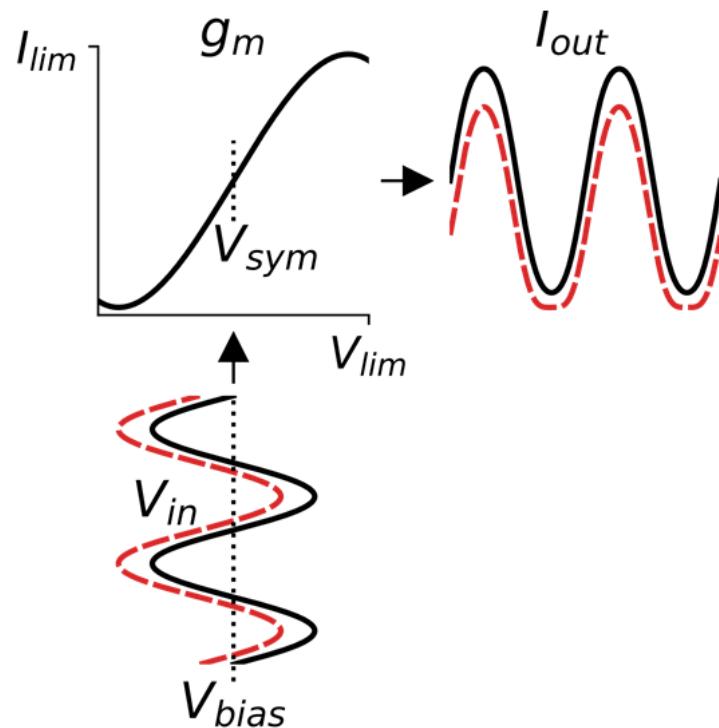
Overview of architecture



Oscillator sensitivity to noise

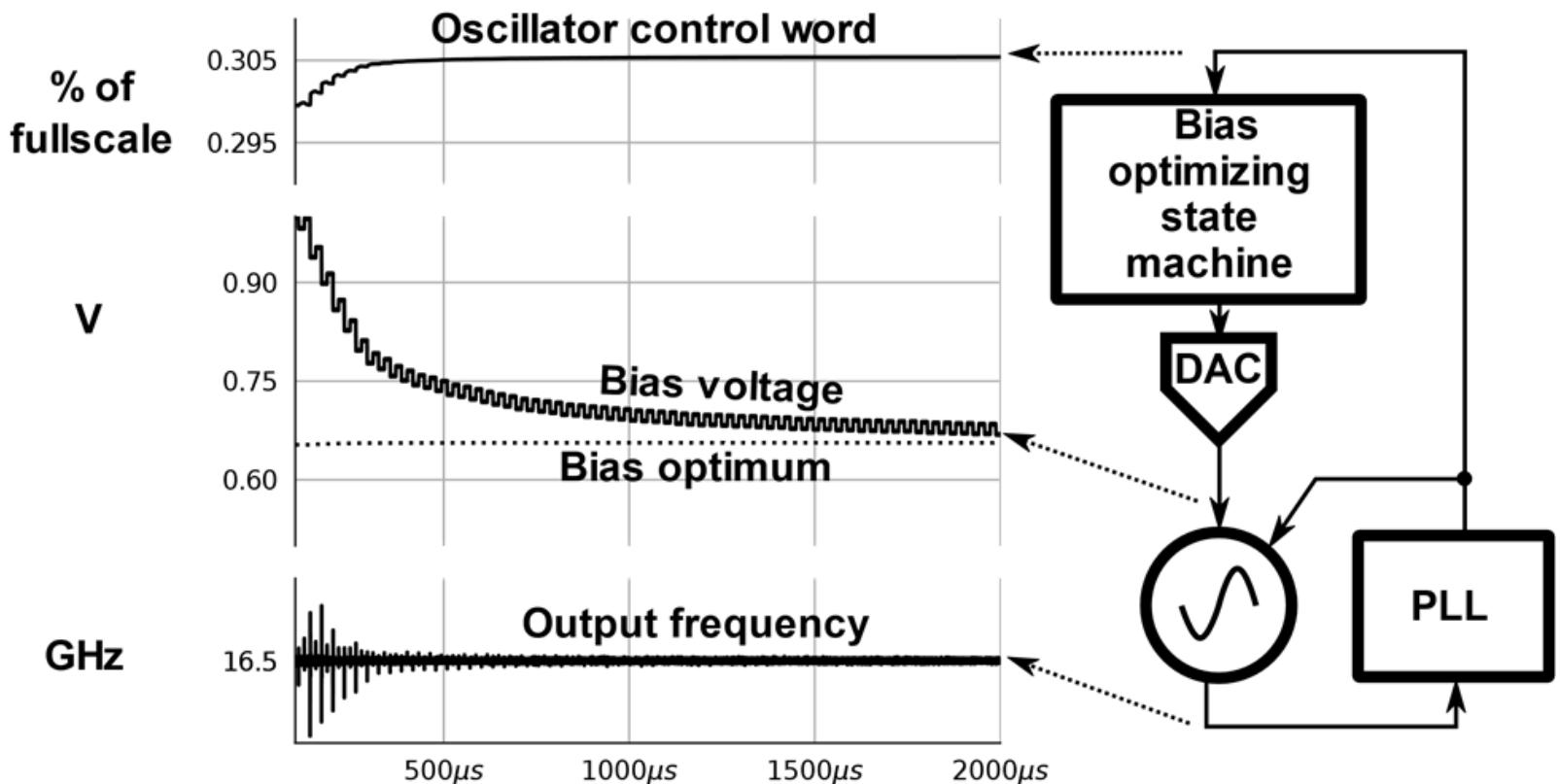


Transconductance

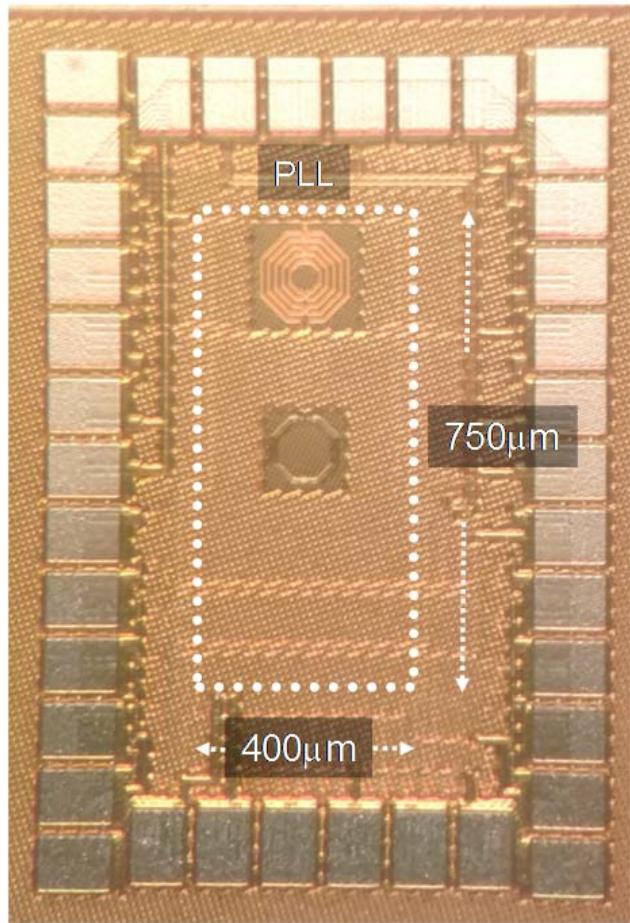


Transconductor with odd I-V characteristic => no up-conversion from DC to phase noise. [Pepe, Andreani TCAS I, 2017]

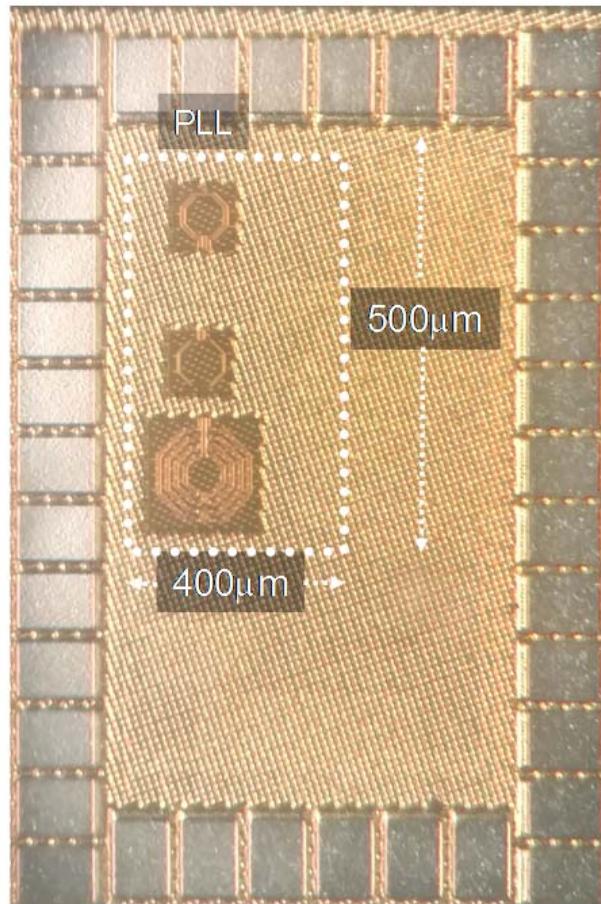
Transient behavioral simulation



Die photos: (a) 45nm, (b) 32nm.

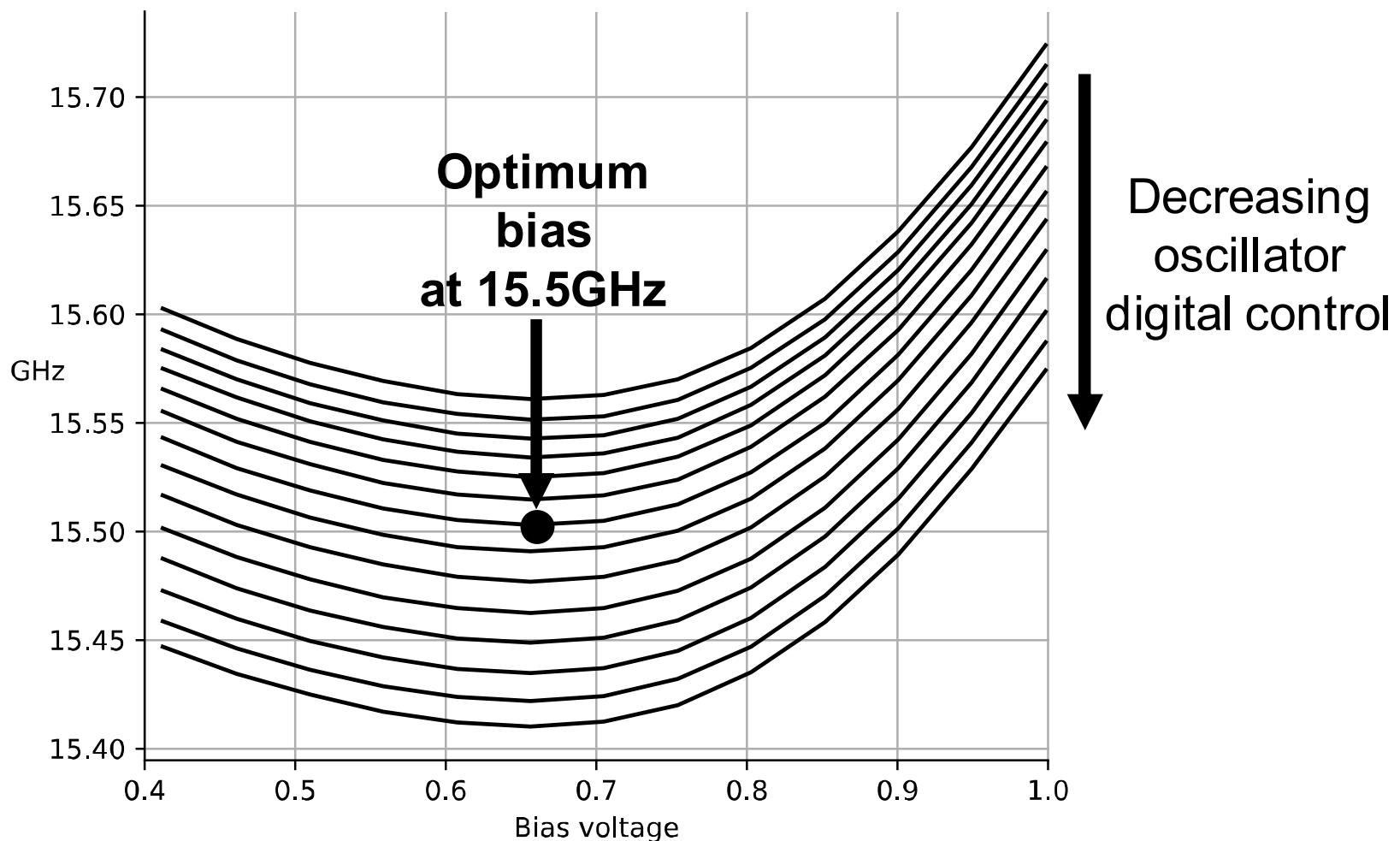


(a)

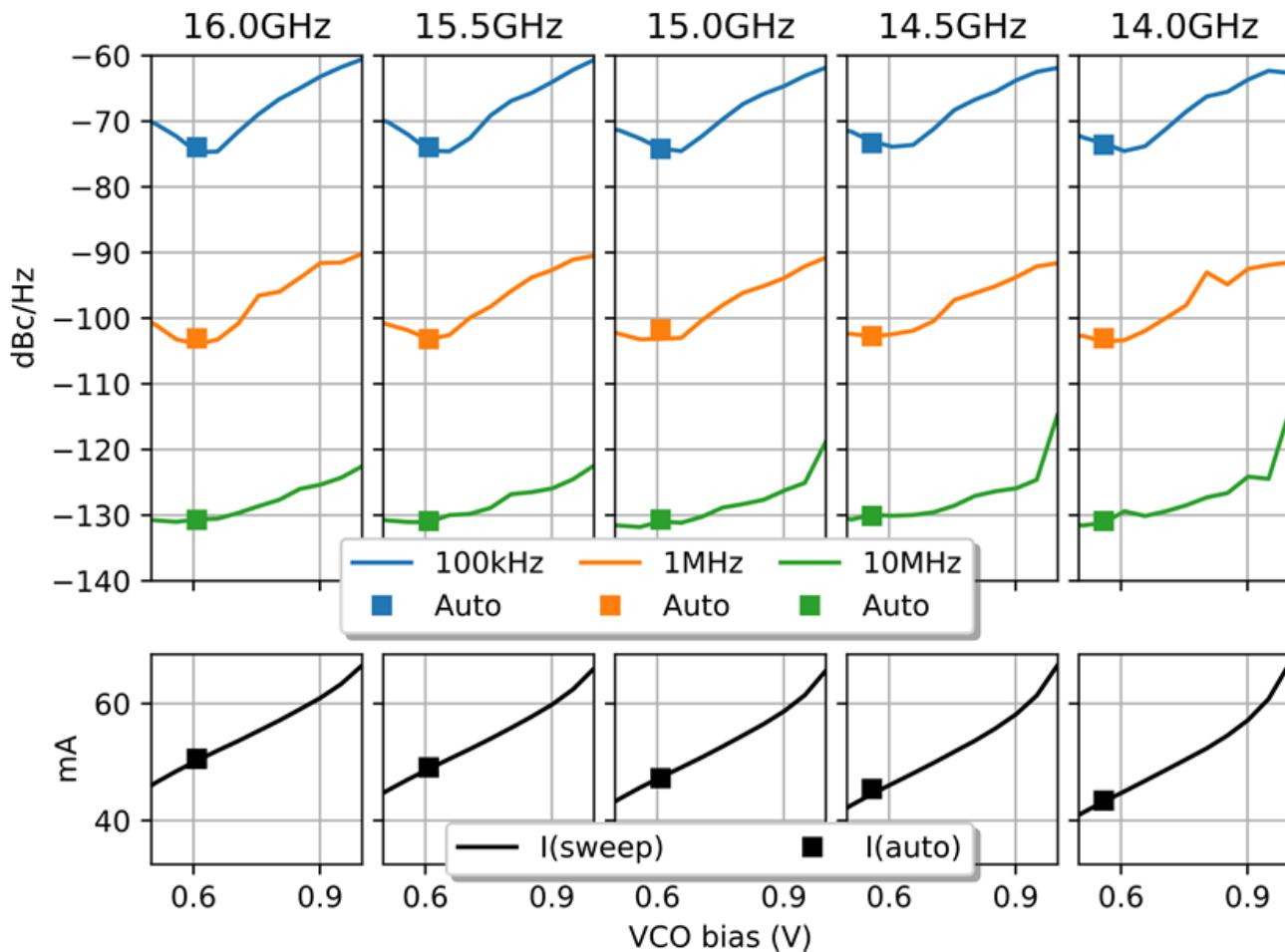


(b)

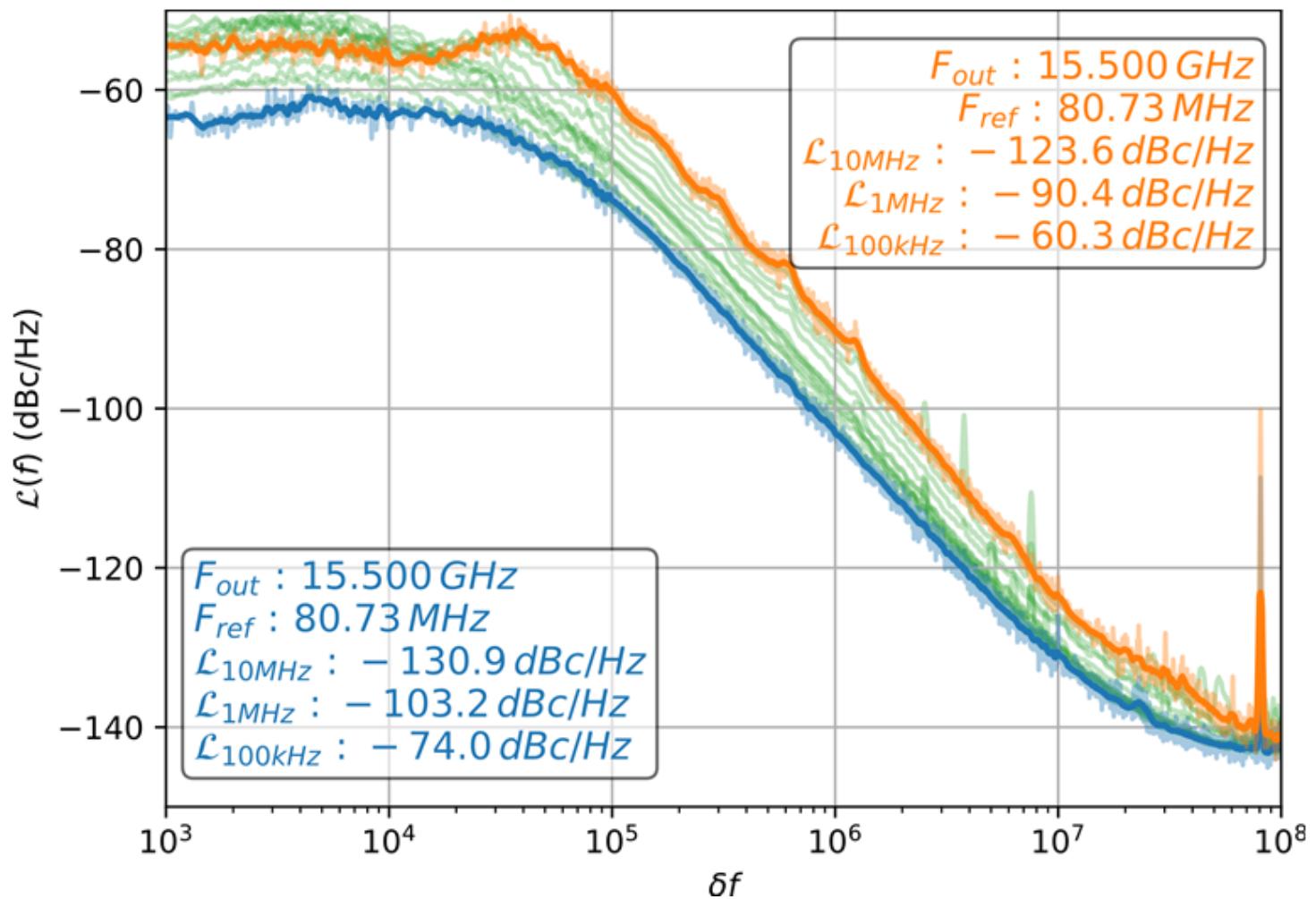
Measured frequency sensitivity to bias voltage



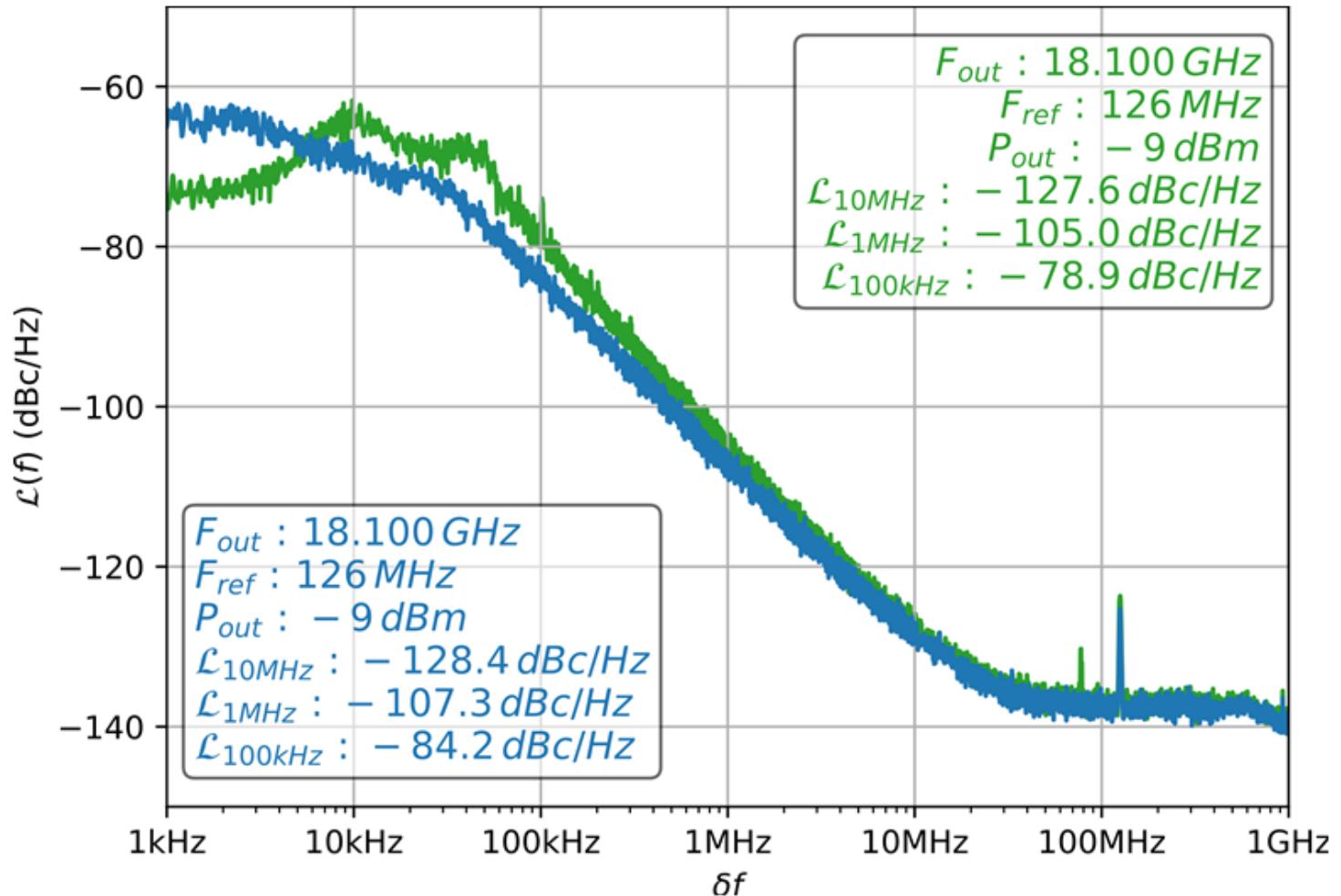
45nm phase noise (top) and current (bottom). Squares are with biasing scheme enabled.



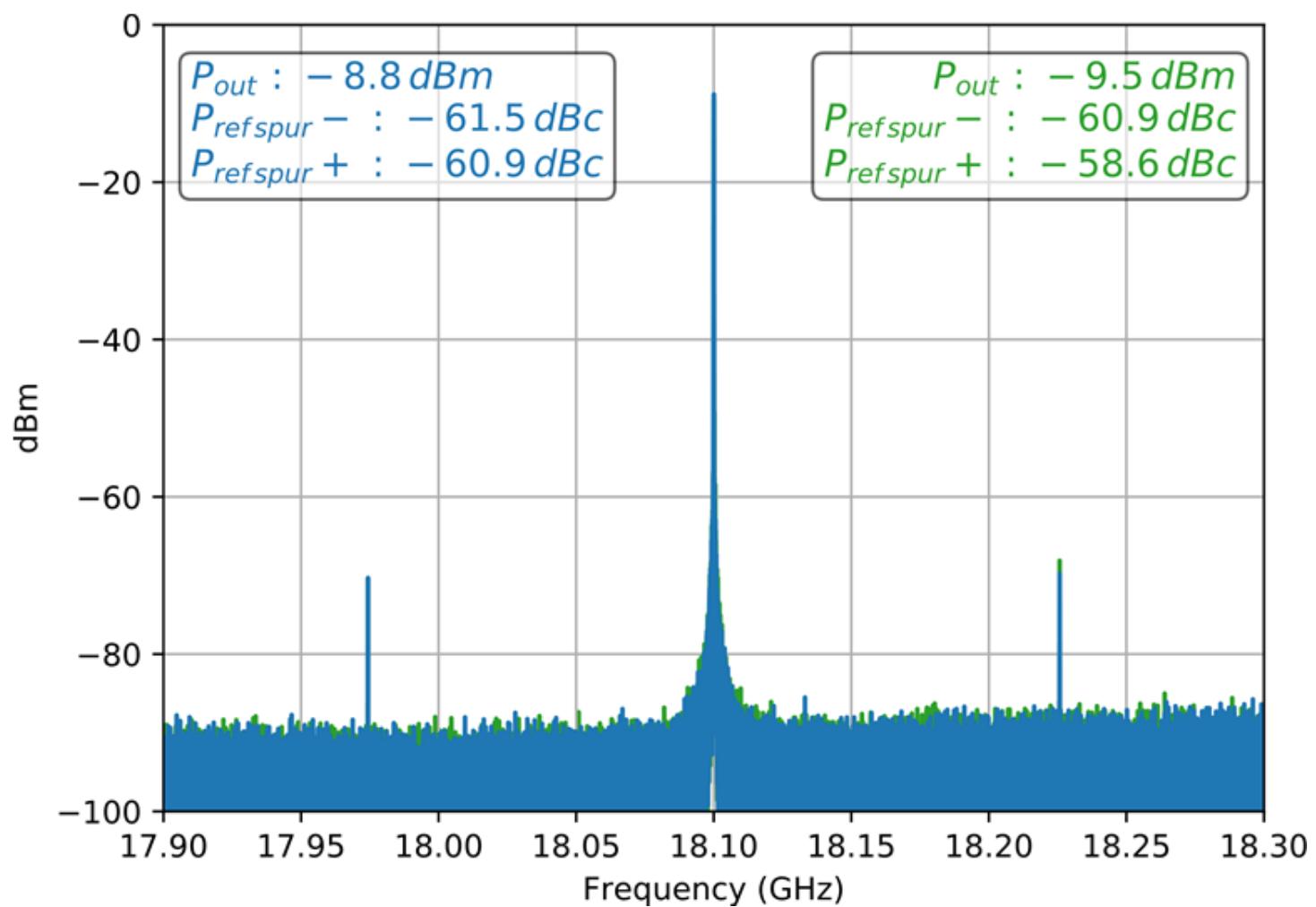
45nm, bias scheme enabled, disabled, and swept



32nm with tail inductor, bias scheme **enabled**, **disabled**



32nm output spectrum

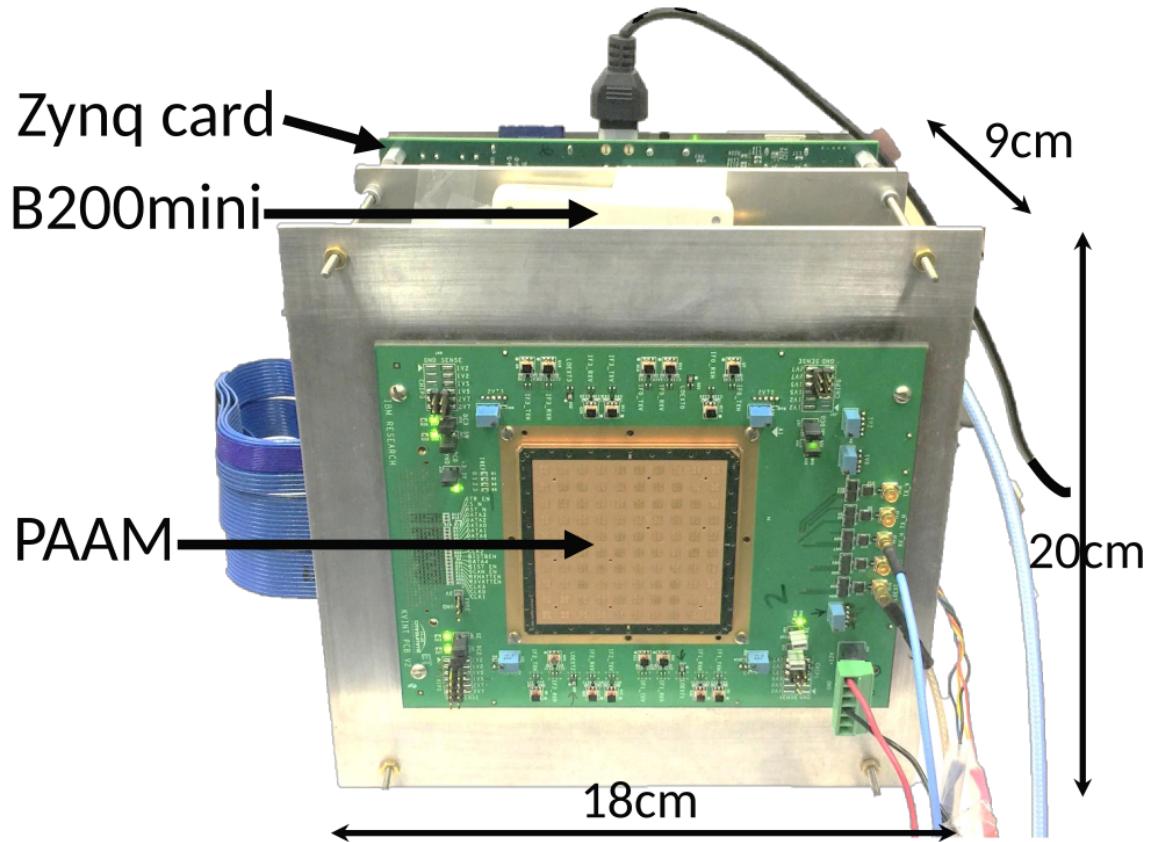


Software for phased arrays

Sadhu, B.; Paidimarri, A.; **Ferriss, M.**; Yeck, M.; Gu, X.; Valdes-Garcia, A.,
"A Software-Defined Phased Array Radio with mmWave to Software Vertical Stack Integration for 5G Experimentation,"
2018 IEEE/MTT-S International Microwave Symposium - (IMS), 2018.

Sadhu, B.; Tousi, Y.; Hallin, J.; Sahl, S.; Reynolds, S.; Renström, Ö.; Sjögren, K.; Haapalahti, O.; Mazor, N.; Bokinge, B.; Weibull, G.; Bengtsson H.; Carlinger, A.; Westesson E., Thillberg, J.; Rexberg, L.; Yeck M., Gu X.; **Ferriss M.**; Liu, D.; Friedman, D.; Valdes-Garcia, A.,
"A 28-GHz 32-Element TRX Phased-Array IC With Concurrent Dual-Polarized Operation and Orthogonal Phase and Gain Control for 5G Communications"
IEEE Journal of Solid-State Circuits, 2017. **Awarded JSSC 2017 Best Paper.**

The 5G module

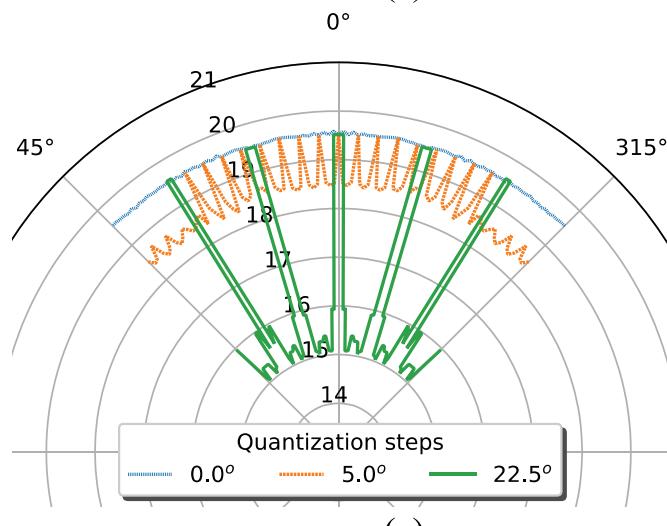


Photograph of the SDPAR system.

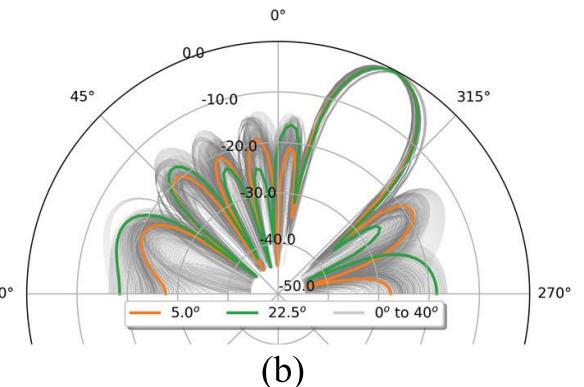
Simulating non-idealities

Phase shifter resolution	0°	5°	22.5°
Beam steering resolution (uniform phase)	0°	1.4°	6.5°
Beam steering resolution (non-uniform phase)	$<1^\circ$	$<1^\circ$	$<1^\circ$
Sidelobe suppression (attempting 20dB)	19.5dB	>18.5dB	>15dB

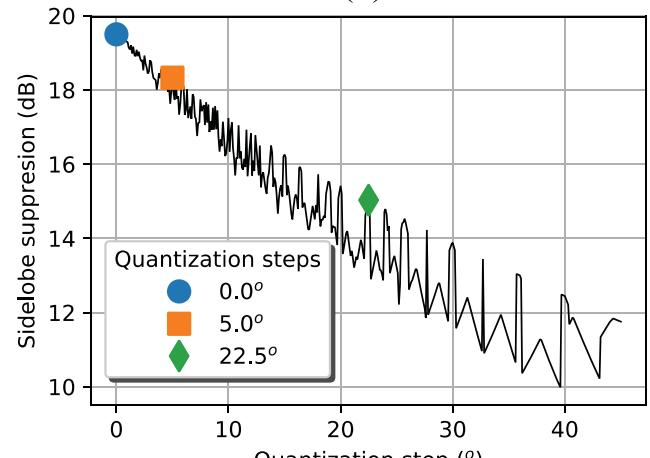
(a)



(c)



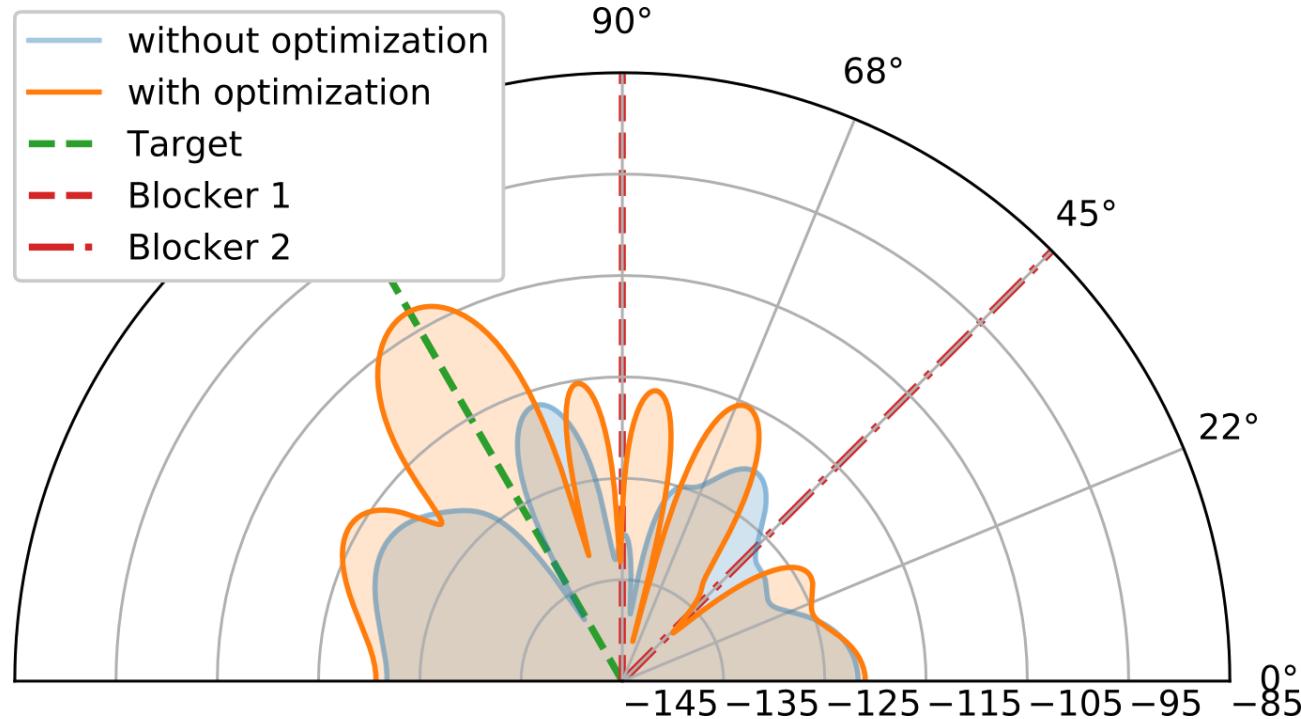
(b)



(d)

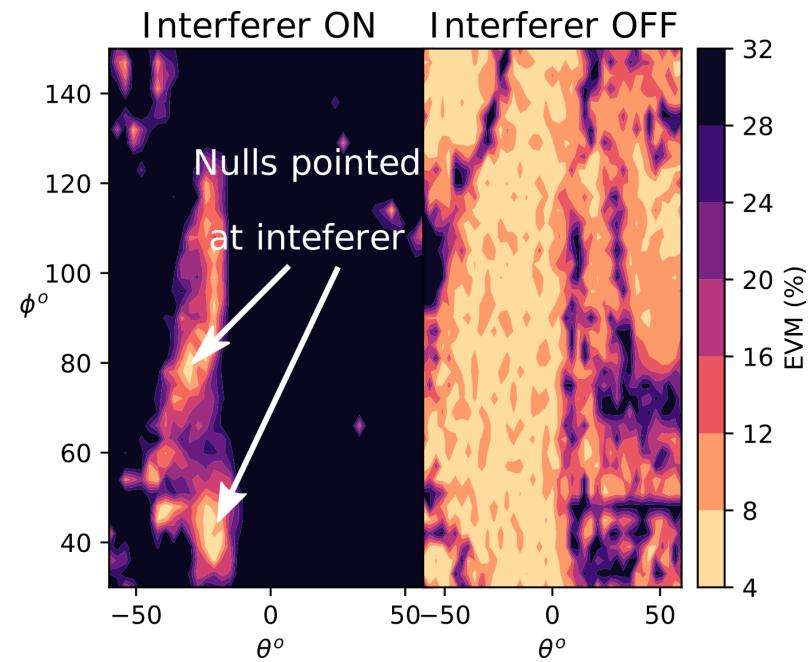
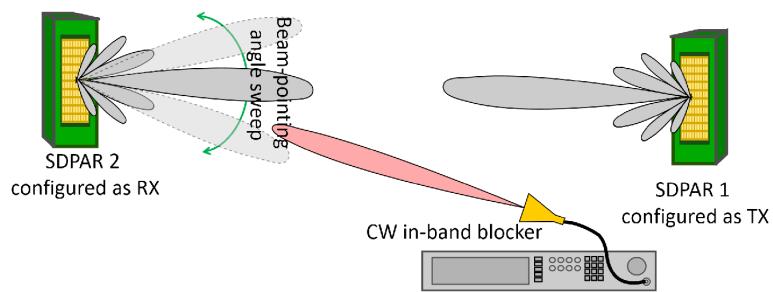
- (a) Simulation of the effect of phase shift quantization in an 8×8 phased array showing beam steering resolution for different phase shifter resolutions.
 (b) Beam pointing at an arbitrary direction (30°) for different phase shifter resolutions showing a large impact on sidelobe suppression. (c) Sidelobe suppression versus beam steering angle for three different phase shifter resolutions while attempting 20-dB Taylor window tapering. (d) Worst case sidelobe suppression versus quantization steps while attempting \sim 20-dB Taylor window tapering.

Beam optimization (Software)



An optimization experiment using the SDPAR software emulator where the optimizer creates a beam pattern to improve signal to interference ratio starting from an arbitrary beam.

Beam optimization (Hardware)



The End