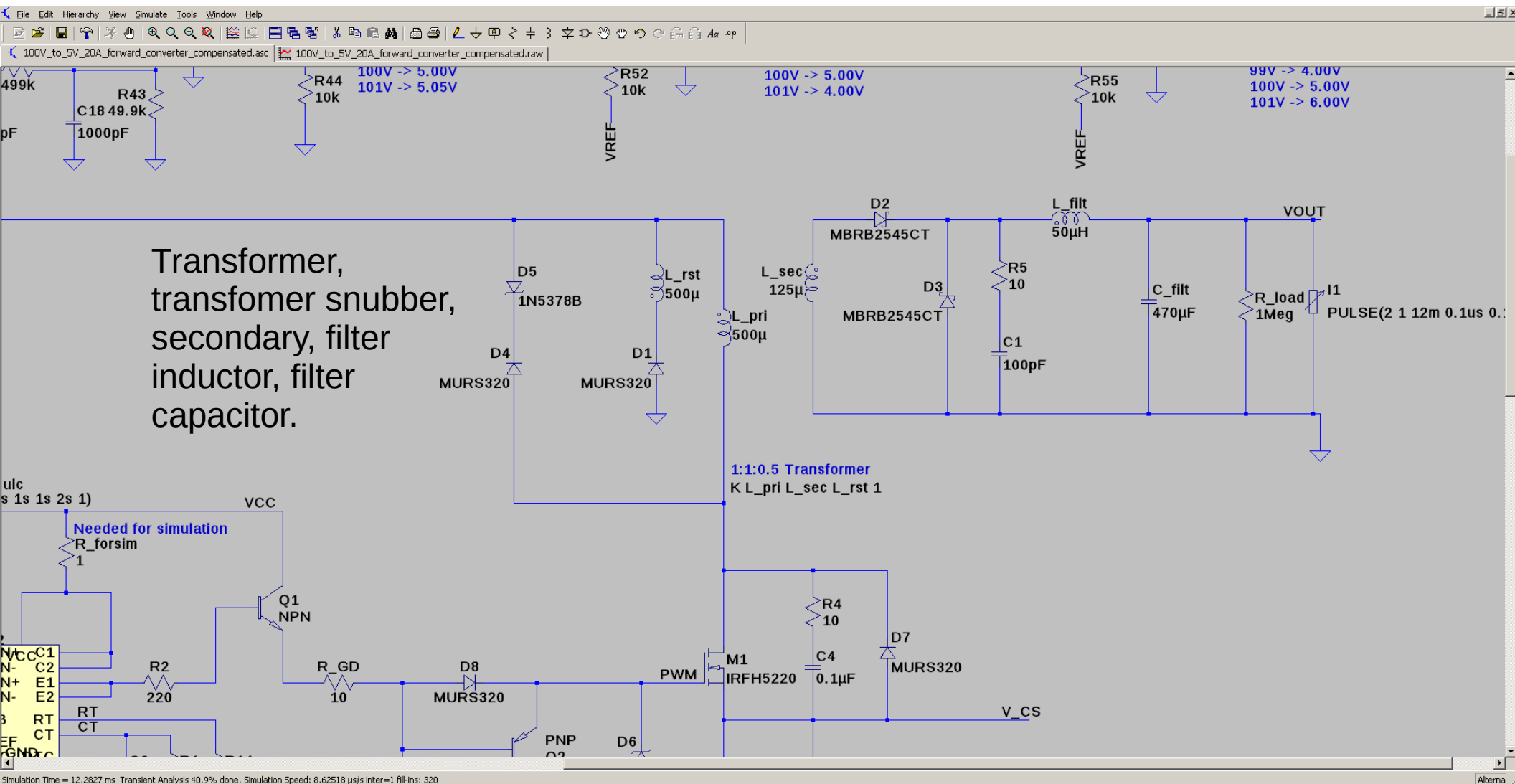


Snubber and antiparallel diode
for inductive kickback from
transformer switching

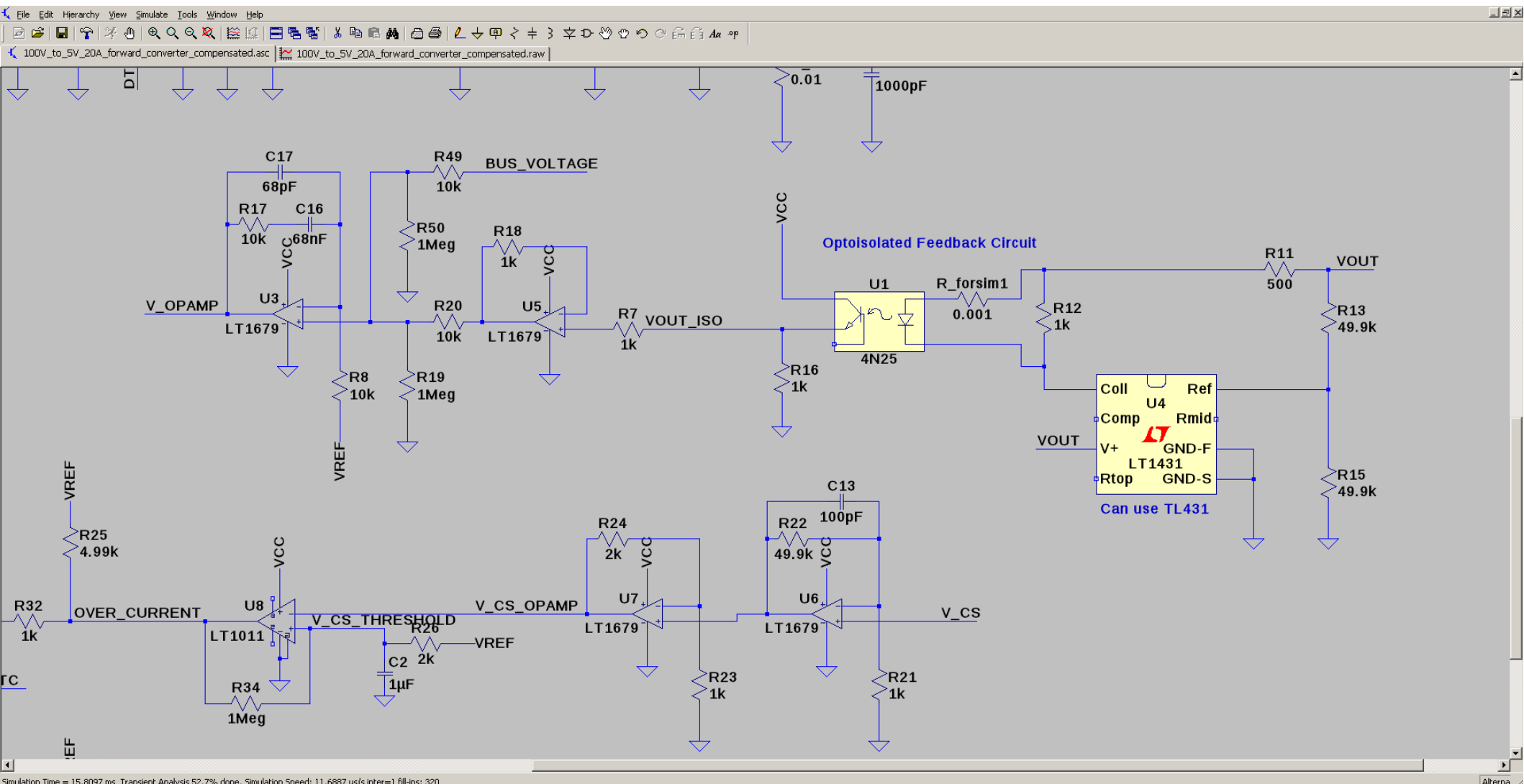


D5 + D4 are a snubber and clipper to limit drain voltage to 180V.

R5 and C1 are a snubber for rectifiers D2 and D3.

L_{filt} and C_{filt} make the current and ripple filter, respectively. NOTE: must use output capacitors that have a combined ESR of about 0.3 ohms for stability.

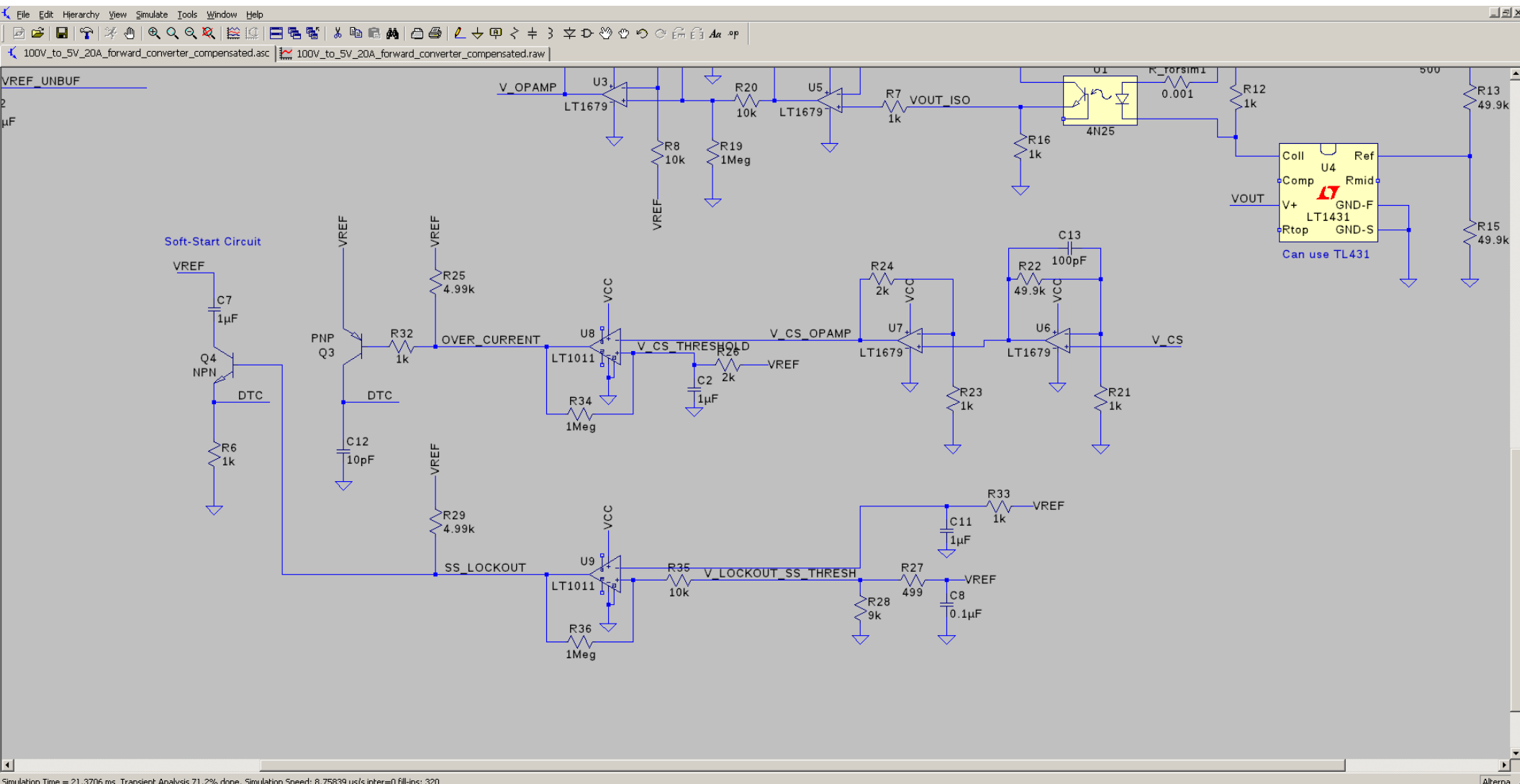
I1 is a stepped load for simulation purposes.



R12 provides a bias current to the opto LED. VOUT can not fall below about 4 V, or the TL431 starts to shutdown.

This is a problem for feedforward control, since if solar panel voltage goes up by 2V, then the output voltage needs to drop to 3V. We might need an auxiliary supply on the secondary side. Perhaps a small 5V → 12V prepackaged boost?

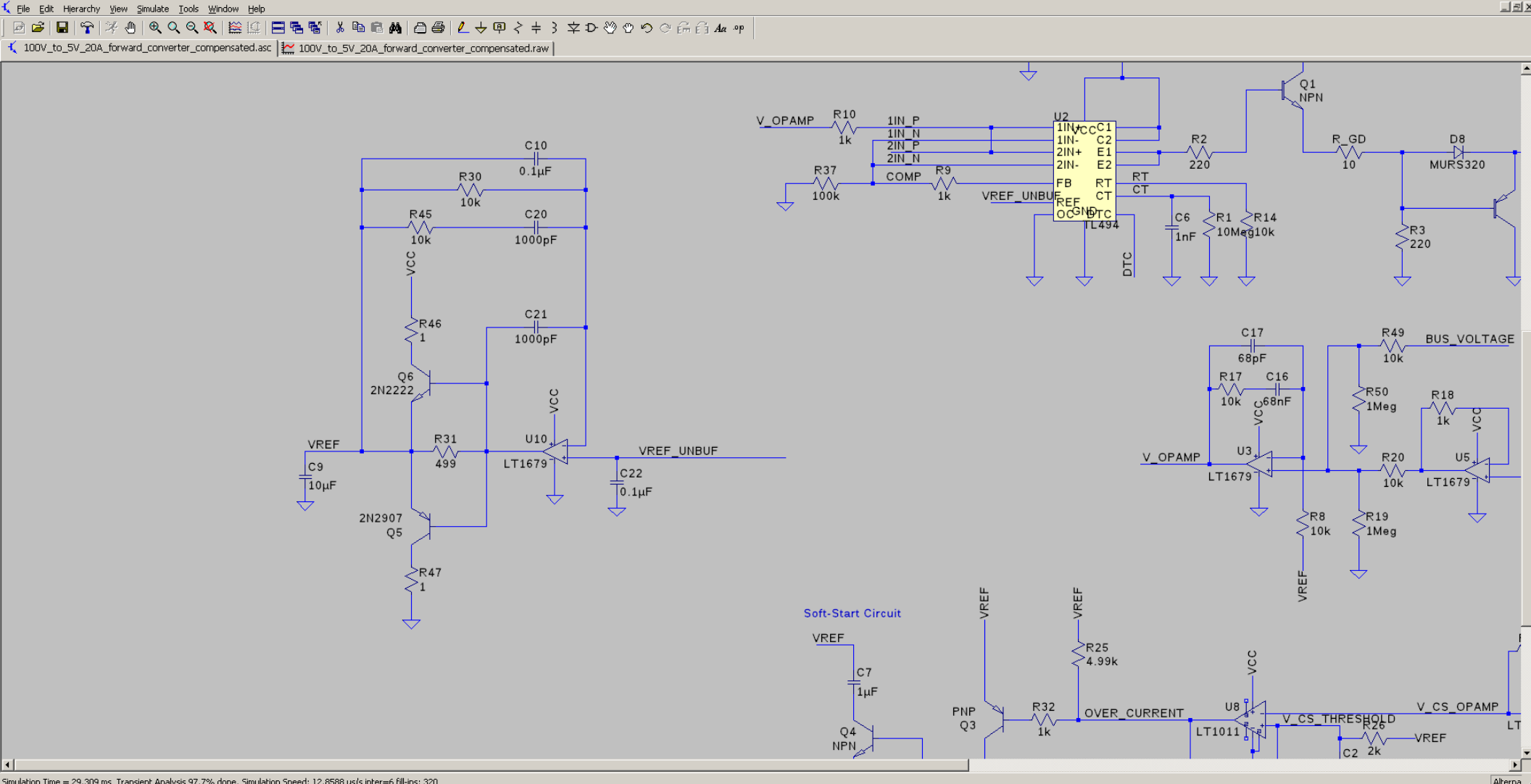
R11, R16, and the opto gain set the output voltage. Need a pot in place of R11 to dial it in



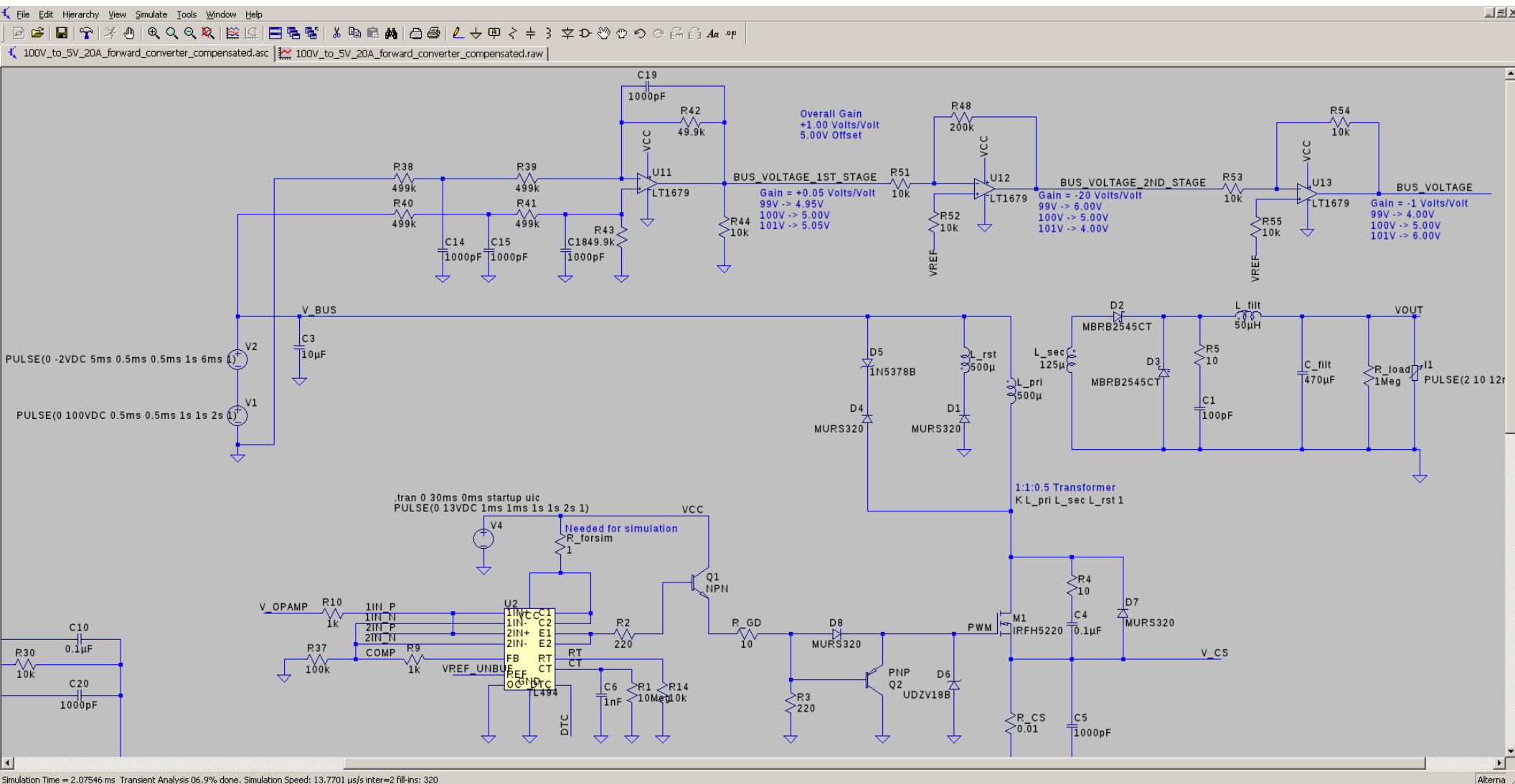
V_{CS} is the raw voltage across the current sense resistor. It is gained up and filtered slightly by U6. The current loop needs to be fast, hence the slight amount of filtering.

U7 provides a final gain of 3V/V. In order to adjust the current limit, the gain is adjusted on U7, not U6, so as to maintain the RC time constant in the feedback of U6.

The current limit threshold is soft-started by an RC formed by R26 and C2 (2k and 1 μF). This voltage forms the threshold for the current limit comparator U8. Upon converter power up, the load wants to draw a huge current from the primary, blowing things up. Having the current limit

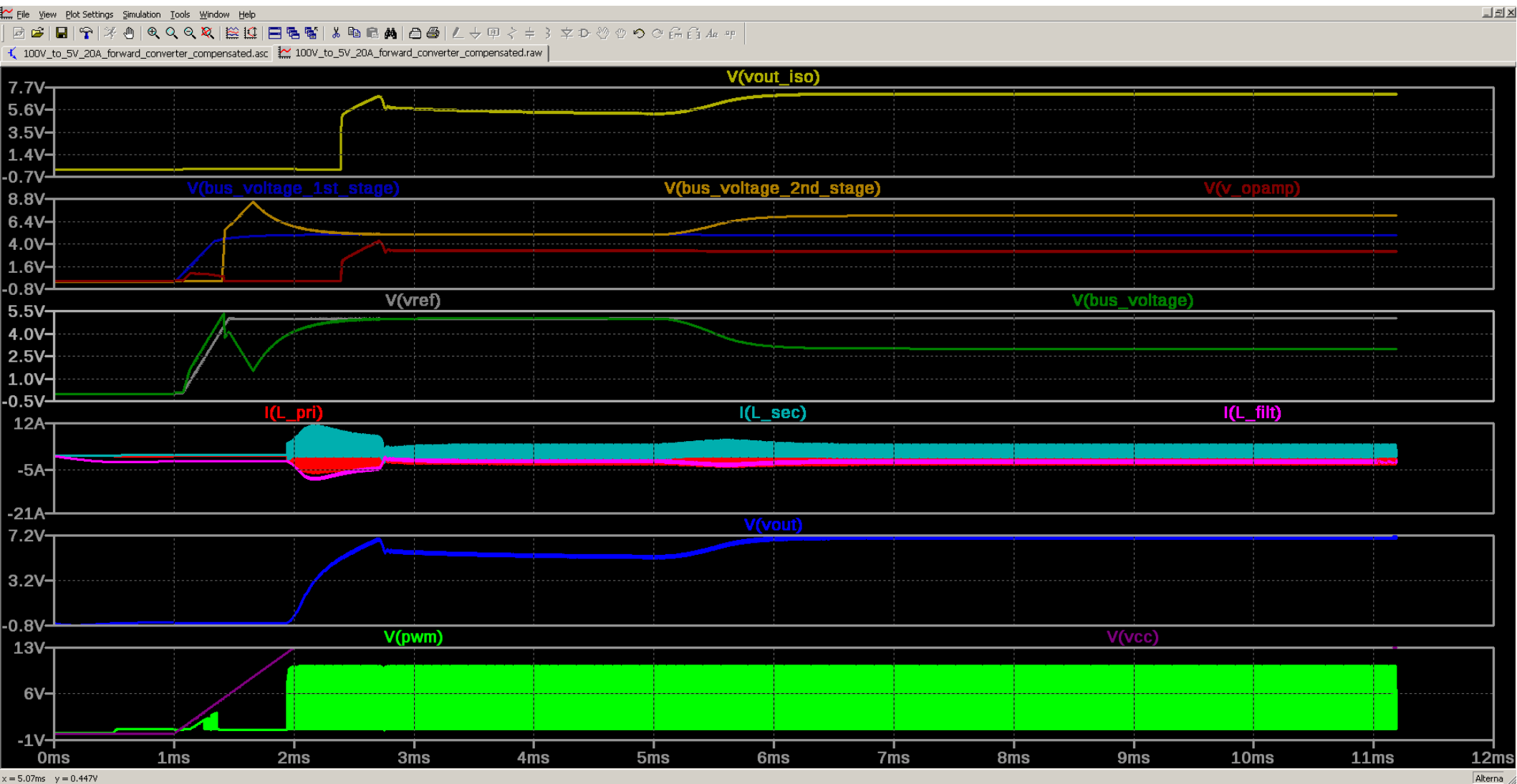


U10 forms a buffer for the 5V reference from the TL494. The stability of the converter is strongly dependent on a stable reference. My current limit circuit is always banging DTC to VREF, causing perturbations, due to insufficient drive. About 50mA is necessary momentarily to charge/discharge caps. This requires a good current booster Q4 and Q5. Stability compensation is provided by C21, C20, R45, and C10. R46 and R47 are for current limit, but of limited benefit.



V1 is the solar panel voltage (100V). V2 simulates a drop in panel voltage by subtracting 2V at 5ms.

U11 is a high-voltage difference amplifier. The gains are written in blue. It is non-inverting. It outputs 5V for 100V solar panel voltage. U12 applies gain to variations off of 5V and subtracts 10V ($2 \times V_{REF}$) leaving a signal that swings 1:1 with solar panel voltage swings. So if the solar panel voltage goes from 100V to 101V, the output of U12 will be 4V (it is inverting). If the solar panel voltage from from 100V to 99V, the output of U12 will be 6V.

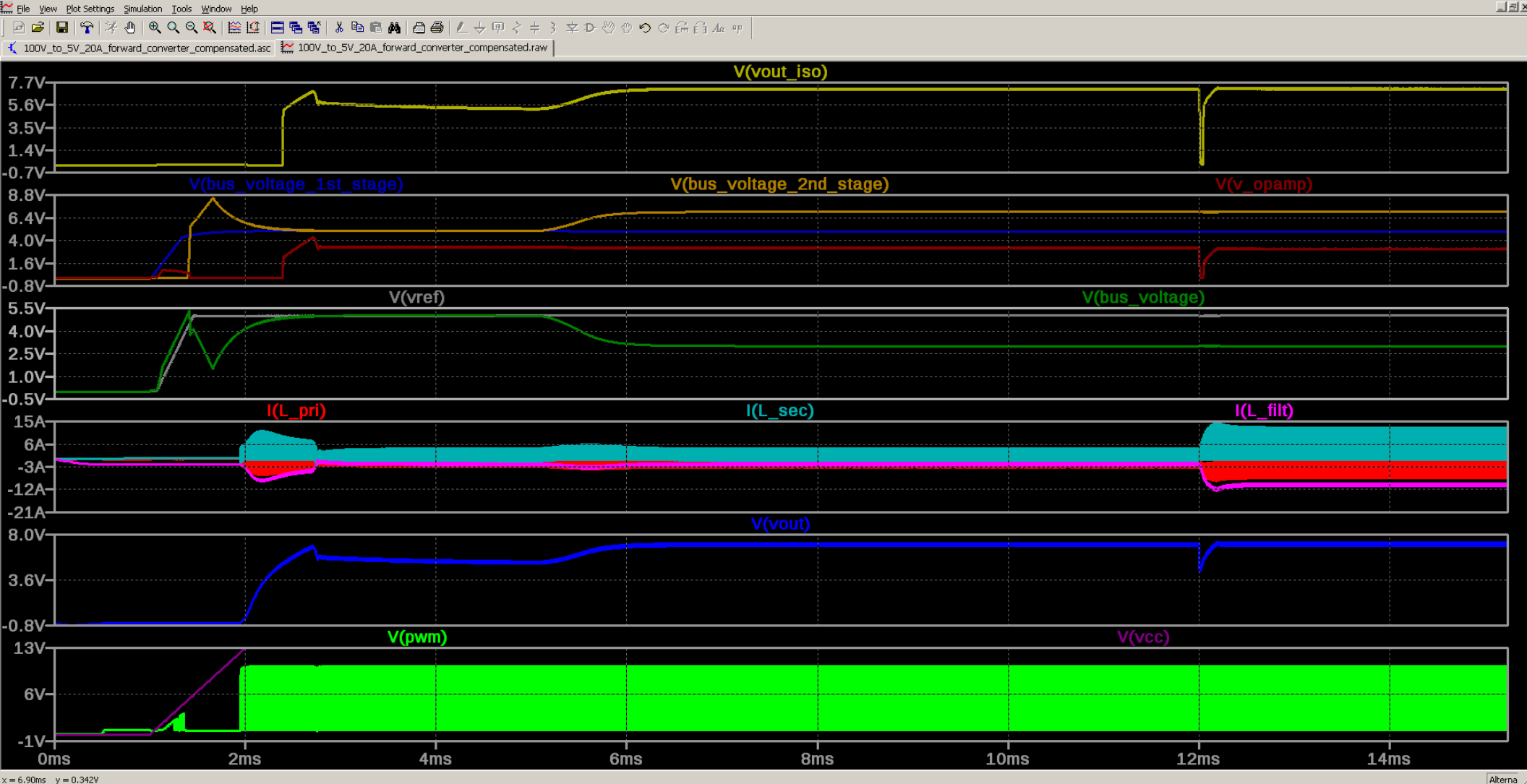


$V(PWM)$ is the PWM gate voltage. The soft start period runs from 1ms to 2ms. After that the gradually increasing current limit takes over.

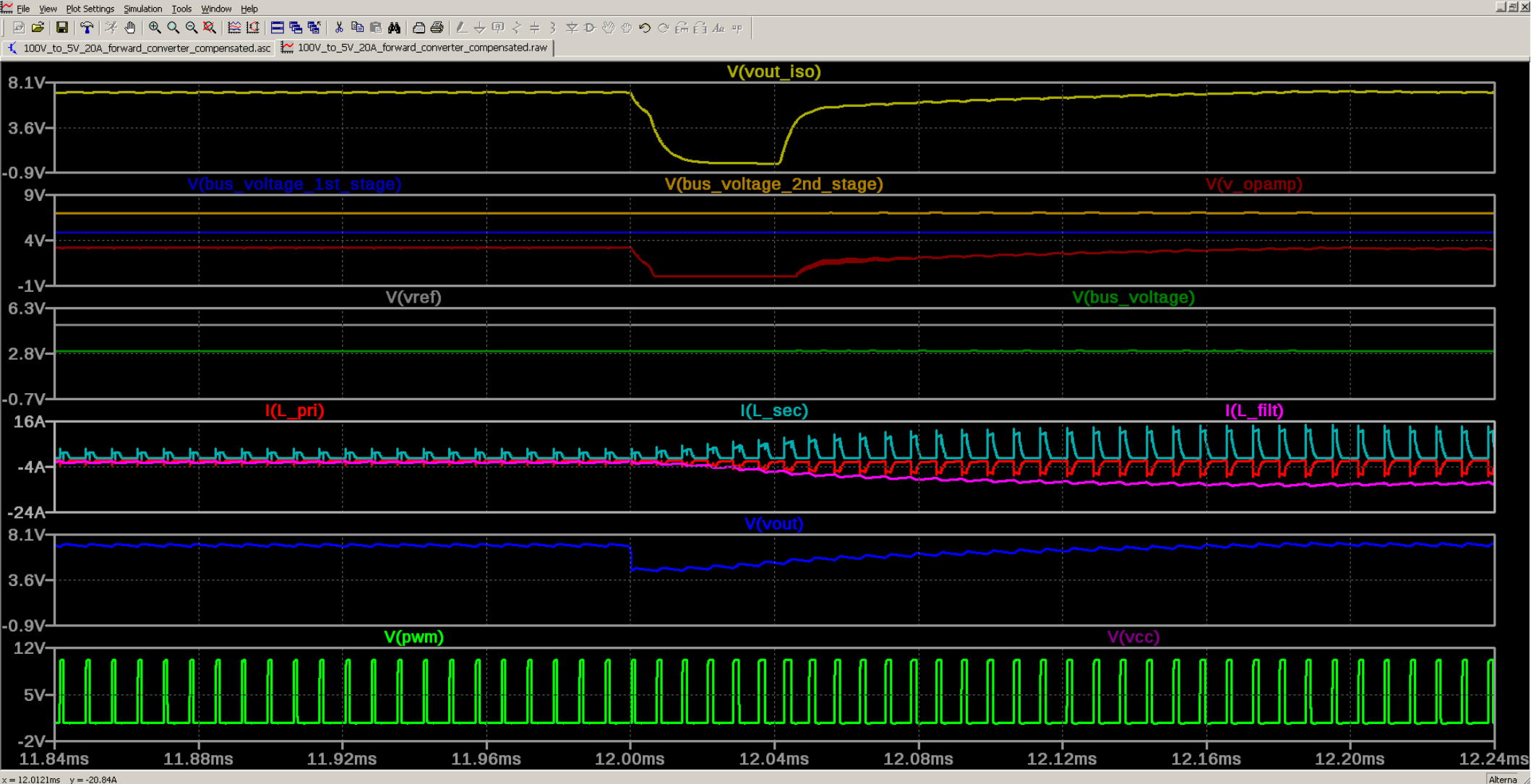
The load current is 2A until 12ms.

The solar panel bus voltage shifts from 100V to 98V at 5ms. The output voltage rises from 5V to 7V ($V(vout)$).

$I(L_pri)$, $I(L_sec)$ and $I(L_filt)$ are the primary, secondary and filter inductor currents, respectively.



At 12ms, the load abruptly changes from 2A to 10A. Transformer currents correspondingly increase, but voltage loop control is maintained. There is a slight dip in the output voltage, which is unavoidable, as no voltage control loop has infinite bandwidth. This response comes from the frequency compensation components around the EA.



Zoomed in view around 12ms, when load step occurs. Notice that the EA output saturates at ground, but recovers. To correct this, it will require lots of calculations to get the optimal frequency compensation values. I got these results by trial and error.



This shows the transformer and filter inductor currents. Some of them are negative to show relative amplitudes, but the currents are actually all positive.

Bus voltage drops from 100V to 98V at 5ms. Output voltage rises to 7V from 5V. Load step from 2A to 10A occurs at 12ms.



The bottom pane shows the overcurrent comparator slamming DTC to VREF when too much current flows in the primary. This limits the primary current until things stabilize.

Also the current blip during the load step is kept under control, as can be seen by the DTC trace at 12 ms.



Here I show the overcurrent threshold RC waveform in the top pane, and the conditioned primary current sense signal (in red). Notice that even under 10A of load to the 5V output, the primary current stays just under the threshold.

NOTE: All of these are adjustable.