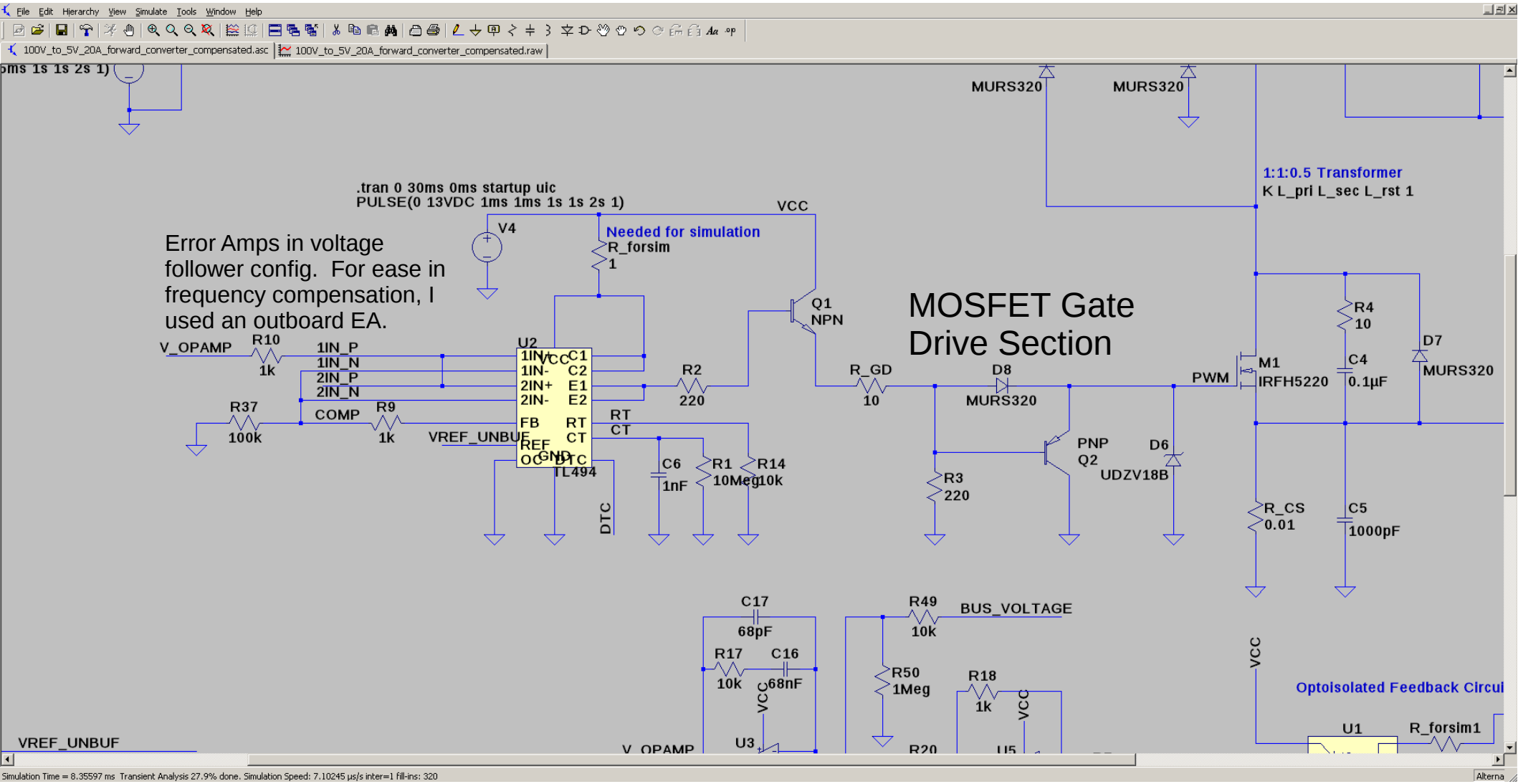
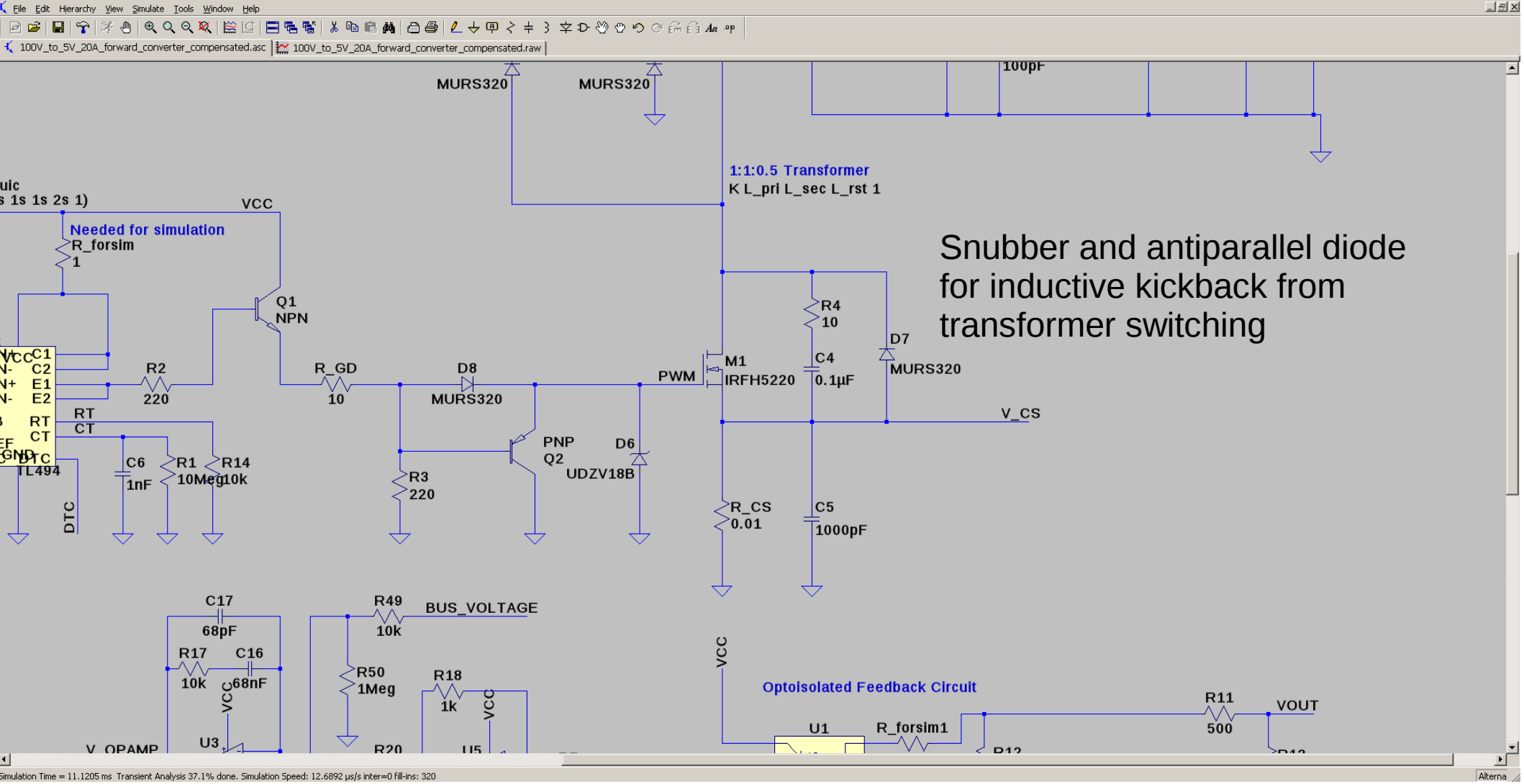
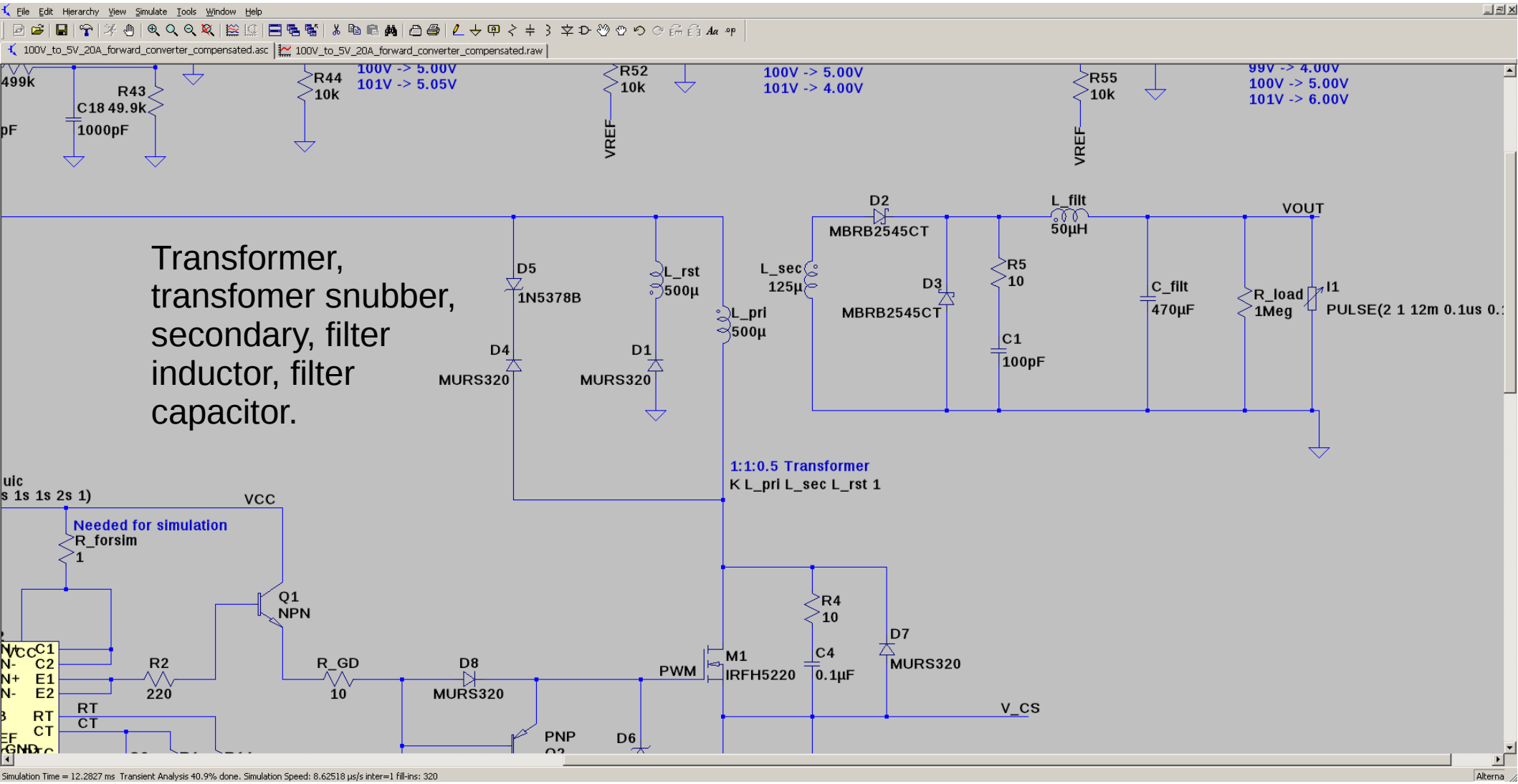
PWM and Gate Drive


File Edit Hierarchy View Simulate Tools Window Help
100V_to_5V_20A_forward_converter_compensated.asc
100V_to_5V_20A_forward_converter_compensated.raw
.tran 0 30ms 0ms startup uic
PULSE(0 13VDC 1ms 1ms 1s 1s 2s 1)
Error Amps in voltage follower config. For ease in frequency compensation, I used an outboard EA.
V4
VCC
Needed for simulation
R_forsim
1
Q1
NPN
MURS320
MURS320
1:1:0.5 Transformer
K L_pri L_sec L_rst 1
MOSFET Gate Drive Section
V_OPAMP
R10
1k
1IN_P
1IN_N
2IN_P
2IN_N
COMP
R37
100k
R9
1k
VREF_UNBUF
U2
1IN+
1IN-
2IN+
2IN-
FB
REF
OC
VCC
GND
C1
C2
E1
E2
RT
CT
DTC
TL494
R2
220
R_GD
10
D8
MURS320
PWM
M1
IRFH5220
R4
10
C4
0.1µF
D7
MURS320
PNP
Q2
R3
220
D6
UDZV18B
R_CS
0.01
C5
1000pF
C6
1nF
R1
10Meg
R14
10k
C17
68pF
R17
10k
C16
68nF
R49
10k
BUS_VOLTAGE
R50
1Meg
R18
1k
U3
U5
R20
U1
R_forsim1
Optoisolated Feedback Circui
VREF_UNBUF
Simulation Time = 8.35597 ms Transient Analysis 27.9% done. Simulation Speed: 7.10245 µs/s inter=1 fill-ins: 320

Main Power Switch Snubber


File Edit Hierarchy View Simulate Tools Window Help
100V_to_5V_20A_forward_converter_compensated.asc
100V_to_5V_20A_forward_converter_compensated.raw
MURS320
MURS320
100pF
1:1:0.5 Transformer
K L_pri L_sec L_rst 1
Needed for simulation
R_forsim
1
VCC
Q1
NPN
R2
220
R_GD
10
D8
MURS320
PWM
M1
IRFH5220
R4
10
C4
0.1µF
D7
MURS320
V_CS
RT
CT
C6
1nF
R1
10Meg
R14
10k
DTC
TL494
PNP
Q2
R3
220
D6
UDZV18B
R_CS
0.01
C5
1000pF
Snubber and antiparallel diode for inductive kickback from transformer switching
C17
68pF
R17
10k
C16
68nF
R49
10k
BUS_VOLTAGE
R50
1Meg
R18
1k
VCC
Optoisolated Feedback Circuit
U1
R_forsim1
R11
500
VOUT
V_OPAMP
U3
R20
U5
Simulation Time = 11.1205 ms Transient Analysis 37.1% done. Simulation Speed: 12.6892 µs/s inter=0 fill-ins: 320

Transformer, Rectifier and Output Filter



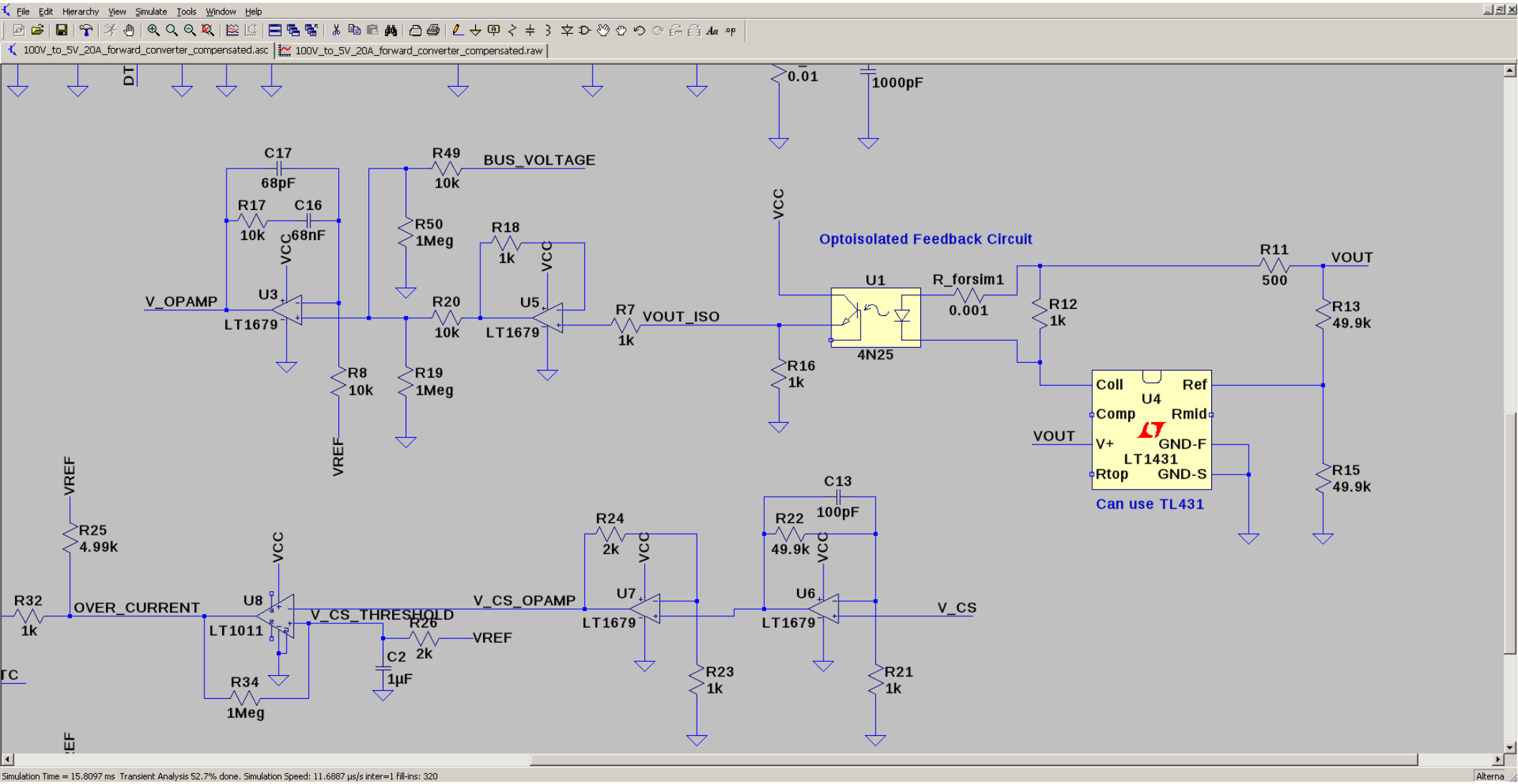
D5 + D4 are a snubber and clipper to limit drain voltage to 180V.

R5 and C1 are a snubber for rectifiers D2 and D3.

L_filt and C_filt make the current and ripple filter, respectively. NOTE: must use output capacitors that have a combined ESR of about 0.3 ohms for stability.

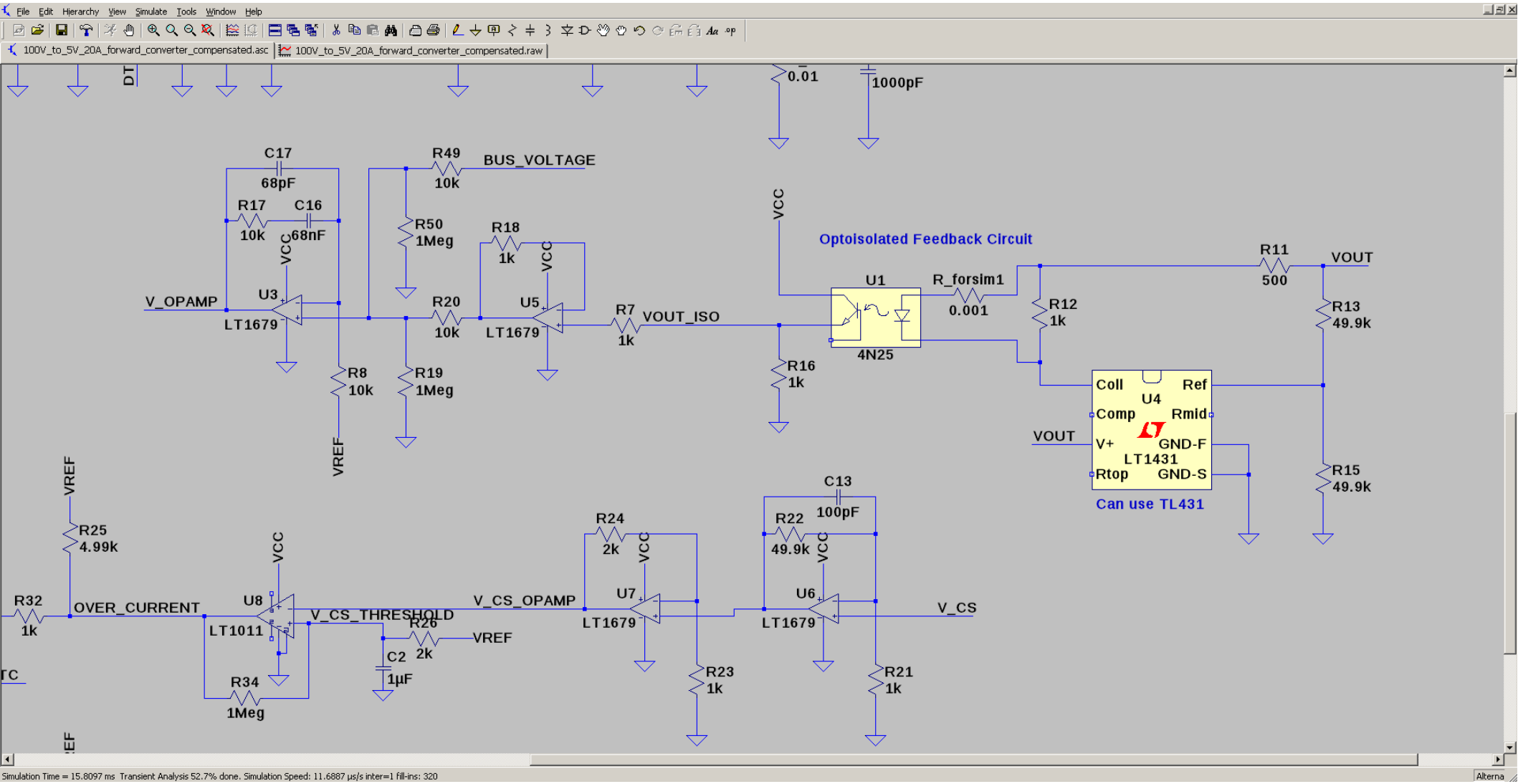
I1 is a stepped load for simulation purposes.

Optoisolator and Type II Error Amplifier



R12 provides a bias current to the opto LED. VOUT can not fall below about 4 V, or the TL431 starts to shutdown.

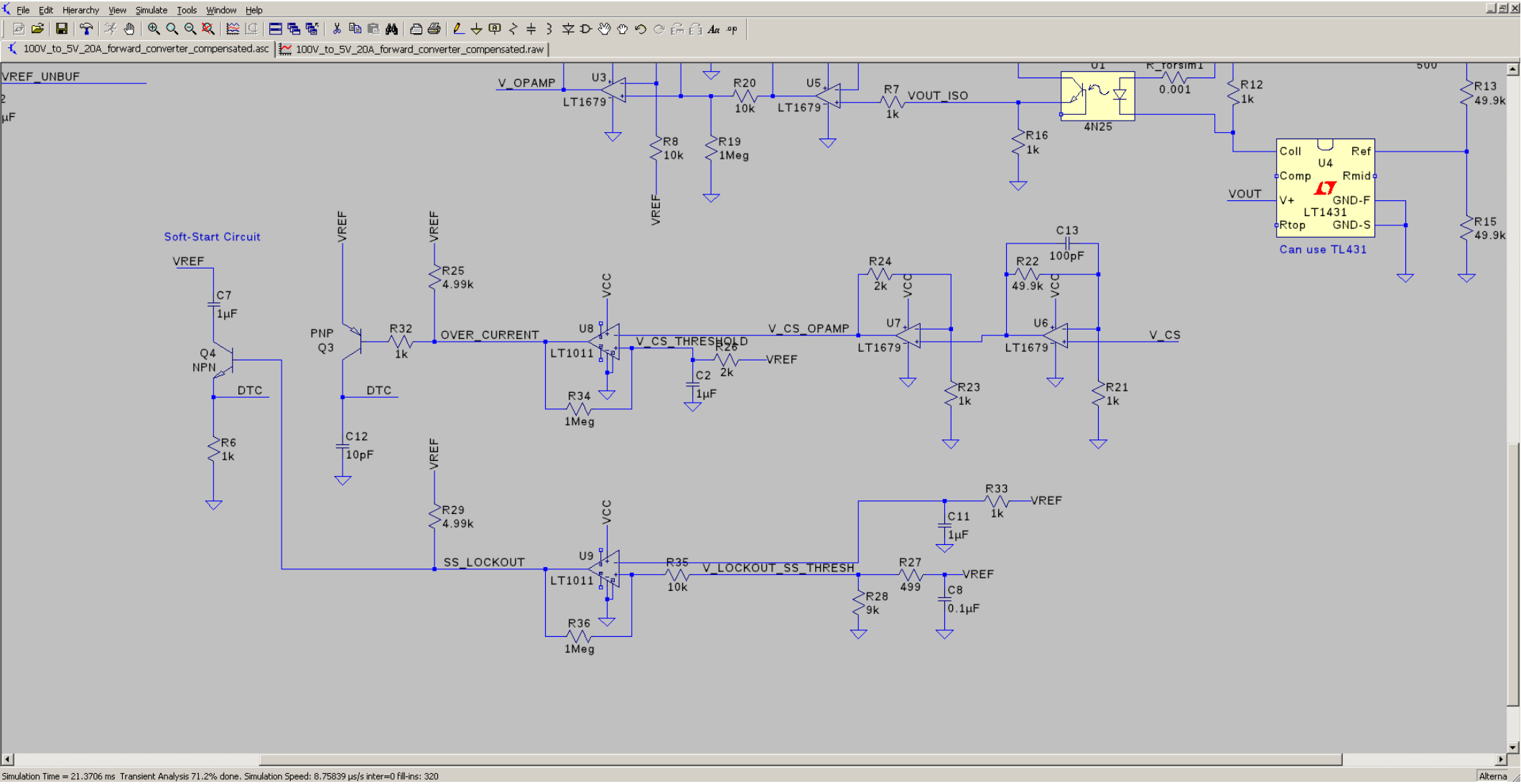
This is a problem for feedforward control, since if solar panel voltage goes up by 2V, then the output voltage needs to drop to 3V. We might need an auxiliary supply on the secondary side. Perhaps a small 5V → 12V prepackaged boost?



R11, R16, and the opto gain set the output voltage. Need a pot in place of R11 to dial it in to account for opto current transfer ratio variation.

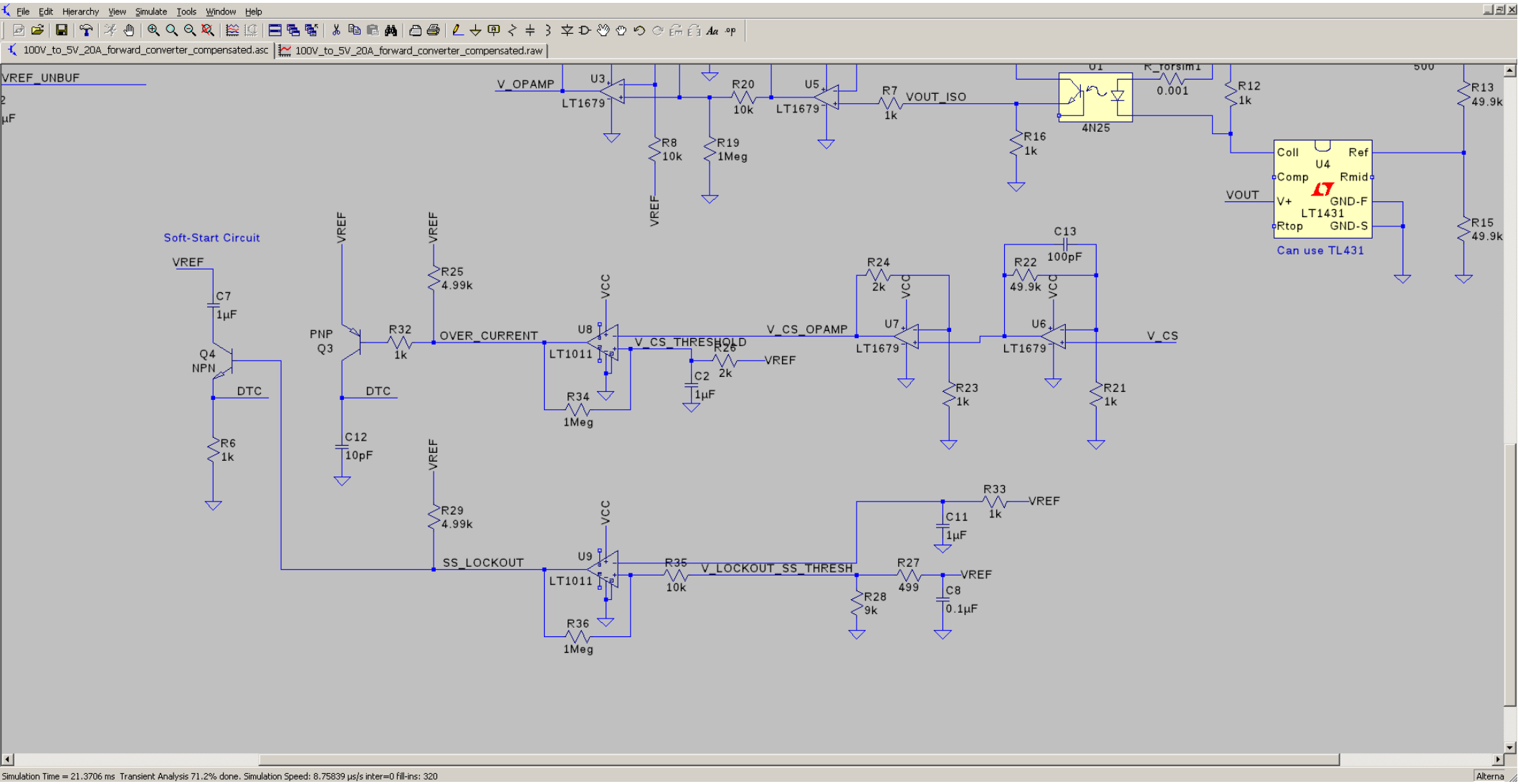
U5 provides buffering of the opto output. U3 is the EA. It is a type 2 error amplifier with dialed in frequency compensation. It also has a feedforward term injected via R49 (BUS_VOLTAGE)

Current Limiting Control and Soft Start

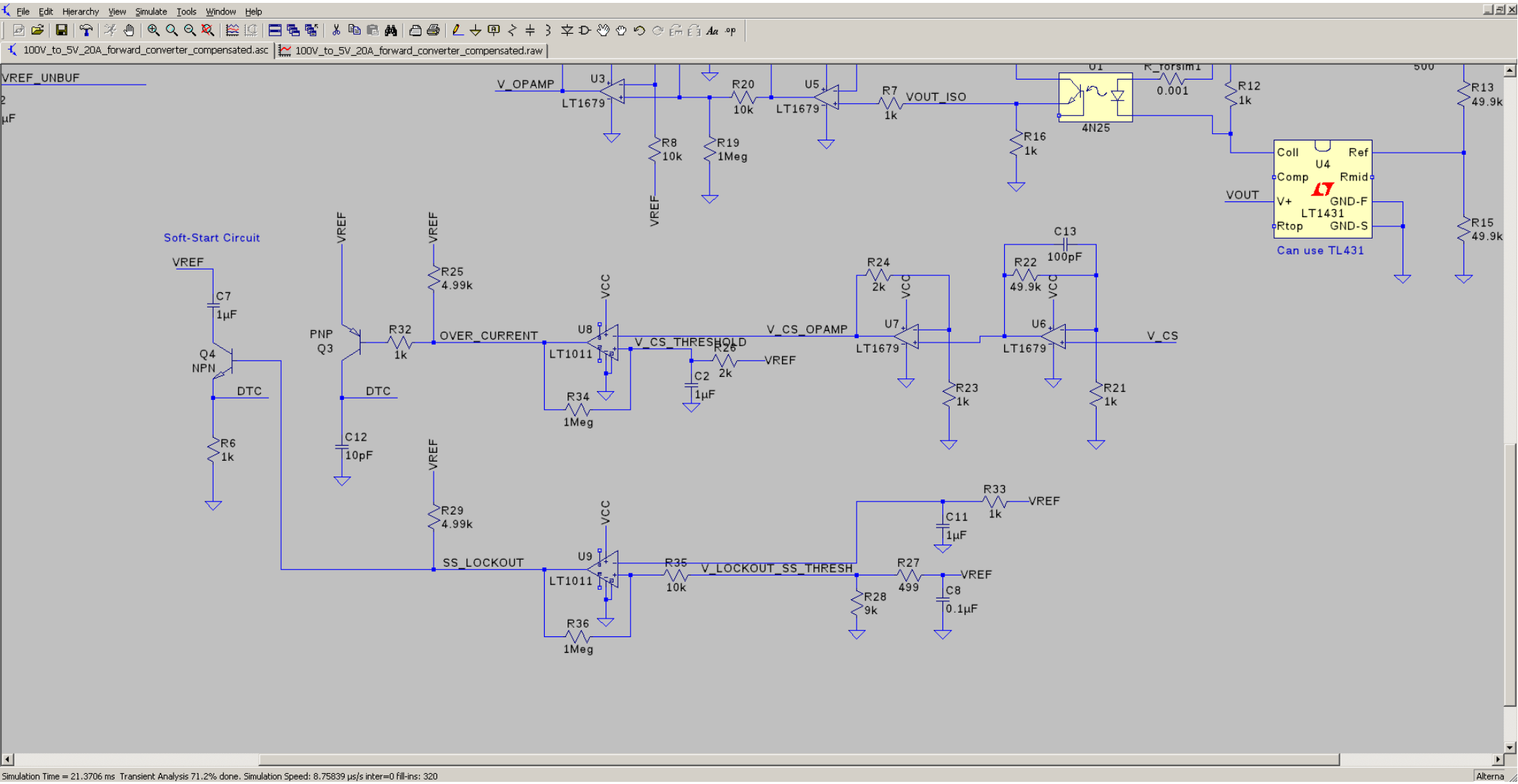


V_CS is the raw voltage across the current sense resistor. It is gained up and filtered slightly by U6. The current loop needs to be fast, hence the slight amount of filtering.

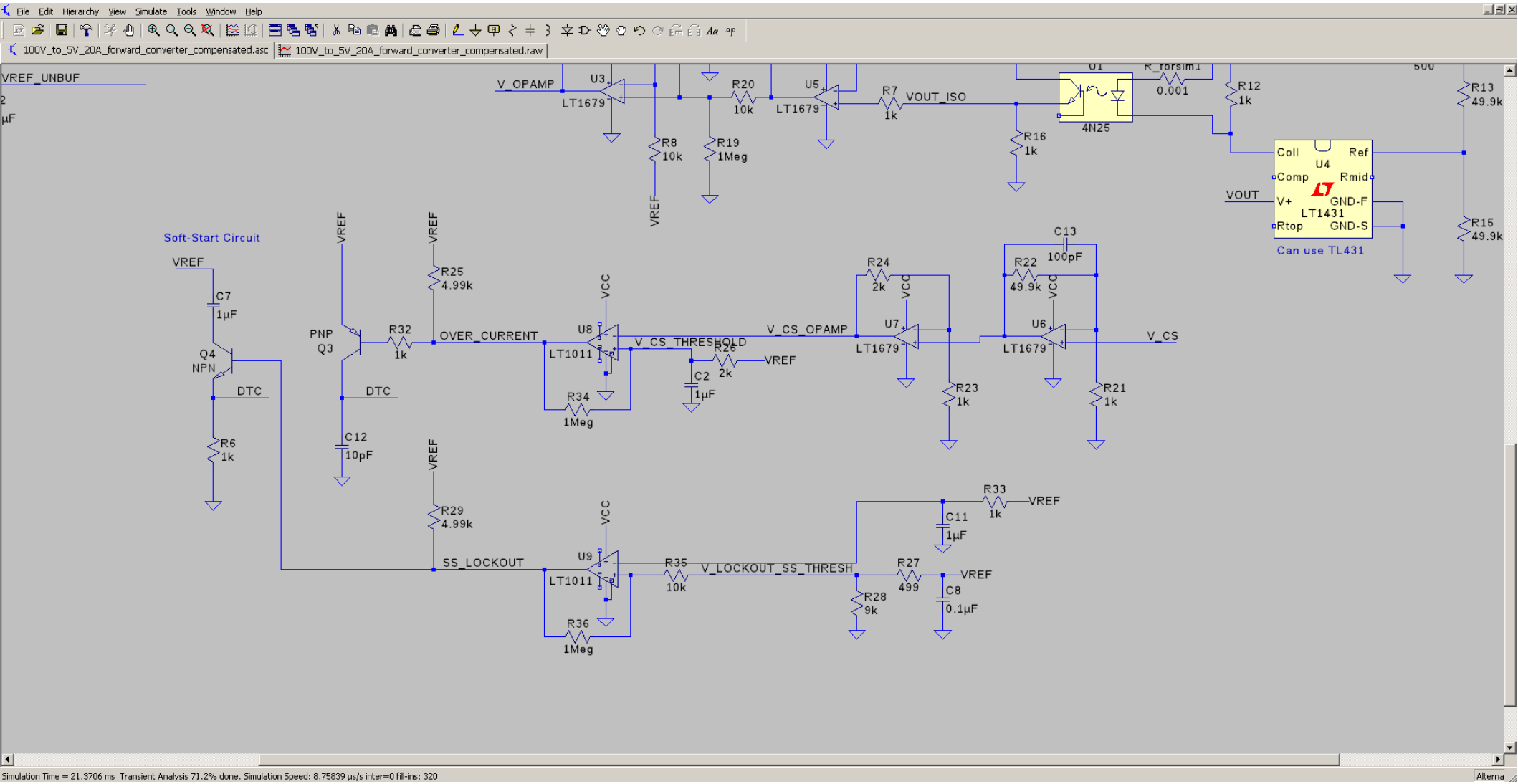
U7 provides a final gain of 3V/V. In order to adjust the current limit, the gain is adjusted on U7, not U6, so as to maintain the RC time constant in the feedback of U6.



The current limit threshold is soft-started by an RC formed by R26 and C2 (2k and 1uF). This voltage forms the threshold for the current limit comparator U8. Upon converter power up, the load wants to draw a huge current from the primary, blowing things up. Having the current limit gradually come up prevents huge startup currents.

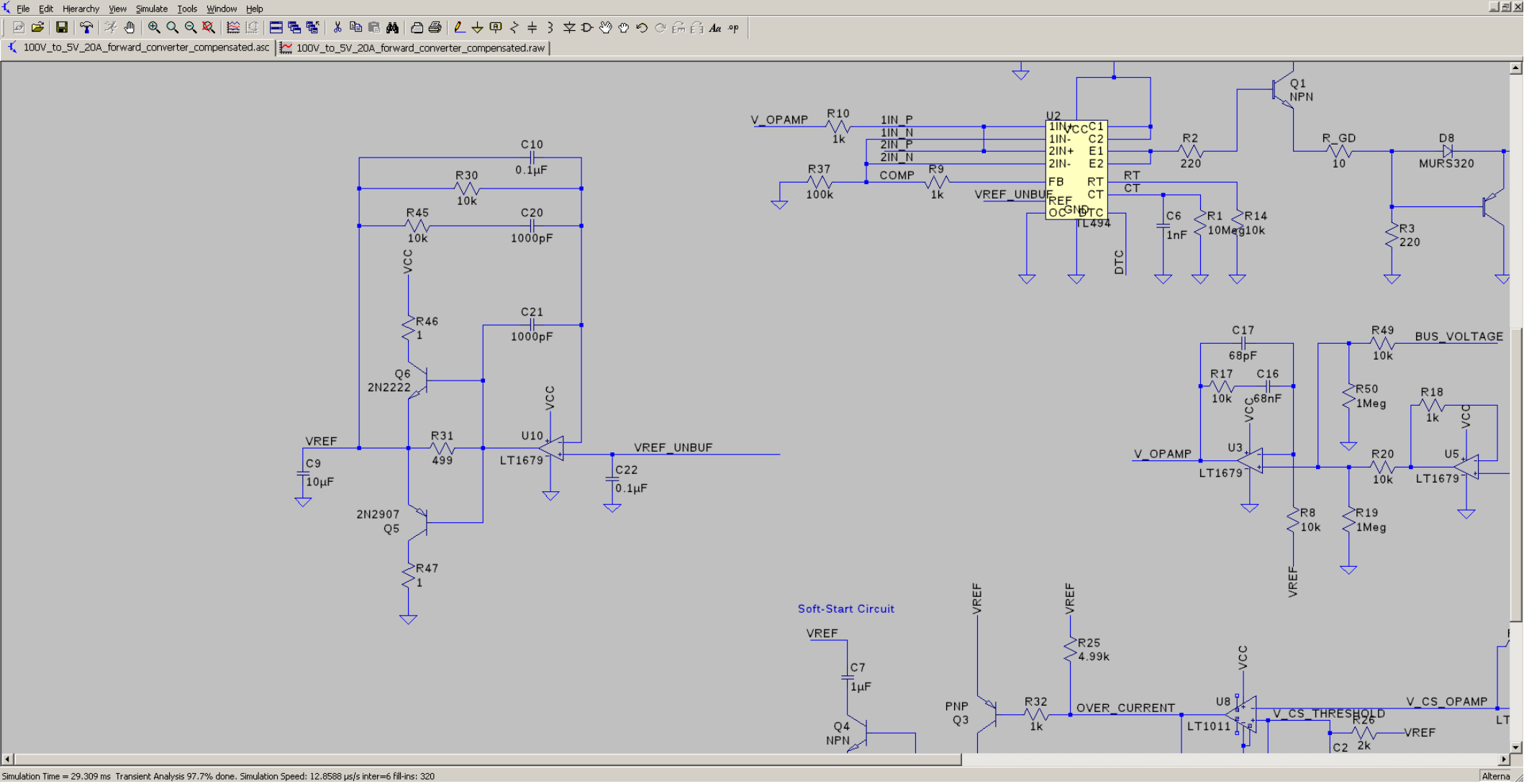


Upon converter power up, the main softstart holds off PWMs until VCC has reached 13V and the TL494 has sufficient voltage to operate. When the TL494 has sufficient voltage to operate, it activates it 5V reference output. This reference is input into R33 and R27. R27 and R28 divide down the reference voltage slightly, to about 4.5V. The reference at R33 is applied to the RC time constant R33 and C11. This allows soft-start time to be active, and once the Vref is good for sufficient time (3 ms), soft-start is locked out from manipulating the Dead Time Control pin on the TL494 by U9 and Q4.



If the primary current has reached the limit, U8 connects DTC to VREF, cutting the PWM pulse at that moment. This is pulse-by-pulse current limiting.

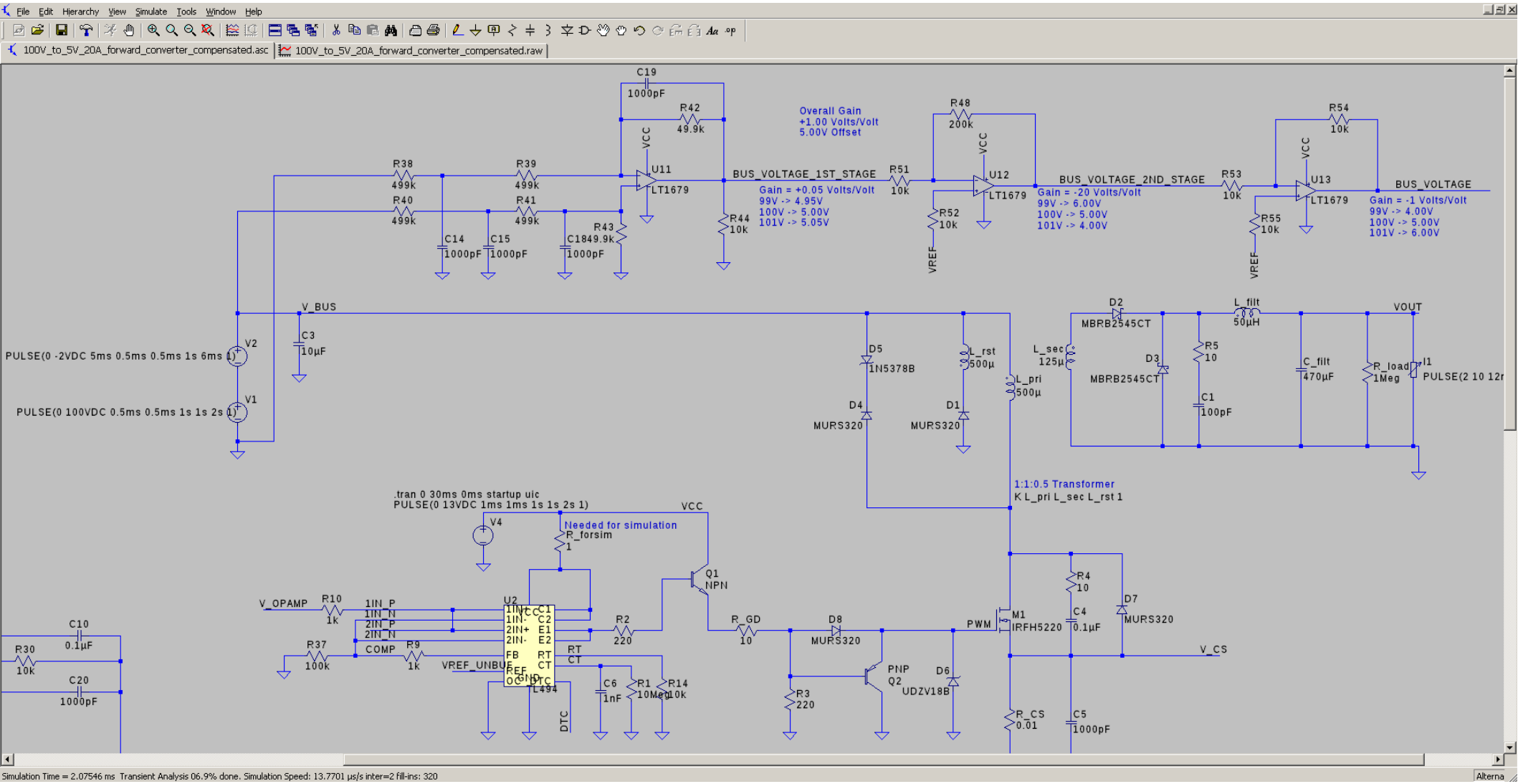
Buffered Voltage Reference



Simulation Time = 29.309 ms Transient Analysis 97.7% done. Simulation Speed: 12.8588 µs/s inter=6 fill-ins: 320

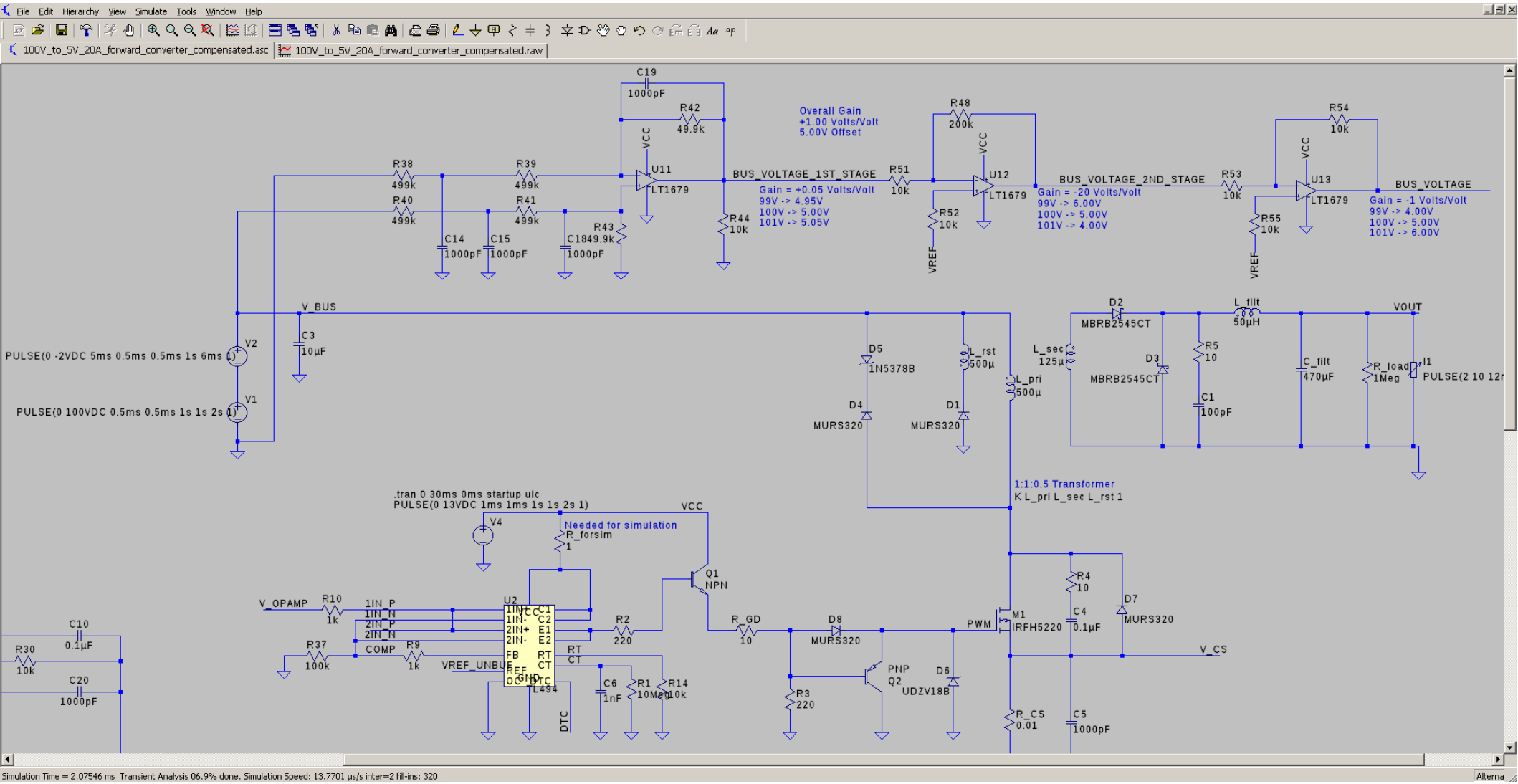
U10 forms a buffer for the 5V reference from the TL494. The stability of the converter is strongly dependent on a stable reference. My current limit circuit is always banging DTC to VREF, causing perterbations, due to insufficient drive. About 50mA is necessary momentarily to charge/discharge caps. This requires a good current booster Q5 and Q6. Stability compensation is provided by C21, C20, R45, and C10. R46 and R47 are for current limit, but of limited benefit.

Input Voltage Feedforward Control



V1 is the solar panel voltage (100V). V2 simulates a drop in panel voltage by substracting 2V at 5ms.

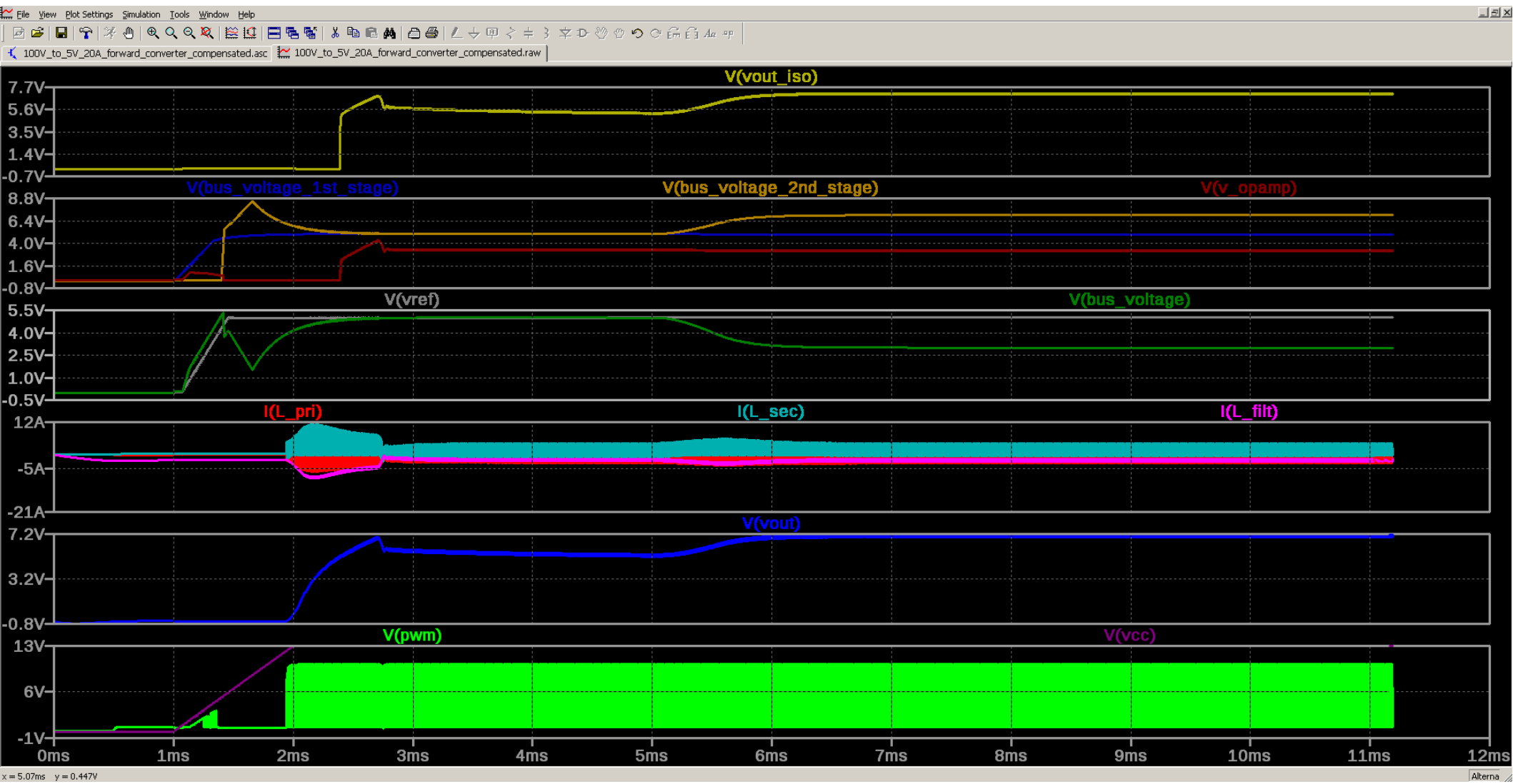
U11 is a high-voltage difference amplifier. The gains are written in blue. It is non-inverting. It outputs 5V for 100V solar panel voltage. U12 applies gain to variations off of 5V and subtracts 10V (2xVREF) leaving a signal that swings 1:1 with solar panel voltage swings. So if the solar panel voltage goes from 100V to 101V, the output of U12 will be 4V (it is inverting). If the solar panel voltage from from 100V to 99V, the output of U12 will be 6V.



U13 simply inverts the output of U11, while maintaining the 5V offset (VREF derived). This signal is applied to the EA as a feedforward term. Since I don't know the bus voltage a priori, I assume it is 100V, knowing how much offset to apply and subtract is critical. All of these offsets are necessary due to single supply op amp operation :(.

To accommodate variation in the solar panel bus voltage, another term will have to be generated that involves the difference between the actual bus voltage and 100V.

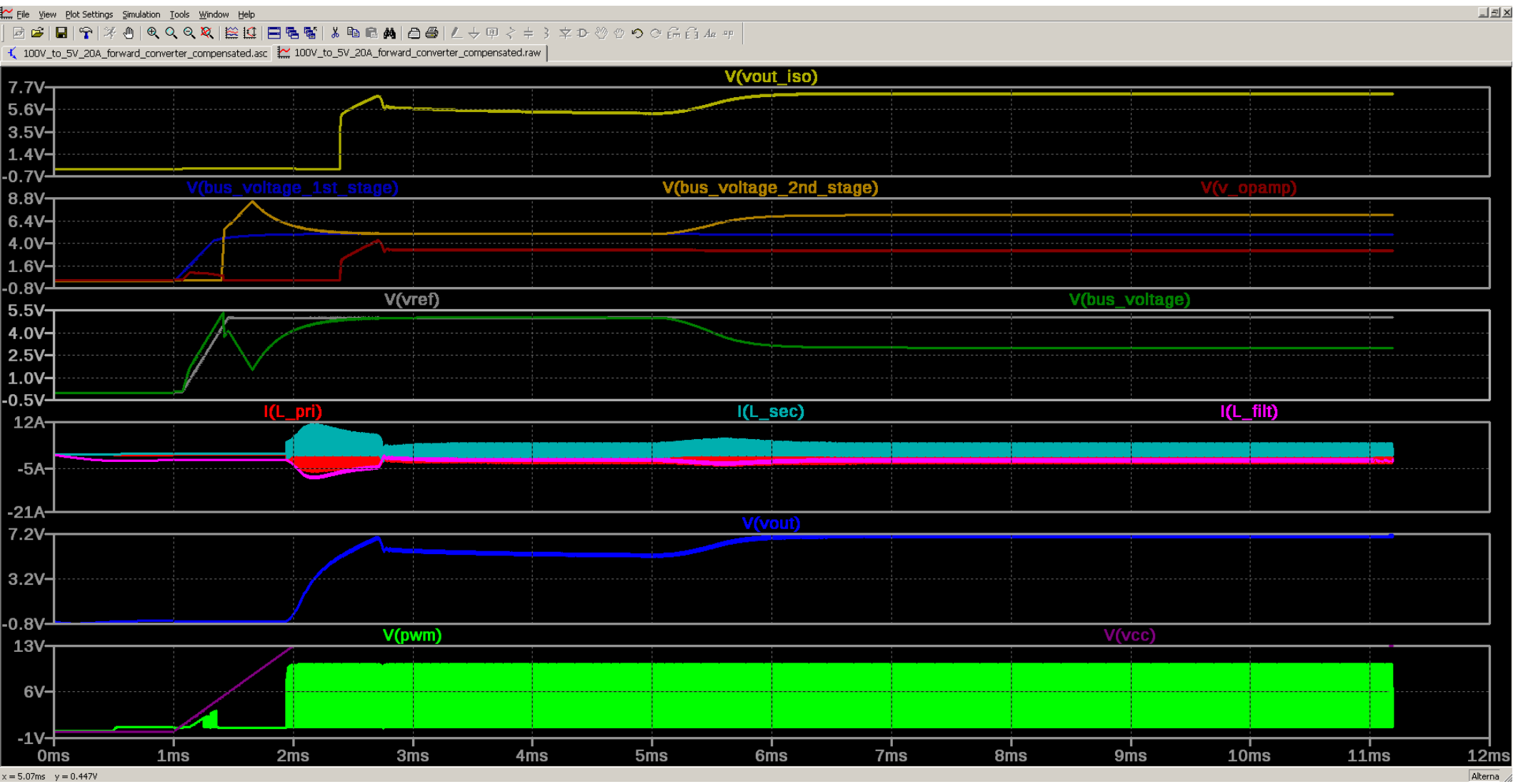
Simulation Results



V(PWM) is the PWM gate voltage. The soft start period runs from 1ms to 2ms. After that the gradually increasing current limit takes over.

The load current is 2A until 12ms.

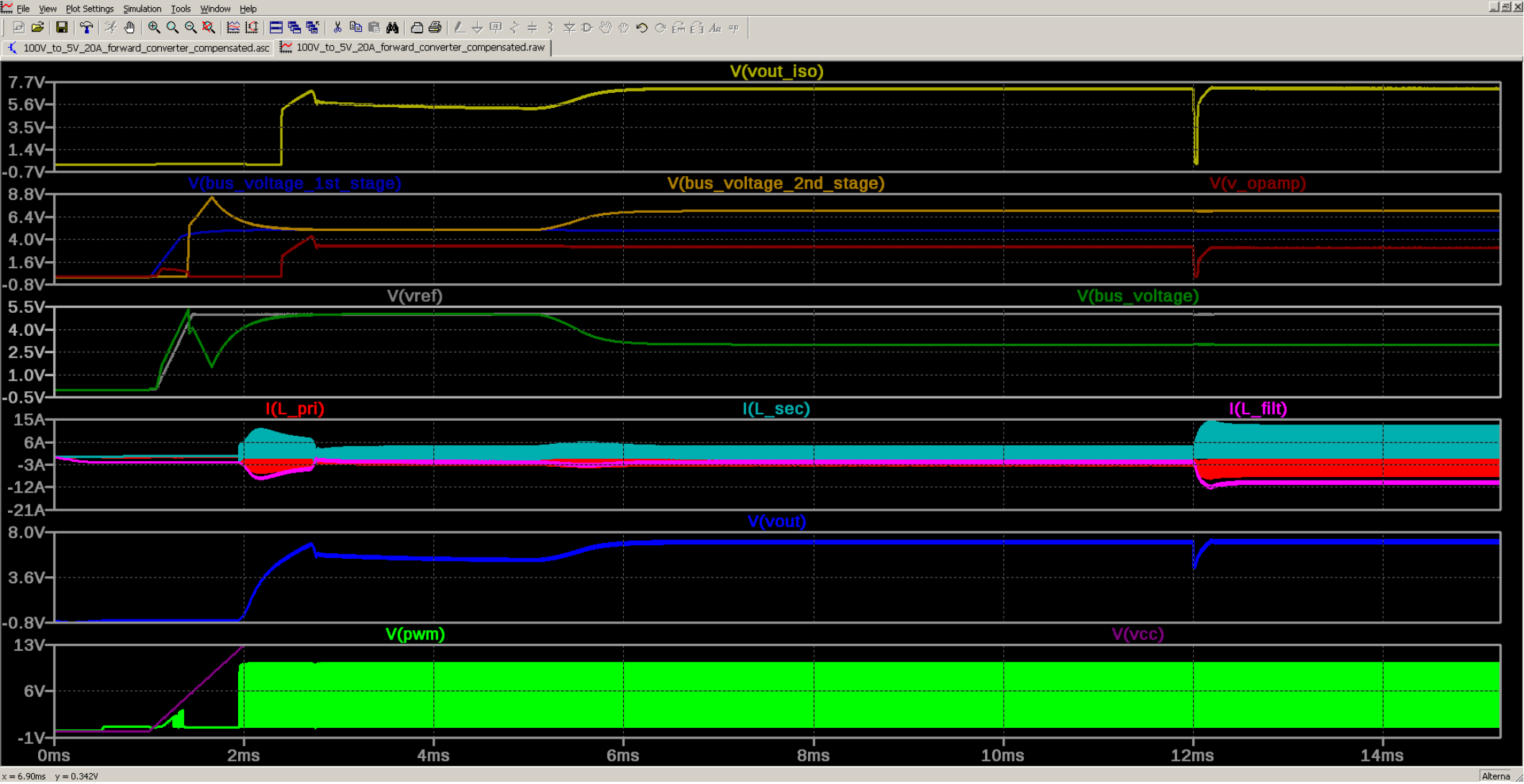
The solar panel bus voltage shifts from 100V to 98V at 5ms. The output voltage rises from 5V to 7V (V(vout)).



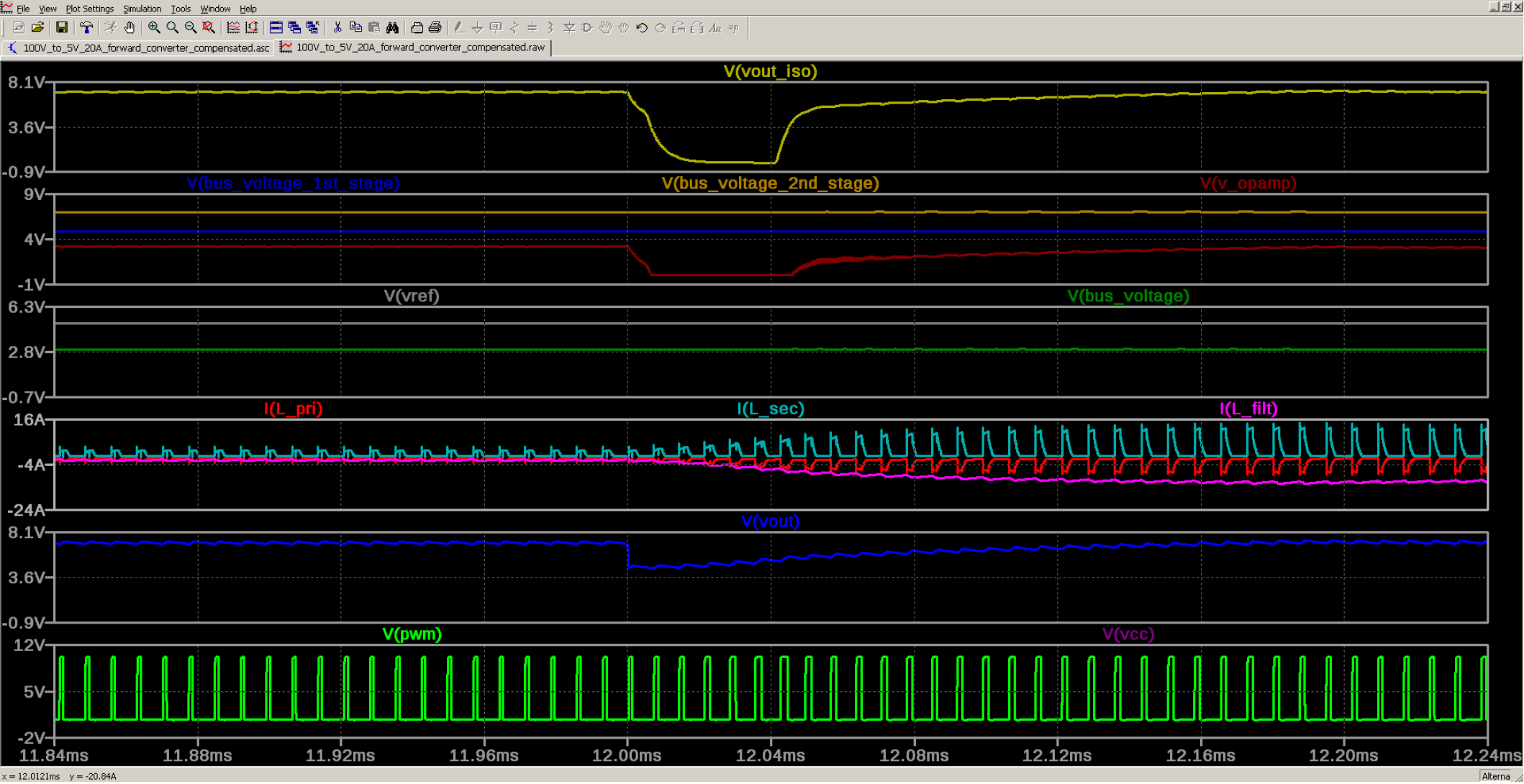
I(Lpri), I(L_sec) and I(L_filt) are the primary, secondary and filter inductor currents, respectively.

V(vref) is the buffered reference voltage. Notice it is very stable.

V(V_opamp) is the EA output voltage. It never saturates to either 13V or 0V; therefore, voltage loop control is maintained.



At 12ms, the load abruptly changes from 2A to 10A. Transformer currents correspondingly increase, but voltage loop control is maintained. There is a slight dip in the output voltage, which is unavoidable, as no voltage control loop has infinite bandwidth. This response comes from the frequency compensation components around the EA.



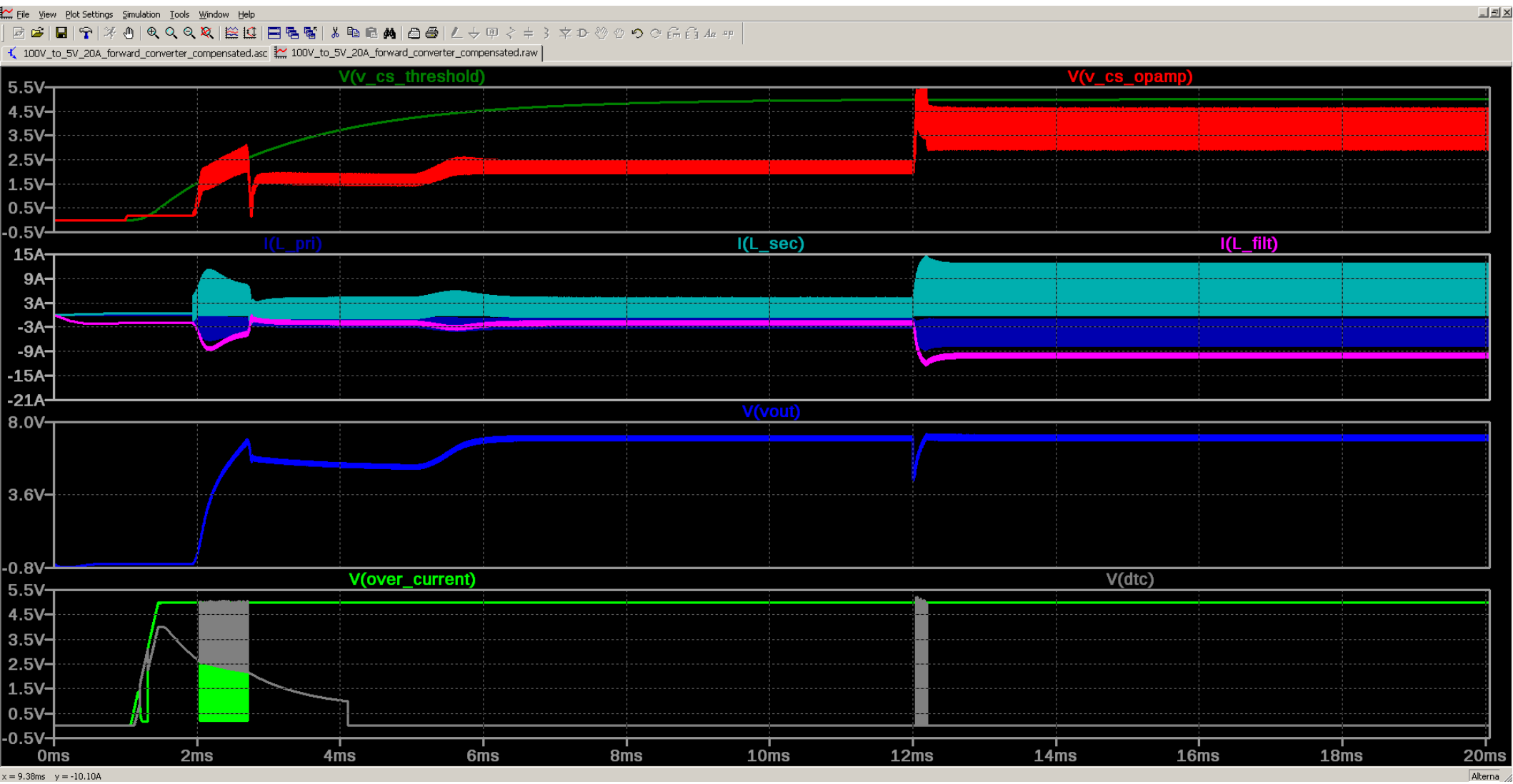
Zoomed in view around 12ms, when load step occurs. Notice that the EA output saturates at ground, but recovers. To correct this, it will require lots of calculations to get the optimal frequency compensation values. I got these results by trial and error.

This shows the transformer and filter inductor currents. Some of them are negative to show relative amplitudes, but the currents are actually all positive.

Bus voltage drops from 100V to 98V at 5ms. Output voltage rises to 7V from 5V. Load step from 2A to 10A occurs at 12ms.

The bottom pane shows the overcurrent comparator slamming DTC to VREF when too much current flows in the primary. This limits the primary current until things stabalize.

Also the current blip during the load step is kept under control, as can be seen by the DTC trace at 12 ms.



Here I show the overcurrent threshold RC waveform in the top pane, and the conditioned primary current sense signal (in red). Notice that even under 10A of load to the 5V output, the primary current stays just under the threshold.

NOTE: All of these are adjustable.