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Unit 4 Lab (Group Lab Assignment)

Time spent on the lab:
10 hours

Table 1:

Hexadecimal Digit	Inputs				Outputs							
	D_3	D_2	D_1	D_0	S_g	S_f	S_e	S_d	S_c	S_b	S_a	(in hex)
0	0	0	0	0	1	0	0	0	0	0	0	40
1	0	0	0	1	1	1	1	1	0	0	1	79
2	0	0	1	0	0	1	0	0	1	0	0	24
3	0	0	1	1	0	1	1	0	0	0	0	30
4	0	1	0	0	0	0	1	1	0	0	1	19
5	0	1	0	1	0	0	1	0	0	1	0	12
6	0	1	1	0	0	0	0	0	0	1	0	2
7	0	1	1	1	1	1	1	1	0	0	0	78
8	1	0	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	1	1	0	0	0	18
A	1	0	1	0	0	0	0	1	0	0	0	8
B	1	0	1	1	0	0	0	0	0	1	1	3
C	1	1	0	0	0	1	0	0	1	1	1	27
D	1	1	0	1	0	1	0	0	0	0	1	21
E	1	1	1	0	0	0	0	0	1	1	0	6
F	1	1	1	1	0	0	0	1	1	1	0	E

Table 1. Truth table for 7-segment display decoder

Equations:

$$S_g = \overline{D_3}\,\overline{D_2}\,\overline{D_1} + \overline{D_3}D_2D_1D_0$$

$$S_f = \overline{D_3}\,\overline{D_2}D_0 + \overline{D_3}D_1D_0 + \overline{D_3}\,\overline{D_2}D_1 + D_3D_2\overline{D_1}$$

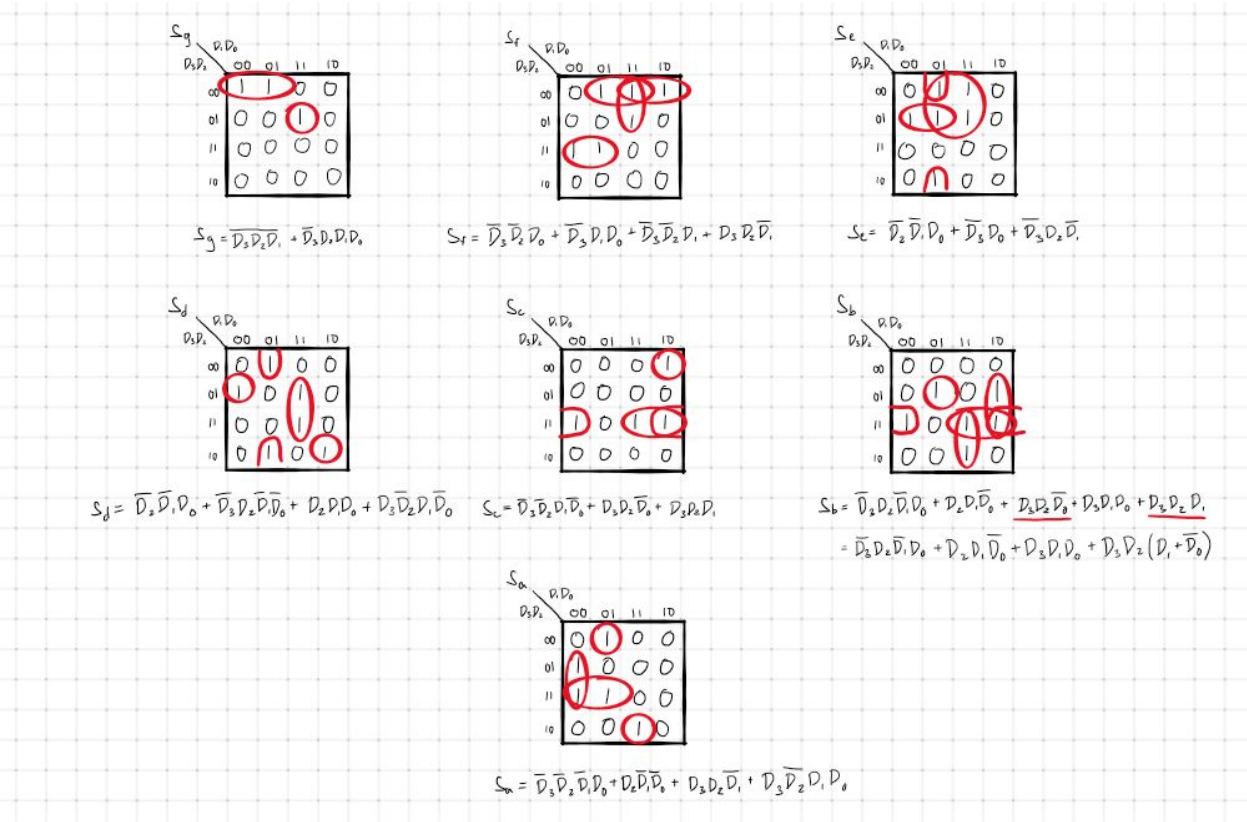
$$S_e = \overline{D_2}\,\overline{D_1}D_0 + \overline{D_3}D_0 + \overline{D_3}D_2\overline{D_1}$$

$$S_d = \overline{D_2}\,\overline{D_1}D_0 + \overline{D_3}D_2\overline{D_1}\,\overline{D_0} + D_2D_1D_0 + D_3\overline{D_2}D_1\overline{D_0}$$

$$S_c = \overline{D_3}\,\overline{D_2}D_1\overline{D_0} + D_3D_2\overline{D_0} + D_3D_2D_1$$

$$S_b = \overline{D_3}D_2\,\overline{D_1}D_0 + D_2D_1\overline{D_0} + D_3D_1D_0 + D_3D_2(D_1 + \overline{D_0})$$

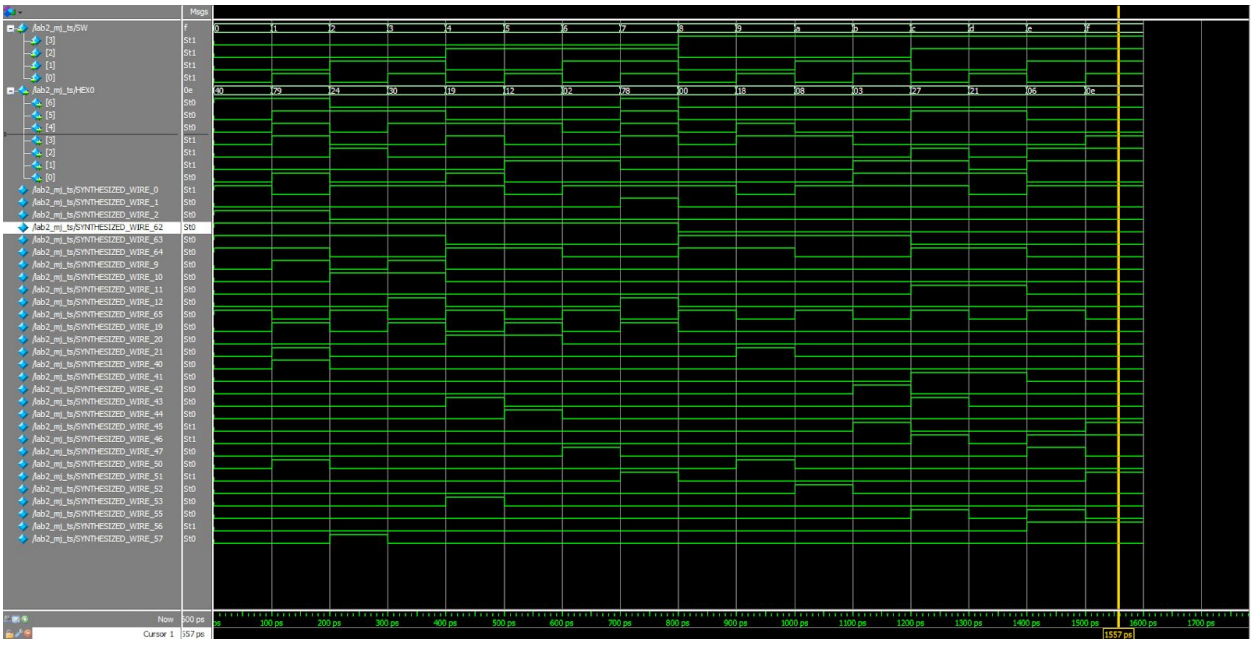
$$S_a = \overline{D_3}\,\overline{D_2}\,\overline{D_1}D_0 + D_2\overline{D_1}\,\overline{D_0} + D_3D_2\overline{D_1} + D_3\overline{D_2}D_1D_0$$



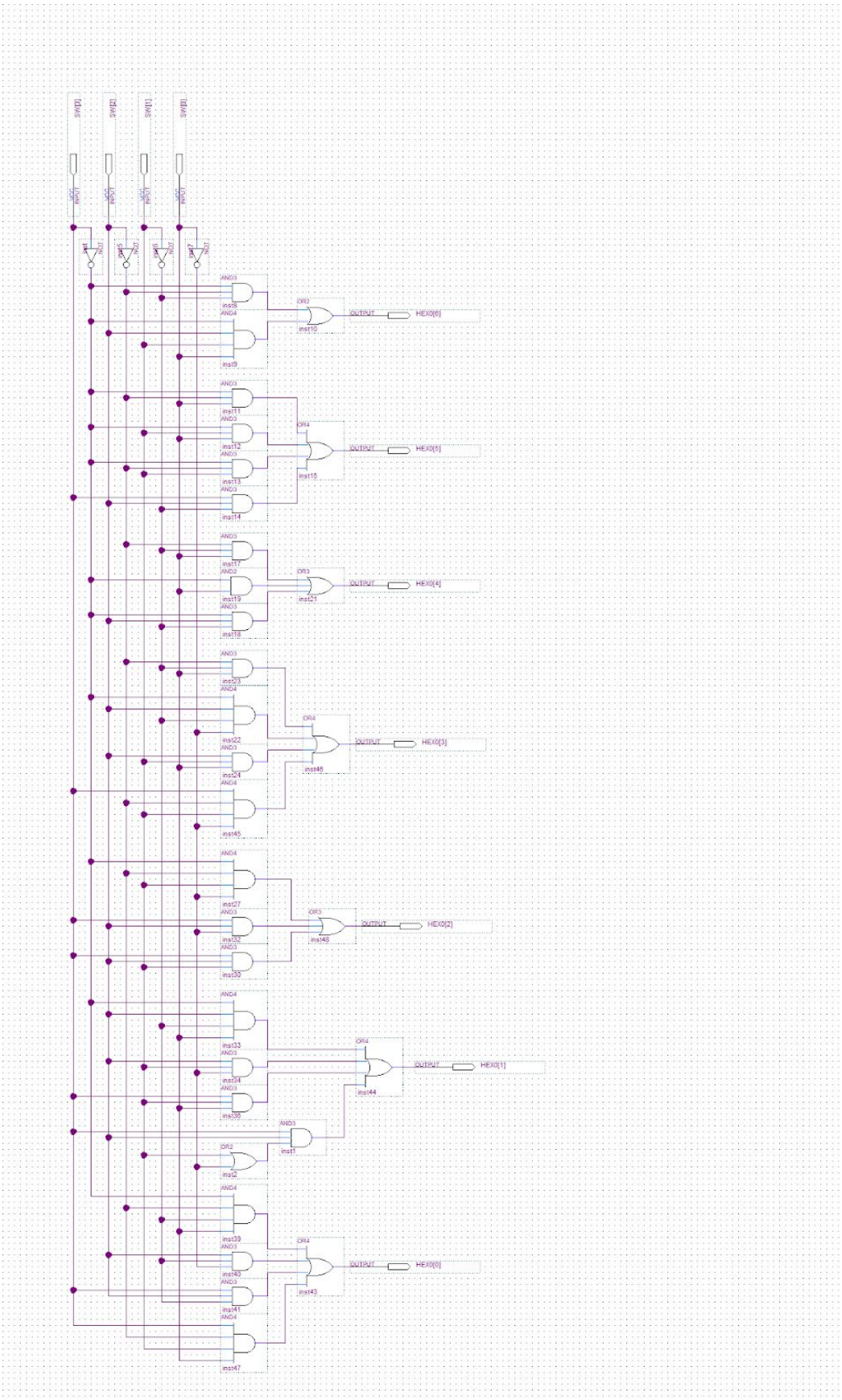
Description:

The design method we used is of a combinational logic design. It takes in 4 inputs and has 7 outputs. We used a combinational logic design because it does not require to be synchronous or asynchronous. It can be used in conjunction with memory or register and some flip flop circuits to turn into a sequential circuit.

Stimulation:

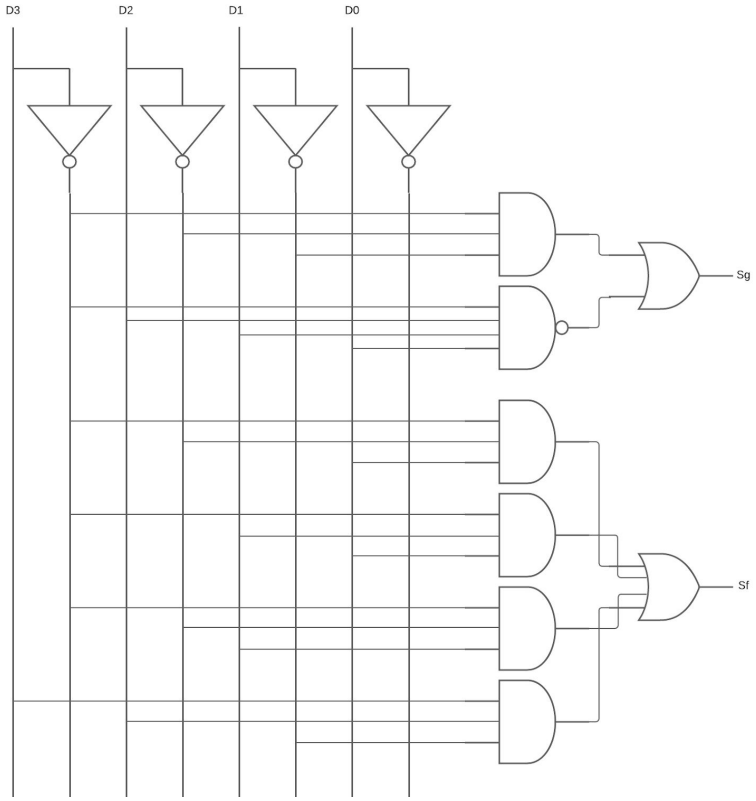


Quatrus schematic:

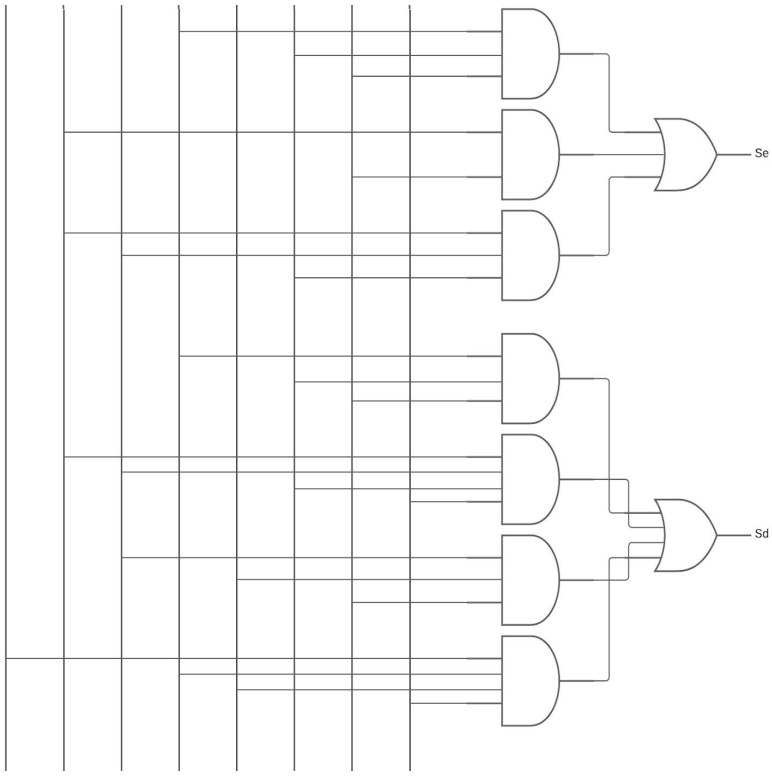


Computer drawn schematic:

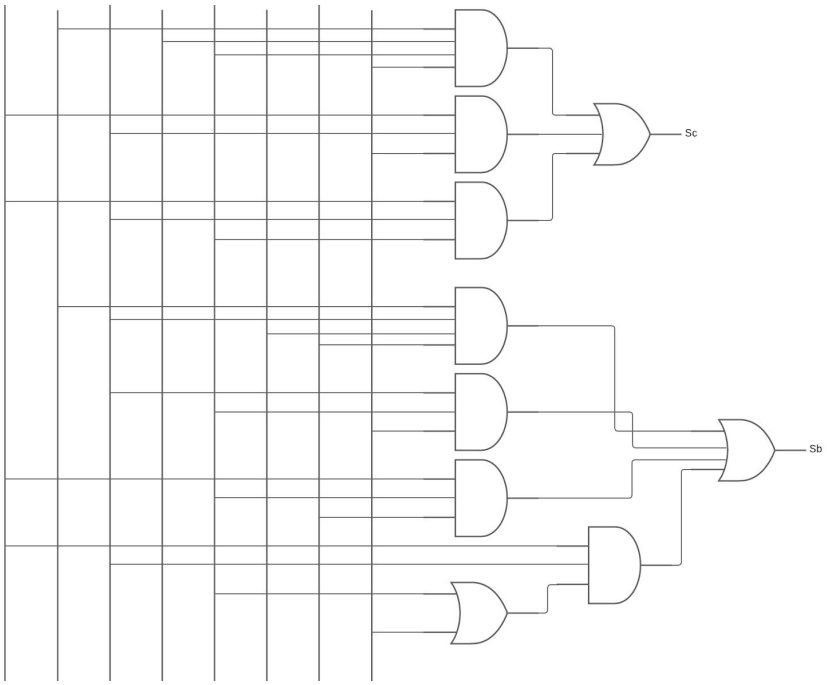
↓ Part 1



↓ Part 2:



↓ Part 3



↓ Part 4