

# AR0134CS

## 1/3-inch 1.2 Mp CMOS Digital Image Sensor with Global Shutter

### Description

The AR0134CS from ON Semiconductor is a 1/3-inch 1.2 Mp CMOS digital image sensor with an active-pixel array of 1280 (H) × 960 (V). It is designed for low light performance and features a global shutter for accurate capture of moving scenes. It includes sophisticated camera functions such as auto exposure control, windowing, scaling, row skip mode, and both video and single frame modes. It is programmable through a simple two-wire serial interface. The AR0134CS produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including scanning and industrial inspection.

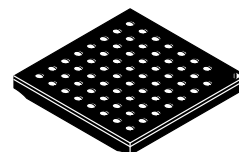
**Table 1. KEY PERFORMANCE PARAMETERS**

| Parameter   | Typical Value   |
|---|---|
| Optical Format                                      | 1/3-inch (6 mm)   |
| Active Pixels                                       | 1280 (H) × 960 (V) = 1.2 Mp                             |
| Pixel Size  | 3.75 μm   |
| Color Filter Array                                  | RGB Bayer or Monochrome                                 |
| Shutter Type  | Global Shutter  |
| Input Clock Range                                   | 6–50 MHz  |
| Output Pixel Clock (Maximum)                        | 74.25 MHz   |
| Output<br>Serial<br>Parallel                        | HiSPi<br>12-bit   |
| Frame Rate<br>Full Resolution<br>720p               | 54 fps<br>60 fps  |
| Responsivity<br>Monochrome<br>Color                 | 6.1 V/lux–sec<br>5.3 V/lux–sec                          |
| SNR <sub>MAX</sub>                                  | 38.6 dB   |
| Dynamic Range                                       | 64 dB   |
| Supply Voltage<br>I/O<br>Digital<br>Analog<br>HiSPi | 1.8 or 2.8 V<br>1.8 V<br>2.8 V<br>0.4 V                 |
| Power Consumption                                   | < 400 mW  |
| Operating Temperature                               | –30°C to + 70°C (Ambient)<br>–30°C to + 80°C (Junction) |
| Package Options                                     | 9 × 9 mm 63-pin iBGA                                    |
|   | 10 × 10 mm 48-pin iLCC                                  |
|   | Bare Die  |

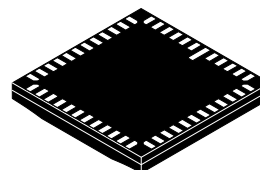


**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)



**IBGA63 9 × 9  
CASE 503AG**



**ILCC48 10 × 10  
CASE 847AE**

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

### Features

- ON Semiconductor's 3<sup>rd</sup> Generation Global Shutter Technology
- Superior Low-light Performance
- HD Video (720p60)
- Video/Single Frame Mode
- Flexible Row-skip Modes
- On-chip AE and Statistics Engine
- Parallel and Serial Output
- Support for External LED or Flash
- Auto Black Level Calibration
- Context Switching

### Applications

- Scene Processing
- Scanning and Machine Vision
- 720p60 Video Applications

## ORDERING INFORMATION

Table 2. ORDERABLE PART NUMBERS

| Part Number       | Description                      |
|-------------------|----------------------------------|
| AR0134CSSM25SUEA0 | Mono, iBGA, 25° Shift            |
| AR0134CSSM00SUEA0 | Mono, iBGA                       |
| AR0134CSSM00SUEAH | Mono, iBGA, Head Board           |
| AR0134CSSM00SUEAD | Mono, iBGA, Demo Kit             |
| AR0134CSSC00SUEA0 | Color, iBGA                      |
| AR0134CSSC00SUEAH | Color, iBGA, Head Board          |
| AR0134CSSC00SUEAD | Color, iBGA, Demo Kit            |
| AR0134CSSM00SPCA0 | Mono, iLCC (Parallel)            |
| AR0134CSSM25SPCA0 | Mono, iLCC (Parallel), 25° Shift |
| AR0134CSSC00SPCA0 | Color, iLCC (Parallel)           |
| AR0134CSSC00SPD20 | Color, Bare Die                  |
| AR0134CSSM00SPD20 | Mono, Bare Die                   |
| AR0134CSSM25SPD20 | Mono, Bare Die, 25° Shift        |

See the ON Semiconductor Device Nomenclature document ([TND310/D](#)) for a full description of the naming convention used for image sensors. For reference

documentation, including information on evaluation kits, please visit our web site at [www.onsemi.com](http://www.onsemi.com).

## GENERAL DESCRIPTION

The ON Semiconductor AR0134CS can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a full-resolution image at 54 frames per second (fps). It outputs 12-bit raw data, using either the parallel or serial (HiSpi) output ports. The device may be operated in video (master) mode or in frame trigger mode.

FRAME\_VALID and LINE\_VALID signals are output on dedicated pins, along with a synchronized pixel clock.

A dedicated FLASH pin can be programmed to control external LED or flash exposure illumination.

The AR0134CS includes additional features to allow application-specific tuning: windowing, adjustable auto-exposure control, auto black level correction, on-board temperature sensor, and row skip and digital binning modes.

The sensor is designed to operate in a wide temperature range ( $-30^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ).

## FUNCTIONAL OVERVIEW

The AR0134CS is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a

single master input clock running between 6 and 50 MHz. The maximum output pixel rate is 74.25 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor.

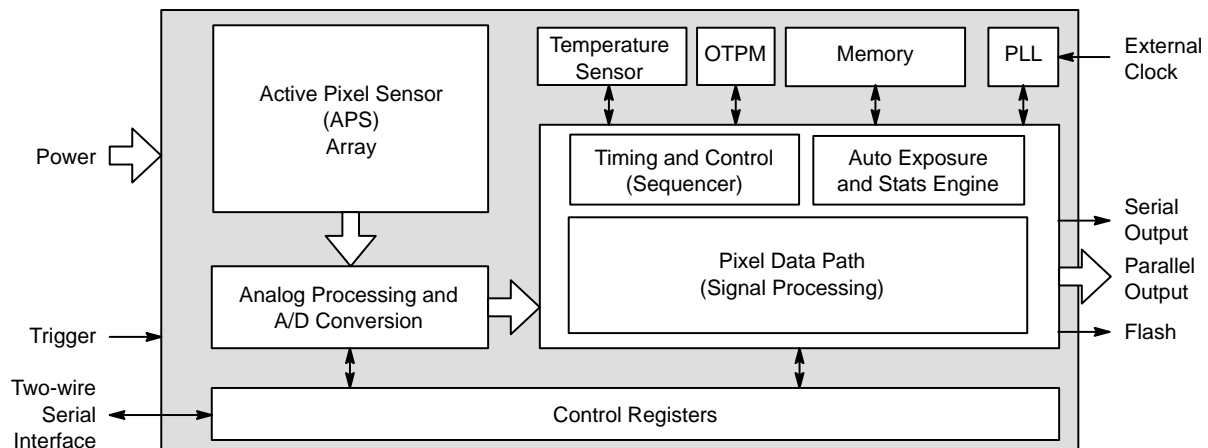


Figure 1. Block Diagram

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.2 Mp Active-Pixel Sensor array. The AR0134CS features global shutter technology for accurate capture of moving images. The exposure of the entire array is controlled by programming the integration time by register setting. All rows simultaneously integrate light prior to readout. Once a row has been read, the data from the

columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 74.25 Mp/s, in parallel to frame and line synchronization signals.

## FEATURES OVERVIEW

The AR0134CS Global Sensor shutter has a wide array of features to enhance functionality and to increase versatility. A summary of features follows. Please refer to the AR0134CS Developer Guide for detailed feature descriptions, register settings, and tuning guidelines and recommendations.

- **Operating Modes**  
The AR0134CS works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two-wire serial interface for both modes. Trigger mode is not compatible with the HiSPi interface.
- **Window Control**  
Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital binning and skipping modes are supported, as are vertical and horizontal mirror operations.
- **Context Switching**  
Context switching may be used to rapidly switch between two sets of register values. Refer to the AR0134CS Developer Guide for a complete set of context switchable registers.
- **Gain**  
The AR0134CS Global Shutter sensor can be configured for analog gain of up to 8x, and digital gain of up to 8x.
- **Automatic Exposure Control**  
The integrated automatic exposure control may be used to ensure optimal settings of exposure and gain are computed and updated every other frame. Refer to the AR0134CS Developer Guide for more details.
- **HiSPi**  
The AR0134CS Global Shutter image sensor supports two or three lanes of Streaming-SP or Packetized-SP protocols of ON Semiconductor's High-Speed Serial Pixel Interface.
- **PLL**  
An on chip PLL provides reference clock flexibility and supports spread spectrum sources for improved EMI performance.

- **Reset**  
The AR0134CS may be reset by a register write, or by a dedicated input pin.
- **Output Enable**  
The AR0134CS output pins may be tri-stated using a dedicated output enable pin.
- **Temperature Sensor**  
The temperature sensor is only guaranteed to be functional when the AR0134CS is initially powered-up or is reset at temperatures at or above 0°C.
- **Black Level Correction**
- **Row Noise Correction**
- **Column Correction**
- **Test Patterns**  
Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to grey, and a walking 1s test pattern.

## PIXEL DATA FORMAT

### Pixel Array Structure

The AR0134CS pixel array is configured as 1412 columns by 1028 rows, (see Figure 2). The dark pixels are optically black and are used internally to monitor black level. Of the right 108 columns, 64 are dark pixels used for row noise correction. Of the top 24 rows of pixels, 12 of the dark rows are used for black level correction. There are 1296 columns by 976 rows of optically active pixels. While the sensor's

format is  $1280 \times 960$ , the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

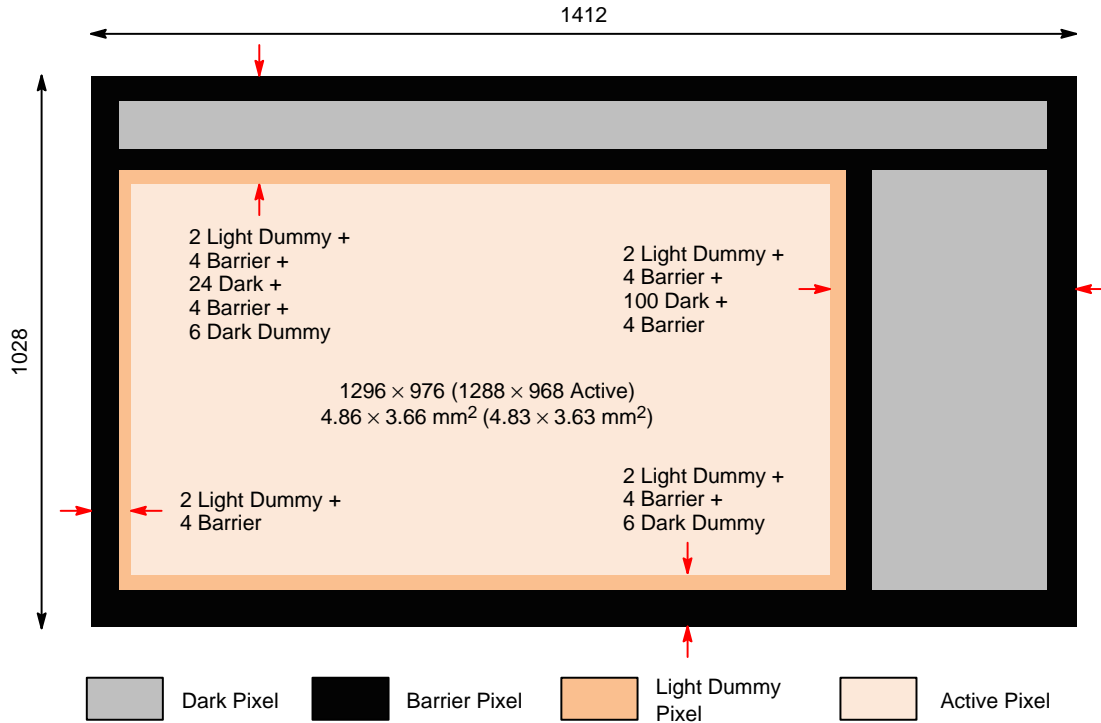


Figure 2. Pixel Array Description

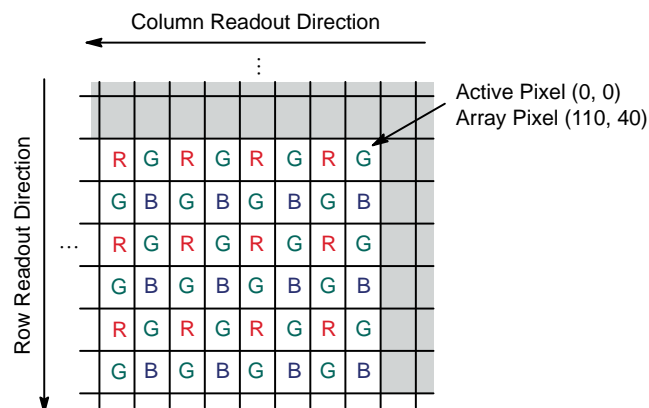


Figure 3. Pixel Color Pattern Detail (Top Right Corner)

### Default Readout Order

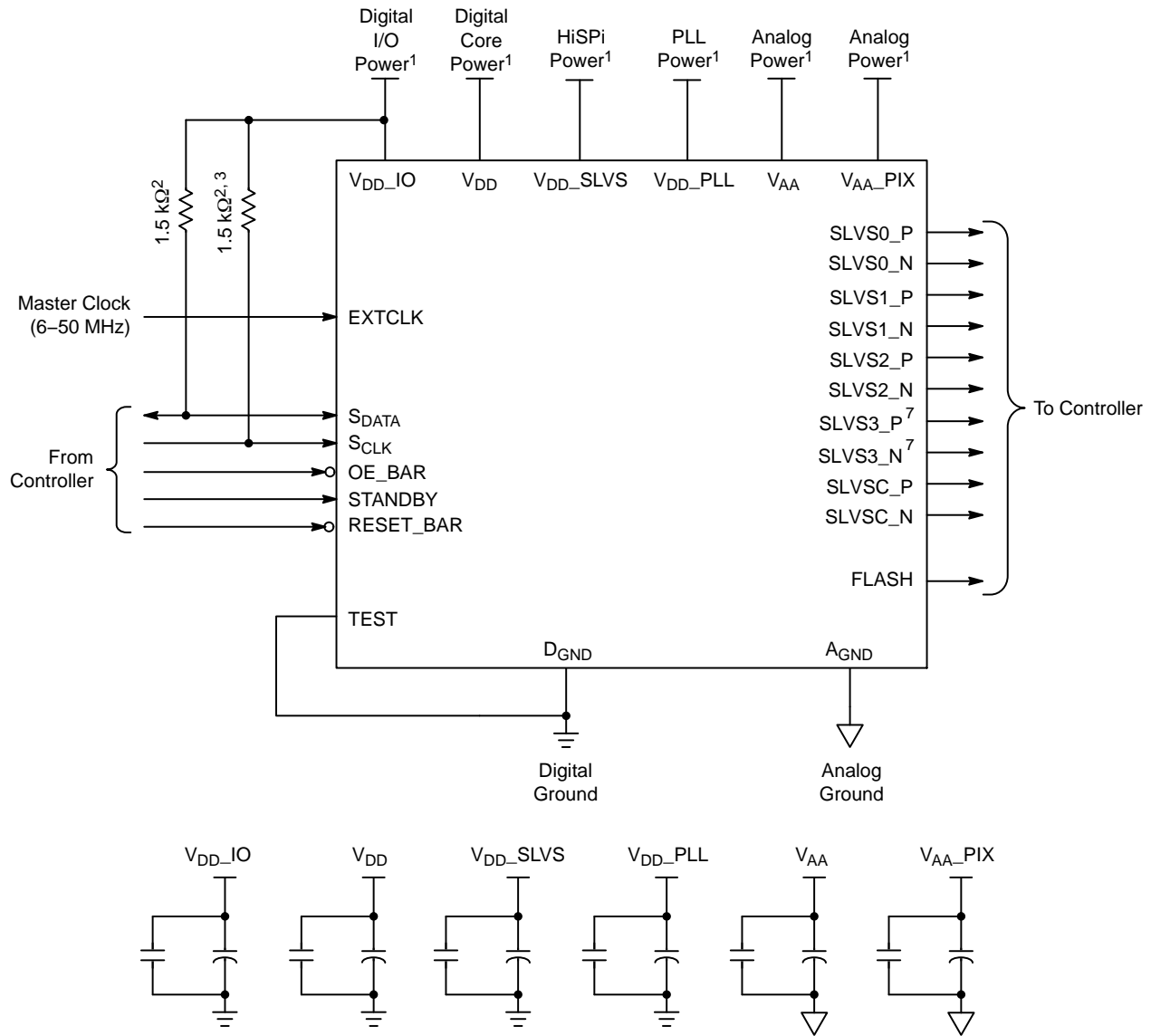
By convention, the sensor core pixel array is shown with the first addressable (logical) pixel (0,0) in the top right corner (see Figure 3). This reflects the actual layout of the

array on the die. Also, the physical location of the first pixel data read out of the sensor in default condition is that of pixel (110, 40).

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## CONFIGURATION AND PINOUT

The figures and tables below show a typical configuration for the AR0134CS image sensor and show the package pinouts.

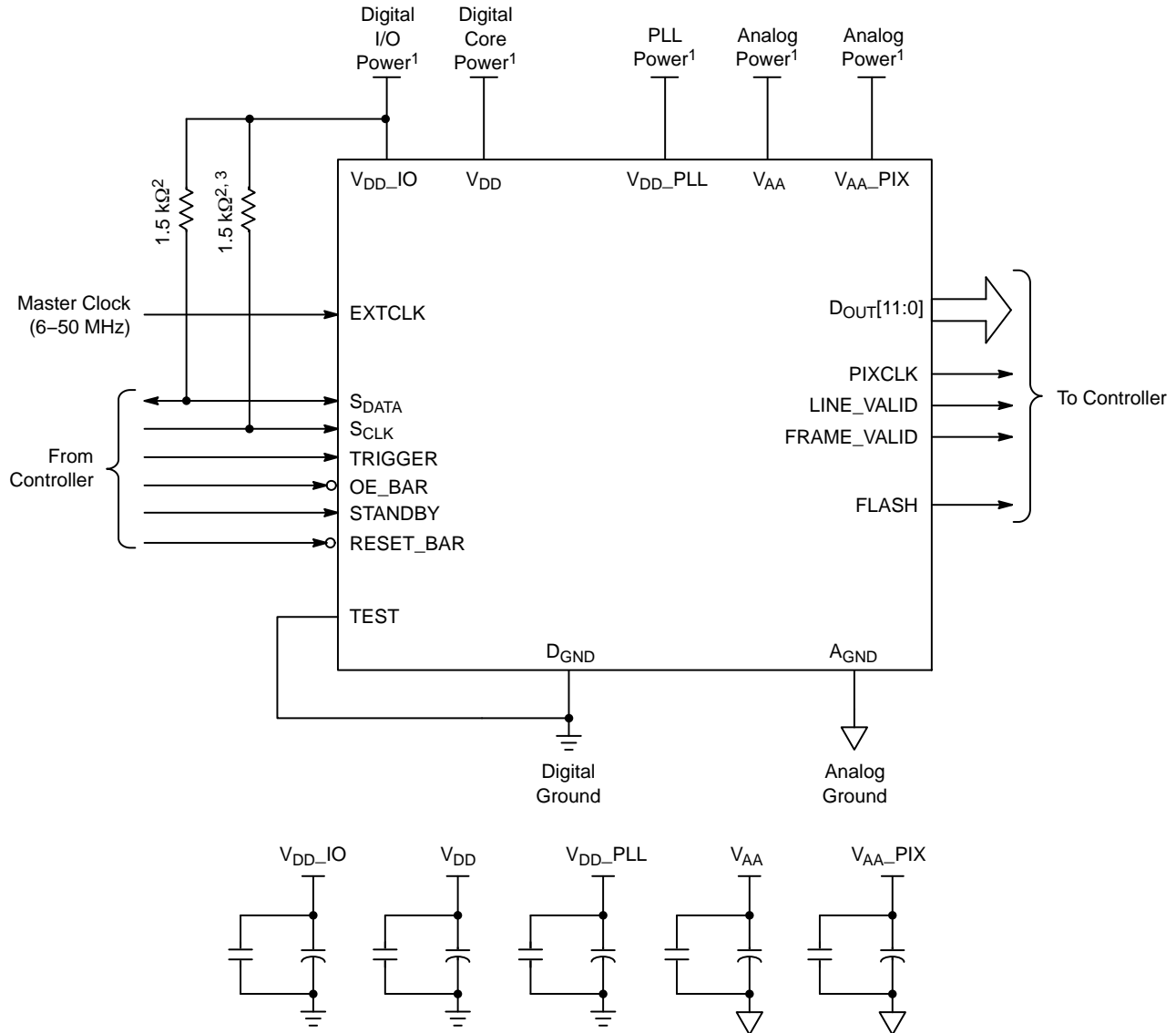


### Notes:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 k $\Omega$ , but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on  $S_{CLK}$  at all times.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. ON Semiconductor recommends that 0.1  $\mu$ F and 10  $\mu$ F decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0134CS demo head-board schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.
7. Although 4 serial lanes are shown, the AR0134CS supports only 2- or 3-lane HiSPi.

**Figure 4. Serial 4-lane HiSPi Interface**

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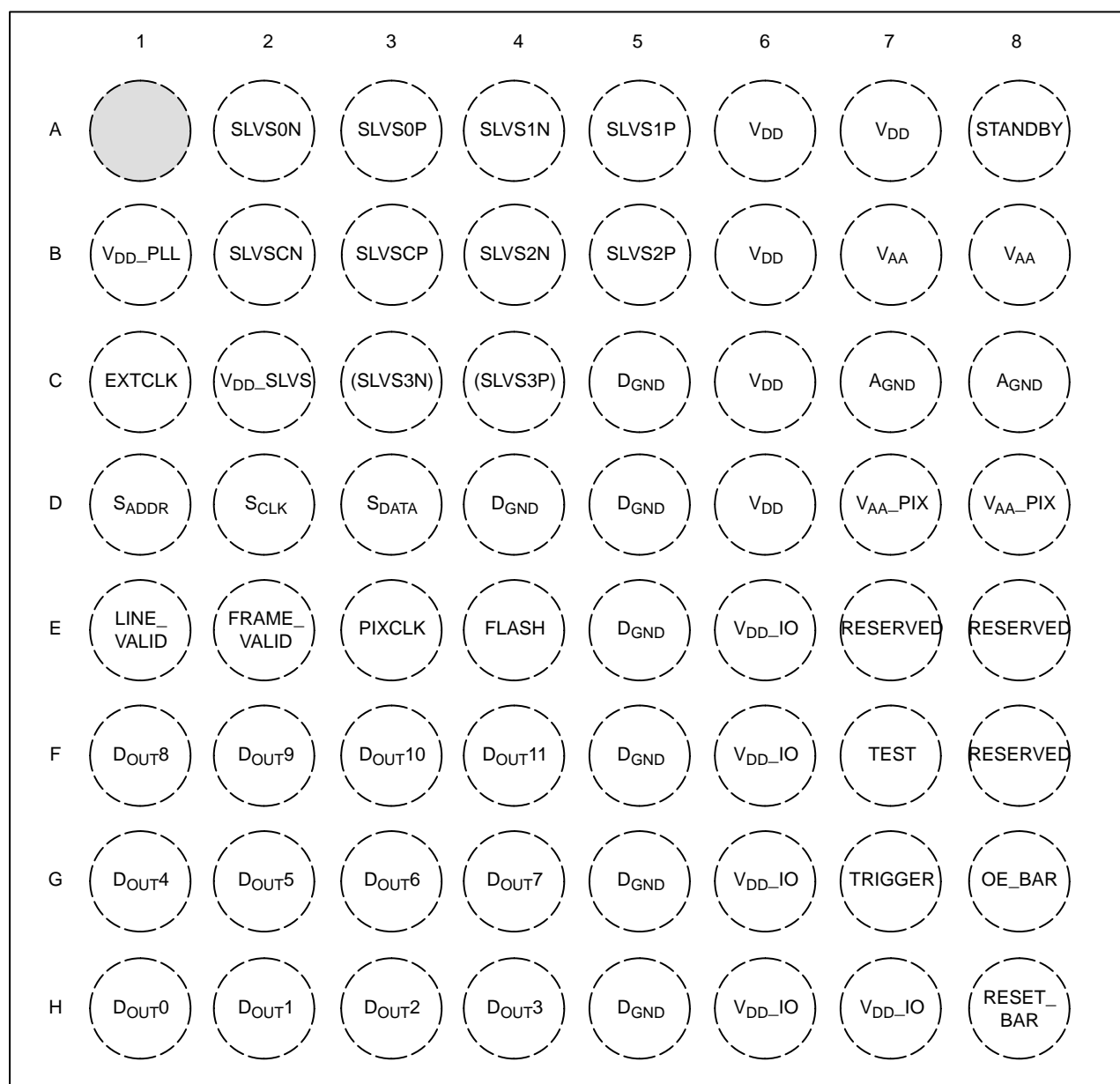


## Notes:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 k $\Omega$ , but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on  $S_{CLK}$  at all times.
4. The serial interface output pads can be left unconnected if the parallel output interface is used.
5. ON Semiconductor recommends that 0.1  $\mu$ F and 10  $\mu$ F decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0134CS demo head-board schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

**Figure 5. Parallel Pixel Data Interface**

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Top View  
(Ball Down)

Figure 6. 9 × 9 mm 63-ball iBGA Package

Table 3. PIN DESCRIPTIONS – 63-BALL IBGA PACKAGE

| Name                | iBGA Pin | Type   | Description                               |
|---------------------|----------|--------|---|
| SLVS0_N             | A2       | Output | HiSPi serial data, lane 0, differential N |
| SLVS0_P             | A3       | Output | HiSPi serial data, lane 0, differential P |
| SLVS1_N             | A4       | Output | HiSPi serial data, lane 1, differential N |
| SLVS1_P             | A5       | Output | HiSPi serial data, lane 1, differential P |
| STANDBY             | A8       | Input  | Standby-mode enable pin (active HIGH)     |
| V <sub>DD_PLL</sub> | B1       | Power  | PLL power                                 |
| SLVSC_N             | B2       | Output | HiSPi serial DDR clock differential N     |

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**Table 3. PIN DESCRIPTIONS – 63-BALL IBGA PACKAGE** (continued)

| Name                  | iBGA Pin                   | Type   | Description   |
|-----------------------|----------------------------|--------|---|
| SLVSC_P               | B3                         | Output | HiSPi serial DDR clock differential P   |
| SLVS2_N               | B4                         | Output | HiSPi serial data, lane 2, differential N   |
| SLVS2_P               | B5                         | Output | HiSPi serial data, lane 2, differential P   |
| V <sub>AA</sub>       | B7, B8                     | Power  | Analog power  |
| EXTCLK                | C1                         | Input  | External input clock  |
| V <sub>DD</sub> _SLVS | C2                         | Power  | HiSPi power (May leave unconnected if parallel interface is used)                       |
| SLVS3_N               | C3                         | Output | (Unsupported) HiSPi serial data, lane 3, differential N                                 |
| SLVS3_P               | C4                         | Output | (Unsupported) HiSPi serial data, lane 3, differential P                                 |
| D <sub>GND</sub>      | C5, D4, D5, E5, F5, G5, H5 | Power  | Digital GND   |
| V <sub>DD</sub>       | A6, A7, B6, C6, D6         | Power  | Digital power   |
| A <sub>GND</sub>      | C7, C8                     | Power  | Analog GND  |
| S <sub>ADDR</sub>     | D1                         | Input  | Two-Wire Serial address select  |
| S <sub>CLK</sub>      | D2                         | Input  | Two-Wire Serial clock input   |
| S <sub>DATA</sub>     | D3                         | I/O    | Two-Wire Serial data I/O  |
| V <sub>AA</sub> _PIX  | D7, D8                     | Power  | Pixel power   |
| LINE_VALID            | E1                         | Output | Asserted when D <sub>OUT</sub> line data is valid                                       |
| FRAME_VALID           | E2                         | Output | Asserted when D <sub>OUT</sub> frame data is valid                                      |
| PIXCLK                | E3                         | Output | Pixel clock out. D <sub>OUT</sub> is valid on rising edge of this clock                 |
| FLASH                 | E4                         | Output | Control signal to drive external light sources  |
| V <sub>DD</sub> _IO   | E6, F6, G6, H6, H7         | Power  | I/O supply power  |
| D <sub>OUT8</sub>     | F1                         | Output | Parallel pixel data output  |
| D <sub>OUT9</sub>     | F2                         | Output | Parallel pixel data output  |
| D <sub>OUT10</sub>    | F3                         | Output | Parallel pixel data output  |
| D <sub>OUT11</sub>    | F4                         | Output | Parallel pixel data output (MSB)  |
| TEST                  | F7                         | Input  | Manufacturing test enable pin (connect to D <sub>GND</sub> )                            |
| D <sub>OUT4</sub>     | G1                         | Output | Parallel pixel data output  |
| D <sub>OUT5</sub>     | G2                         | Output | Parallel pixel data output  |
| D <sub>OUT6</sub>     | G3                         | Output | Parallel pixel data output  |
| D <sub>OUT7</sub>     | G4                         | Output | Parallel pixel data output  |
| TRIGGER               | G7                         | Input  | Exposure synchronization input (Connect to D <sub>GND</sub> if HiSPi interface is used) |
| OE_BAR                | G8                         | Input  | Output enable (active LOW)  |
| D <sub>OUT0</sub>     | H1                         | Output | Parallel pixel data output (LSB)  |
| D <sub>OUT1</sub>     | H2                         | Output | Parallel pixel data output  |
| D <sub>OUT2</sub>     | H3                         | Output | Parallel pixel data output  |
| D <sub>OUT3</sub>     | H4                         | Output | Parallel pixel data output  |
| RESET_BAR             | H8                         | Input  | Asynchronous reset (active LOW). All settings are restored to factory default           |
| Reserved              | E7, E8, F8                 | N/A    | Reserved (do not connect)   |



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|    |             |  |    |          |    |    |
|----|-------------|--|----|----------|----|----|
| 19 | VDD         |  | 6  | DGND     |    |    |
| 20 | NC          |  | 5  | EXTCLK   |    |    |
| 21 | NC          |  | 4  | VDD_PLL  |    |    |
| 22 | STANDBY     |  | 3  | DOUT6    |    |    |
| 23 | OE_BAR      |  | 2  | DOUT5    |    |    |
| 24 | SADDR       |  | 1  | DOUT4    |    |    |
| 25 | TEST        |  | 48 | DOUT3    |    |    |
| 26 | FLASH       |  | 47 | DOUT2    |    |    |
| 27 | TRIGGER     |  | 46 | DOUT1    |    |    |
| 28 | FRAME_VALID |  | 45 | DOUT0    |    |    |
| 29 | LINE_VALID  |  | 44 | DGND     |    |    |
| 30 | DGND        |  | 43 | NC       |    |    |
| 7  | DOUT7       |  |    |          | NC | 42 |
| 8  | DOUT8       |  |    |          | NC | 41 |
| 9  | DOUT9       |  |    | VAA      | 40 |    |
| 10 | DOUT10      |  |    | AGND     | 39 |    |
| 11 | DOUT11      |  |    | VAA_PIX  | 38 |    |
| 12 | VDD_IO      |  |    | VAA_PIX  | 37 |    |
| 13 | PIXCLK      |  |    | VAA      | 36 |    |
| 14 | VDD         |  |    | AGND     | 35 |    |
| 15 | SCLK        |  |    | VAA      | 34 |    |
| 16 | SDATA       |  |    | Reserved | 33 |    |
| 17 | RESET_BAR   |  |    | Reserved | 32 |    |
| 18 | VDD_IO      |  |    | Reserved | 31 |    |

**Figure 7. 10 × 10 mm 48-pin iLCC Package, Parallel Output**

**Table 4. PIN DESCRIPTIONS – 48-PIN ILCC PACKAGE, PARALLEL**

| Pin Number | Name                 | Type   | Description                |
|------------|----------------------|--------|----------------------------|
| 1          | D <sub>OUT</sub> 4   | Output | Parallel pixel data output |
| 2          | D <sub>OUT</sub> 5   | Output | Parallel pixel data output |
| 3          | D <sub>OUT</sub> 6   | Output | Parallel pixel data output |
| 4          | V <sub>DD</sub> _PLL | Power  | PLL power                  |
| 5          | EXTCLK               | Input  | External input clock       |
| 6          | D <sub>GND</sub>     | Power  | Digital ground             |
| 7          | D <sub>OUT</sub> 7   | Output | Parallel pixel data output |
| 8          | D <sub>OUT</sub> 8   | Output | Parallel pixel data output |
| 9          | D <sub>OUT</sub> 9   | Output | Parallel pixel data output |

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**Table 4. PIN DESCRIPTIONS – 48-PIN ILCC PACKAGE, PARALLEL** (continued)

| Pin Number | Name                 | Type   | Description   |
|------------|----------------------|--------|---|
| 10         | D <sub>OUT</sub> 10  | Output | Parallel pixel data output  |
| 11         | D <sub>OUT</sub> 11  | Output | Parallel pixel data output (MSB)  |
| 12         | V <sub>DD</sub> _IO  | Power  | I/O supply power  |
| 13         | PIXCLK               | Output | Pixel clock out. D <sub>OUT</sub> is valid on rising edge of this clock       |
| 14         | V <sub>DD</sub>      | Power  | Digital power   |
| 15         | S <sub>CLK</sub>     | Input  | Two-Wire Serial clock input   |
| 16         | S <sub>DATA</sub>    | I/O    | Two-Wire Serial data I/O  |
| 17         | RESET_BAR            | Input  | Asynchronous reset (active LOW). All settings are restored to factory default |
| 18         | V <sub>DD</sub> _IO  | Power  | I/O supply power  |
| 19         | V <sub>DD</sub>      | Power  | Digital power   |
| 20         | NC                   |        | No connection   |
| 21         | NC                   |        | No connection   |
| 22         | STANDBY              | Input  | Standby-mode enable pin (active HIGH)   |
| 23         | OE_BAR               | Input  | Output enable (active LOW)  |
| 24         | S <sub>ADDR</sub>    | Input  | Two-Wire Serial address select  |
| 25         | TEST                 | Input  | Manufacturing test enable pin (connect to D <sub>GND</sub> )                  |
| 26         | FLASH                | Output | Flash output control  |
| 27         | TRIGGER              | Input  | Exposure synchronization input  |
| 28         | FRAME_VALID          | Output | Asserted when D <sub>OUT</sub> frame data is valid                            |
| 29         | LINE_VALID           | Output | Asserted when D <sub>OUT</sub> line data is valid                             |
| 30         | D <sub>GND</sub>     | Power  | Digital ground  |
| 31         | Reserved             | N/A    | Reserved (do not connect)   |
| 32         | Reserved             | N/A    | Reserved (do not connect)   |
| 33         | Reserved             | N/A    | Reserved (do not connect)   |
| 34         | V <sub>AA</sub>      | Power  | Analog power  |
| 35         | A <sub>GND</sub>     | Power  | Analog ground   |
| 36         | V <sub>AA</sub>      | Power  | Analog power  |
| 37         | V <sub>AA</sub> _PIX | Power  | Pixel power   |
| 38         | V <sub>AA</sub> _PIX | Power  | Pixel power   |
| 39         | A <sub>GND</sub>     | Power  | Analog ground   |
| 40         | V <sub>AA</sub>      | Power  | Analog power  |
| 41         | NC                   |        | No connection   |
| 42         | NC                   |        | No connection   |
| 43         | NC                   |        | No connection   |
| 44         | D <sub>GND</sub>     | Power  | Digital ground  |
| 45         | D <sub>OUT</sub> 0   | Output | Parallel pixel data output (LSB)  |
| 46         | D <sub>OUT</sub> 1   | Output | Parallel pixel data output  |
| 47         | D <sub>OUT</sub> 2   | Output | Parallel pixel data output  |
| 48         | D <sub>OUT</sub> 3   | Output | Parallel pixel data output  |

## TWO-WIRE SERIAL REGISTER INTERFACE

The two-wire serial interface bus enables read/write access to control and status registers within the AR0134CS.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD\_IO off-chip by a 1.5 kΩ resistor. Either the slave or master device can drive SDATA LOW – the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two-wire serial interface specification allow the slave device to drive SCLK LOW; the AR0134CS uses SCLK as an input only and therefore never drives it LOW.

### Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements:

1. a (repeated) start condition
2. a slave address/data direction byte
3. an (a no) acknowledge bit
4. a message byte
5. a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

### Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

### Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

### Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

### Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ.

The default slave addresses used by the AR0134CS are 0x20 (write address) and 0x21 (read address) in accordance with the specification. Alternate slave addresses of 0x30 (write address) and 0x31 (read address) can be selected by enabling and asserting the SADDR input.

An alternate slave address can also be programmed through R0x31FC.

### Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

### Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

### No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

### Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a “0” indicates a write and a “1” indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which the WRITE should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave’s internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

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## Single READ from Random Location

This sequence (Figure 8) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit read slave address/data direction byte and clocks out one byte of

register data. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. Figure 8 shows how the internal register address maintained by the AR0134CS is loaded and incremented as the sequence proceeds.

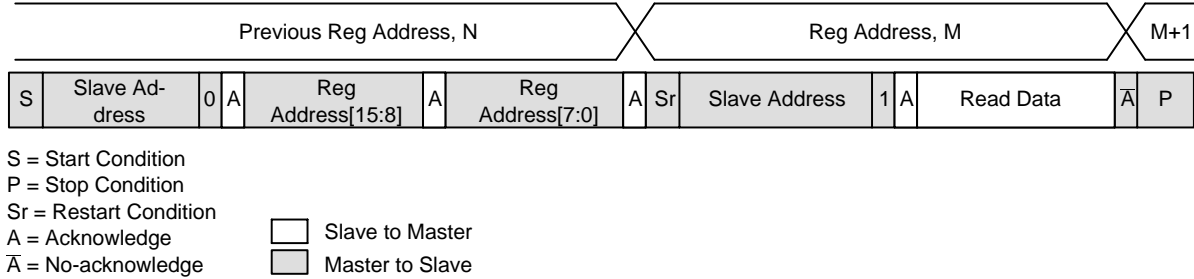


Figure 8. Single READ from Random Location

## Single READ from Current Location

This sequence (Figure 9) performs a read using the current value of the AR0134CS internal register address.

The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

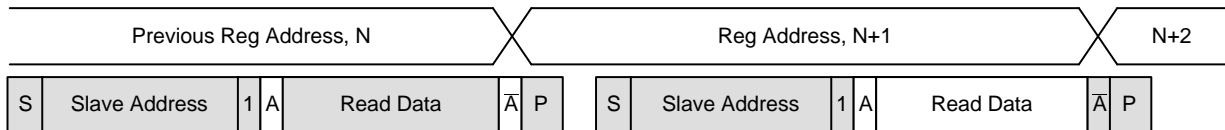


Figure 9. Single READ from Current Location

## Sequential READ, Start from Random Location

This sequence (Figure 10) starts in the same way as the single READ from random location (Figure 8). Instead of generating a no-acknowledge bit after the first byte of data

has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

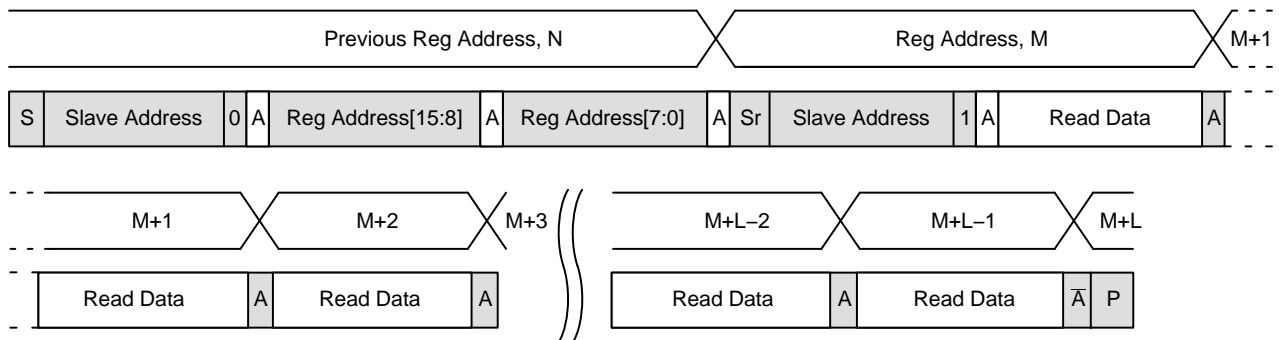


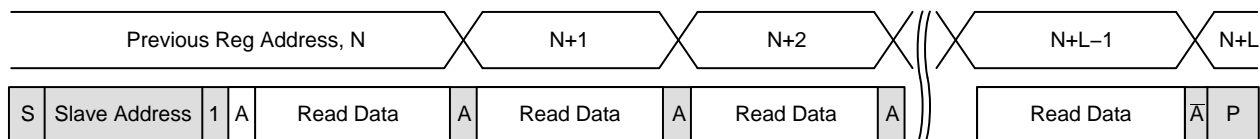
Figure 10. Sequential READ, Start from Random Location

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### Sequential READ, Start from Current Location

This sequence (Figure 11) starts in the same way as the single READ from current location (Figure 9). Instead of generating a no-acknowledge bit after the first byte of data

has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

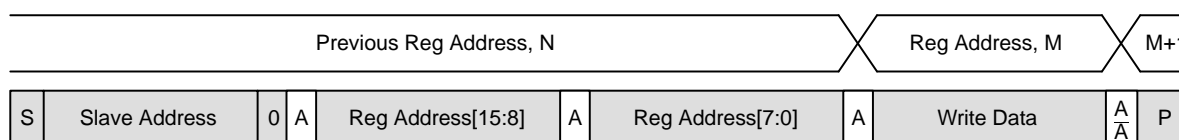


**Figure 11. Sequential READ, Start from Current Location**

### Single WRITE to Random Location

This sequence (Figure 12) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH

then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

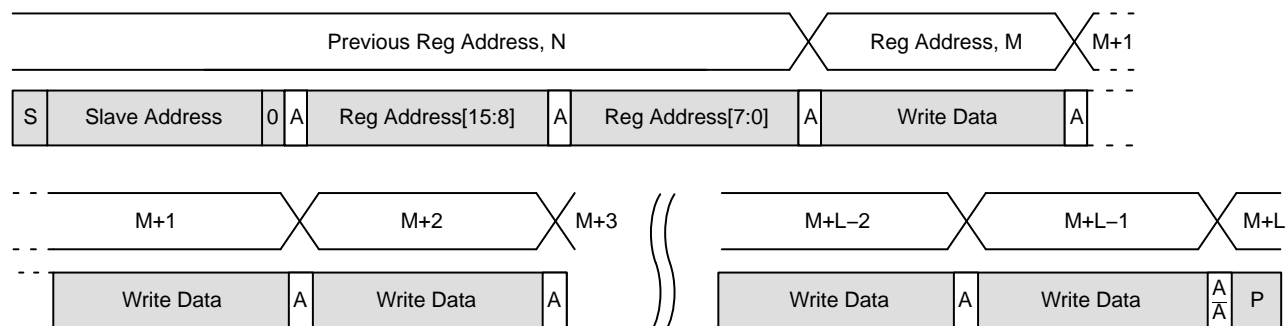


### Figure 12. Single WRITE to Random Location

### Sequential WRITE, Start at Random Location

This sequence (Figure 13) starts in the same way as the single WRITE to random location (Figure 12). Instead of generating a no-acknowledge bit after the first byte of data

has been transferred, the master generates an acknowledge bit and continues to perform byte WRITES until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.



**Figure 13. Sequential WRITE, Start at Random Location**

## ELECTRICAL SPECIFICATIONS

Unless otherwise stated, the following specifications apply to the following conditions:

$V_{DD} = 1.8 \text{ V} -0.10/+0.15$ ;

$V_{DD\_IO} = V_{DD\_PLL} = V_{AA} = V_{AA\_PIX} = 2.8 \text{ V} \pm 0.3 \text{ V}$ ;

$V_{DD\_SLVS} = 0.4 \text{ V} -0.1/+0.2$ ;

$T_A = -30^\circ\text{C to } +70^\circ\text{C}$ ;

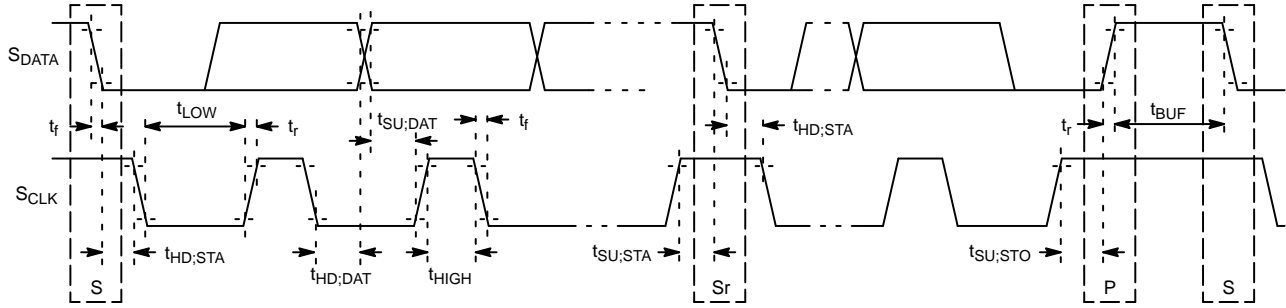
Output Load = 10 pF;

PIXCLK Frequency = 74.25 MHz;

HiSpi off.

### Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface ( $S_{CLK}$ ,  $S_{DATA}$ ) are shown in Figure 14 and Table 5.



NOTE: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Figure 14. Two-Wire Serial Bus Timing Parameters

Table 5. TWO-WIRE SERIAL BUS CHARACTERISTICS

( $f_{EXTCLK} = 27 \text{ MHz}$ ;  $V_{DD} = 1.8 \text{ V}$ ;  $V_{DD\_IO} = 2.8 \text{ V}$ ;  $V_{AA} = 2.8 \text{ V}$ ;  $V_{AA\_PIX} = 2.8 \text{ V}$ ;  $V_{DD\_PLL} = 2.8 \text{ V}$ ;  $V_{DD\_DAC} = 2.8 \text{ V}$ ;  $T_A = 25^\circ\text{C}$ )

| Parameter   | Symbol       | Standard Mode |               | Fast-Mode              |              | Unit          |
|---|--------------|---------------|---------------|------------------------|--------------|---------------|
|   |              | Min           | Max           | Min                    | Max          |               |
| $S_{CLK}$ Clock Frequency                             | $f_{SCL}$    | 0             | 100           | 0                      | 400          | kHz           |
| Hold Time (Repeated) START Condition                  |              |               |               |                        |              |               |
| After This Period, the First Clock Pulse is Generated | $t_{HD;STA}$ | 4.0           | –             | 0.6                    | –            | $\mu\text{s}$ |
| LOW Period of the $S_{CLK}$ Clock                     | $t_{LOW}$    | 4.7           | –             | 1.3                    | –            | $\mu\text{s}$ |
| HIGH Period of the $S_{CLK}$ Clock                    | $t_{HIGH}$   | 4.0           | –             | 0.6                    | –            | $\mu\text{s}$ |
| Set-up Time for a Repeated START Condition            | $t_{SU;STA}$ | 4.7           | –             | 0.6                    | –            | $\mu\text{s}$ |
| Data Hold Time  | $t_{HD;DAT}$ | 0 (Note 4)    | 3.45 (Note 5) | 0 (Note 6)             | 0.9 (Note 5) | $\mu\text{s}$ |
| Data Set-up Time                                      | $t_{SU;DAT}$ | 250           | –             | 100 (Note 6)           | –            | ns            |
| Rise Time of both $S_{DATA}$ and $S_{CLK}$ Signals    | $t_r$        | –             | 1000          | $20 + 0.1C_b$ (Note 7) | 300          | ns            |
| Fall Time of both $S_{DATA}$ and $S_{CLK}$ Signals    | $t_f$        | –             | 300           | $20 + 0.1C_b$ (Note 7) | 300          | ns            |
| Set-up Time for STOP Condition                        | $t_{SU;STO}$ | 4.0           | –             | 0.6                    | –            | $\mu\text{s}$ |
| Bus Free Time between a STOP and START Condition      | $t_{BUF}$    | 4.7           | –             | 1.3                    | –            | $\mu\text{s}$ |
| Capacitive Load for each Bus Line                     | $C_b$        | –             | 400           | –                      | 400          | pF            |
| Serial Interface Input Pin Capacitance                | $C_{IN\_SI}$ | –             | 3.3           | –                      | 3.3          | pF            |

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**Table 5. TWO-WIRE SERIAL BUS CHARACTERISTICS** (continued)

( $f_{EXTCLK} = 27 \text{ MHz}$ ;  $V_{DD} = 1.8 \text{ V}$ ;  $V_{DD\_IO} = 2.8 \text{ V}$ ;  $V_{AA} = 2.8 \text{ V}$ ;  $V_{AA\_PIX} = 2.8 \text{ V}$ ;  $V_{DD\_PLL} = 2.8 \text{ V}$ ;  $V_{DD\_DAC} = 2.8 \text{ V}$ ;  $T_A = 25^\circ\text{C}$ )

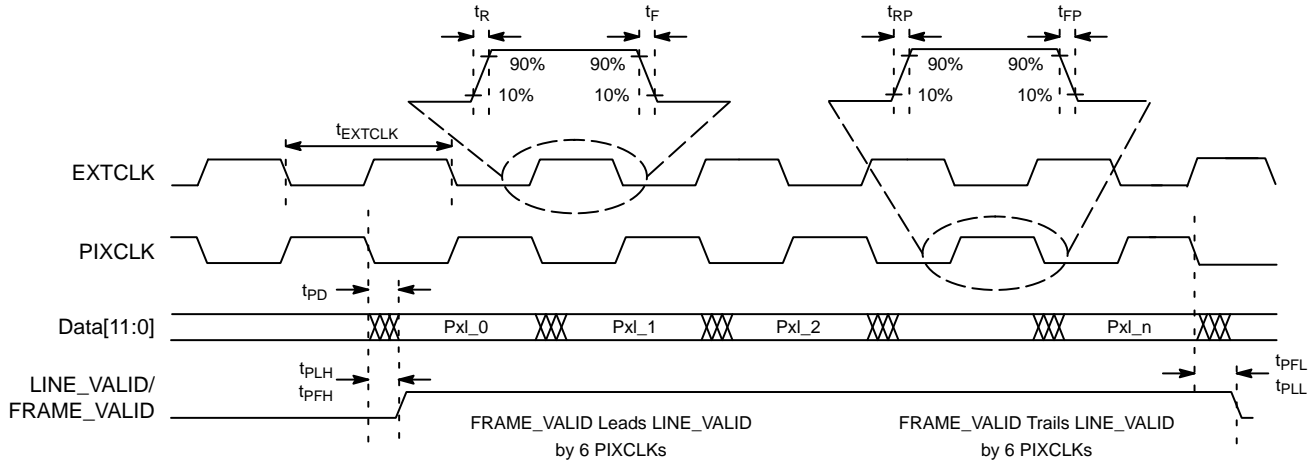
| Parameter                              | Symbol   | Standard Mode |     | Fast-Mode |     | Unit       |
|--|----------|---------------|-----|-----------|-----|------------|
|  |          | Min           | Max | Min       | Max |            |
| S <sub>DATA</sub> Max Load Capacitance | CLOAD_SD | –             | 30  | –         | 30  | pF         |
| S <sub>DATA</sub> Pull-up Resistor     | RSD      | 1.5           | 4.7 | 1.5       | 4.7 | k $\Omega$ |

1. This table is based on I<sup>2</sup>C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I<sup>2</sup>C-compatible.
3. All values referred to  $V_{IHmin} = 0.9 V_{DD\_IO}$  and  $V_{ILmax} = 0.1 V_{DD\_IO}$  levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the S<sub>DATA</sub> signal to bridge the undefined region of the falling edge of S<sub>CLK</sub>.
5. The maximum  $t_{HD,DAT}$  has only to be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the S<sub>CLK</sub> signal.
6. A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU,DAT} 250 \text{ ns}$  must then be met. This will automatically be the case if the device does not stretch the LOW period of the S<sub>CLK</sub> signal. If such a device does stretch the LOW period of the S<sub>CLK</sub> signal, it must output the next data bit to the S<sub>DATA</sub> line  $t_r \text{ max} + t_{SU,DAT} = 1000 + 250 = 1250 \text{ ns}$  (according to the Standard-mode I<sup>2</sup>C-bus specification) before the S<sub>CLK</sub> line is released.
7. C<sub>b</sub> = total capacitance of one bus line in pF.

## I/O Timing

By default, the AR0134CS launches pixel data, FV and LV with the falling edge of PIXCLK. The expectation is that the user captures D<sub>OUT</sub>[11:0], FV and LV using the rising

edge of PIXCLK. The launch edge of PIXCLK can be configured in register R0x3028. See Figure 15 and Table 6 for I/O timing (AC) characteristics.



**Figure 15. I/O Timing Diagram**

**Table 6. I/O TIMING CHARACTERISTICS, PARALLEL OUTPUT (1.8 V  $V_{DD\_IO}$ )** (Note 8)

| Symbol       | Definition                         | Condition  | Min  | Typ | Max   | Unit |
|--------------|------------------------------------|--|------|-----|-------|------|
| $f_{EXTCLK}$ | Input Clock Frequency              |  | 6    | –   | 50    | MHz  |
| $t_{EXTCLK}$ | Input Clock Period                 |  | 20   | –   | 166   | ns   |
| $t_R$        | Input Clock Rise Time              | PLL Enabled  | –    | 3   | –     | ns   |
| $t_F$        | Input Clock Fall Time              | PLL Enabled  | –    | 3   | –     | ns   |
| $t_{JITTER}$ | Input Clock Jitter                 |  | –    | –   | 600   | ns   |
| $t_{cp}$     | EXTCLK to PIXCLK Propagation Delay | Nominal Voltages, PLL Disabled, PIXCLK Slew Rate = 4 | 5.7  | –   | 14.3  | ns   |
| $t_{RP}$     | PIXCLK Rise Time                   | PCLK Slew Rate = 6                                   | 1.3  | –   | 4.0   | ns   |
| $t_{FP}$     | PIXCLK Fall Time                   | PCLK Slew Rate = 6                                   | 1.3  | –   | 3.9   | ns   |
|              | PIXCLK Duty Cycle                  |  | 40   | 50  | 60    | %    |
| $f_{PIXCLK}$ | PIXCLK Frequency                   | PIXCLK Slew Rate = 6, Data Slew Rate = 7             | 6    | –   | 74.25 | MHz  |
| $t_{PD}$     | PIXCLK to Data Valid               | PIXCLK Slew Rate = 6, Data Slew Rate = 7             | –2.5 | –   | 2     | ns   |

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**Table 6. I/O TIMING CHARACTERISTICS, PARALLEL OUTPUT (1.8 V V<sub>DD\_IO</sub>)** (Note 8) (continued)

| Symbol           | Definition            | Condition                                | Min  | Typ | Max | Unit |
|------------------|-----------------------|--|------|-----|-----|------|
| t <sub>PFH</sub> | PIXCLK to FV HIGH     | PIXCLK Slew Rate = 6, Data Slew Rate = 7 | –2.5 | –   | 2   | ns   |
| t <sub>PLH</sub> | PIXCLK to LV HIGH     | PIXCLK Slew Rate = 6, Data Slew Rate = 7 | –3   | –   | 1.5 | ns   |
| t <sub>PFL</sub> | PIXCLK to FV LOW      | PIXCLK Slew Rate = 6, Data Slew Rate = 7 | –2.5 | –   | 2   | ns   |
| t <sub>PLL</sub> | PIXCLK to LV LOW      | PIXCLK Slew Rate = 6, Data Slew Rate = 7 | –3   | –   | 1.5 | ns   |
| C <sub>IN</sub>  | Input Pin Capacitance |  | –    | 2.5 | –   | pF   |

8. Minimum and maximum values are taken at 70°C, 1.7 V and –30°C, 1.95 V. All values are taken at the 50% transition point. The loading used is 10 pF.

9. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

**Table 7. I/O TIMING CHARACTERISTICS, PARALLEL OUTPUT (2.8 V V<sub>DD\_IO</sub>)** (Note 10)

| Symbol              | Definition                         | Condition  | Min  | Typ | Max   | Unit |
|---------------------|------------------------------------|--|------|-----|-------|------|
| f <sub>EXTCLK</sub> | Input Clock Frequency              |  | 6    | –   | 50    | MHz  |
| t <sub>EXTCLK</sub> | Input Clock Period                 |  | 20   | –   | 166   | ns   |
| t <sub>R</sub>      | Input Clock Rise Time              | PLL Enabled  | –    | 3   | –     | ns   |
| t <sub>F</sub>      | Input Clock Fall Time              | PLL Enabled  | –    | 3   | –     | ns   |
| t <sub>JITTER</sub> | Input Clock Jitter                 |  | –    | –   | 600   | ns   |
| t <sub>cp</sub>     | EXTCLK to PIXCLK Propagation Delay | Nominal Voltages, PLL Disabled, PIXCLK Slew Rate = 4 | 5.3  | –   | 13.4  | ns   |
| t <sub>RP</sub>     | PIXCLK Rise Time                   | PCLK Slew Rate = 6                                   | 1.3  | –   | 4.0   | ns   |
| t <sub>FP</sub>     | PIXCLK Fall Time                   | PCLK slew rate = 6                                   | 1.3  | –   | 3.9   | ns   |
|                     | PIXCLK Duty Cycle                  |  | 40   | 50  | 60    | %    |
| f <sub>PIXCLK</sub> | PIXCLK Frequency                   | PIXCLK Slew Rate = 6, Data Slew Rate = 7             | 6    | –   | 74.25 | MHz  |
| t <sub>PD</sub>     | PIXCLK to Data Valid               | PIXCLK Slew Rate = 6, Data Slew Rate = 7             | –2.5 | –   | 2     | ns   |
| t <sub>PFH</sub>    | PIXCLK to FV HIGH                  | PIXCLK Slew Rate = 6, Data Slew Rate = 7             | –2.5 | –   | 2     | ns   |
| t <sub>PLH</sub>    | PIXCLK to LV HIGH                  | PIXCLK Slew Rate = 6, Data Slew Rate = 7             | –2.5 | –   | 2     | ns   |
| t <sub>PFL</sub>    | PIXCLK to FV LOW                   | PIXCLK Slew Rate = 6, Data Slew Rate = 7             | –2.5 | –   | 2     | ns   |
| t <sub>PLL</sub>    | PIXCLK to LV LOW                   | PIXCLK Slew Rate = 6, Data Slew Rate = 7             | –2.5 | –   | 2     | ns   |
| C <sub>IN</sub>     | Input Pin Capacitance              |  | –    | 2.5 | –     | pF   |

10. Minimum and maximum values are taken at 70°C, 2.5 V and –30°C, 3.1 V. All values are taken at the 50% transition point. The loading used is 10 pF.

11. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

**Table 8. I/O RISE SLEW RATE (2.8 V V<sub>DD\_IO</sub>)** (Note 12)

| Parallel Slew (R0x306E[15:13]) | Condition | Min  | Typ  | Max  | Unit |
|--------------------------------|-----------|------|------|------|------|
| 7                              | Default   | 1.50 | 2.50 | 3.90 | V/ns |
| 6                              | Default   | 0.98 | 1.62 | 2.52 | V/ns |
| 5                              | Default   | 0.71 | 1.12 | 1.79 | V/ns |
| 4                              | Default   | 0.52 | 0.82 | 1.26 | V/ns |
| 3                              | Default   | 0.37 | 0.58 | 0.88 | V/ns |
| 2                              | Default   | 0.26 | 0.40 | 0.61 | V/ns |
| 1                              | Default   | 0.17 | 0.27 | 0.40 | V/ns |
| 0                              | Default   | 0.10 | 0.16 | 0.23 | V/ns |

12. Minimum and maximum values are taken at 70°C, 2.5 V and –30°C, 3.1 V. The loading used is 10 pF.



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**Table 9. I/O FALL SLEW RATE (2.8 V  $V_{DD\_IO}$ ) (Note 13)**

| Parallel Slew (R0x306E[15:13]) | Condition | Min  | Typ  | Max  | Unit |
|--------------------------------|-----------|------|------|------|------|
| 7                              | Default   | 1.40 | 2.30 | 3.50 | V/ns |
| 6                              | Default   | 0.97 | 1.61 | 2.48 | V/ns |
| 5                              | Default   | 0.73 | 1.21 | 1.86 | V/ns |
| 4                              | Default   | 0.54 | 0.88 | 1.36 | V/ns |
| 3                              | Default   | 0.39 | 0.63 | 0.88 | V/ns |
| 2                              | Default   | 0.27 | 0.43 | 0.66 | V/ns |
| 1                              | Default   | 0.18 | 0.29 | 0.44 | V/ns |
| 0                              | Default   | 0.11 | 0.17 | 0.25 | V/ns |

13. Minimum and maximum values are taken at 70°C, 2.5 V and –30°C, 3.1 V. The loading used is 10 pF.

**Table 10. I/O RISE SLEW RATE (1.8 V  $V_{DD\_IO}$ ) (Note 14)**

| Parallel Slew (R0x306E[15:13]) | Condition | Min  | Typ  | Max  | Unit |
|--------------------------------|-----------|------|------|------|------|
| 7                              | Default   | 0.57 | 0.91 | 1.55 | V/ns |
| 6                              | Default   | 0.39 | 0.61 | 1.02 | V/ns |
| 5                              | Default   | 0.29 | 0.46 | 0.75 | V/ns |
| 4                              | Default   | 0.22 | 0.34 | 0.54 | V/ns |
| 3                              | Default   | 0.16 | 0.24 | 0.39 | V/ns |
| 2                              | Default   | 0.12 | 0.17 | 0.27 | V/ns |
| 1                              | Default   | 0.08 | 0.11 | 0.18 | V/ns |
| 0                              | Default   | 0.05 | 0.07 | 0.10 | V/ns |

14. Minimum and maximum values are taken at 70°C, 1.7 V and –30°C, 1.95 V. The loading used is 10 pF.

**Table 11. I/O FALL SLEW RATE (1.8 V  $V_{DD\_IO}$ ) (Note 15)**

| Parallel Slew (R0x306E[15:13]) | Condition | Min  | Typ  | Max  | Unit |
|--------------------------------|-----------|------|------|------|------|
| 7                              | Default   | 0.57 | 0.92 | 1.55 | V/ns |
| 6                              | Default   | 0.40 | 0.64 | 1.08 | V/ns |
| 5                              | Default   | 0.31 | 0.50 | 0.82 | V/ns |
| 4                              | Default   | 0.24 | 0.38 | 0.61 | V/ns |
| 3                              | Default   | 0.18 | 0.27 | 0.44 | V/ns |
| 2                              | Default   | 0.13 | 0.19 | 0.31 | V/ns |
| 1                              | Default   | 0.09 | 0.13 | 0.20 | V/ns |
| 0                              | Default   | 0.05 | 0.08 | 0.12 | V/ns |

15. Minimum and maximum values are taken at 70°C, 1.7 V and –30°C, 1.95 V. The loading used is 10 pF.

**DC Electrical Characteristics**

The DC electrical characteristics are shown in Table 12, Table 13, Table 14, and Table 15.

**Table 12. DC ELECTRICAL CHARACTERISTICS**

| Symbol               | Definition            | Condition  | Min                      | Typ     | Max                      | Unit |
|----------------------|-----------------------|--|--------------------------|---------|--------------------------|------|
| V <sub>DD</sub>      | Core Digital Voltage  |  | 1.7                      | 1.8     | 1.95                     | V    |
| V <sub>DD_IO</sub>   | I/O Digital Voltage   |  | 1.7/2.5                  | 1.8/2.8 | 1.9/3.1                  | V    |
| V <sub>AA</sub>      | Analog Voltage        |  | 2.5                      | 2.8     | 3.1                      | V    |
| V <sub>AA_PIX</sub>  | Pixel Supply Voltage  |  | 2.5                      | 2.8     | 3.1                      | V    |
| V <sub>DD_PLL</sub>  | PLL Supply Voltage    |  | 2.5                      | 2.8     | 3.1                      | V    |
| V <sub>DD_SLVS</sub> | HiSPi Supply Voltage  |  | 0.3                      | 0.4     | 0.6                      | V    |
| V <sub>IH</sub>      | Input HIGH Voltage    |  | V <sub>DD_IO</sub> × 0.7 | –       | –                        | V    |
| V <sub>IL</sub>      | Input LOW Voltage     |  | –                        | –       | V <sub>DD_IO</sub> × 0.3 | V    |
| I <sub>IN</sub>      | Input Leakage Current | No Pull-up Resistor;<br>V <sub>IN</sub> = V <sub>DD_IO</sub> or D <sub>GND</sub> | 20                       | –       | –                        | μA   |
| V <sub>OH</sub>      | Output HIGH Voltage   |  | V <sub>DD_IO</sub> – 0.3 | –       | –                        | V    |
| V <sub>OL</sub>      | Output LOW Voltage    | V <sub>DD_IO</sub> = 2.8 V   | –                        | –       | 0.4                      | V    |
| I <sub>OH</sub>      | Output HIGH Current   | At Specified V <sub>OH</sub>   | –22                      | –       | –                        | mA   |
| I <sub>OL</sub>      | Output LOW Current    | At Specified V <sub>OL</sub>   | –                        | –       | 22                       | mA   |

**CAUTION:** Stresses greater than those listed in Table 13 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**Table 13. ABSOLUTE MAXIMUM RATINGS**

| Symbol              | Parameter                           | Minimum | Maximum                  | Unit |
|---------------------|-------------------------------------|---------|--------------------------|------|
| V <sub>SUPPLY</sub> | Power Supply Voltage (All Supplies) | –0.3    | 4.5                      | V    |
| I <sub>SUPPLY</sub> | Total Power Supply Current          | –       | 200                      | mA   |
| I <sub>GND</sub>    | Total Ground Current                | –       | 200                      | mA   |
| V <sub>IN</sub>     | DC Input Voltage                    | –0.3    | V <sub>DD_IO</sub> + 0.3 | V    |
| V <sub>OUT</sub>    | DC Output Voltage                   | –0.3    | V <sub>DD_IO</sub> + 0.3 | V    |
| T <sub>STG</sub>    | Storage Temperature (Note 16)       | –40     | +85                      | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

16. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 14. OPERATING CURRENT CONSUMPTION FOR PARALLEL OUTPUT**

(V<sub>AA</sub> = V<sub>AA\_PIX</sub> = V<sub>DD\_IO</sub> = V<sub>DD\_PLL</sub> = 2.8 V; V<sub>DD</sub> = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; T<sub>A</sub> = 25°C; C<sub>LOAD</sub> = 10 pF)

| Symbol              | Parameter                     | Condition                                   | Min | Typ | Max | Unit |
|---------------------|-------------------------------|---|-----|-----|-----|------|
| I <sub>DD1</sub>    | Digital Operating Current     | Parallel, Streaming, Full Resolution 54 fps | –   | 46  | 60  | mA   |
| I <sub>DD_IO</sub>  | I/O Digital Operating Current | Parallel, Streaming, Full Resolution 54 fps | –   | 52  | –   | mA   |
| I <sub>AA</sub>     | Analog Operating Current      | Parallel, Streaming, Full Resolution 54 fps | –   | 46  | 55  | mA   |
| I <sub>AA_PIX</sub> | Pixel Supply Current          | Parallel, Streaming, Full Resolution 54 fps | –   | 7   | 9   | mA   |
| I <sub>DD_PLL</sub> | PLL Supply Current            | Parallel, Streaming, Full Resolution 54 fps | –   | 8   | 10  | mA   |

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**Table 15. STANDBY CURRENT CONSUMPTION**

(Analog –  $V_{AA} + V_{AA\_PIX} + V_{DD\_PLL}$ ; Digital –  $V_{DD} + V_{DD\_IO}$ ;  $T_A = 25^\circ\text{C}$ )

| Definition                               | Condition      | Min | Typ | Max | Unit          |
|--|----------------|-----|-----|-----|---------------|
| Hard Standby (Clock Off, Driven Low)     | Analog, 2.8 V  | –   | 3   | 15  | $\mu\text{A}$ |
|  | Digital, 1.8 V | –   | 25  | 80  | $\mu\text{A}$ |
| Hard Standby (Clock On, EXTCLK = 20 MHz) | Analog, 2.8 V  | –   | 12  | 25  | $\mu\text{A}$ |
|  | Digital, 1.8 V | –   | 1.1 | 1.7 | mA            |
| Soft Standby (Clock Off, Driven Low)     | Analog, 2.8 V  | –   | 3   | 15  | $\mu\text{A}$ |
|  | Digital, 1.8 V | –   | 25  | 80  | $\mu\text{A}$ |
| Soft Standby (Clock On, EXTCLK = 20 MHz) | Analog, 2.8 V  | –   | 12  | 25  | $\mu\text{A}$ |
|  | Digital, 1.8 V | –   | 1.1 | 1.7 | mA            |

## HiSPi Electrical Specifications

The ON Semiconductor AR0134CS sensor supports SLVS mode only, and does not have a DLL for timing adjustments. Refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing

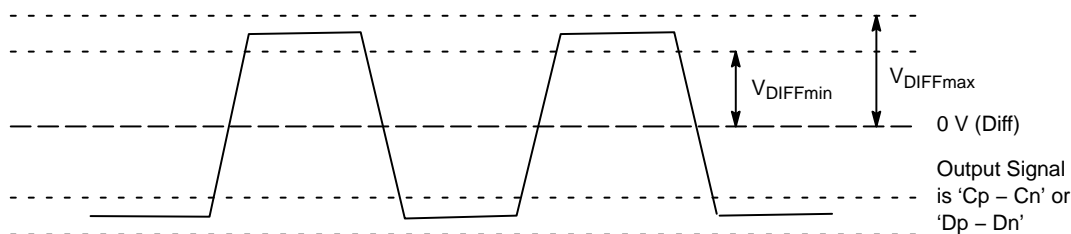
information. The  $V_{DD\_SLVS}$  supply in this data sheet corresponds to  $V_{DD\_TX}$  in the HiSPi Physical Layer Specification. Similarly,  $V_{DD}$  is equivalent to  $V_{DD\_HiSPi}$  as referenced in the specification. The HiSPi transmitter electrical specifications are listed at 700 MHz.

**Table 16. INPUT VOLTAGE AND CURRENT (HiSPi POWER SUPPLY 0.4 V)**

(Measurement Conditions: Max Freq. 700 MHz)

| Symbol              | Parameter   | Min                        | Typ              | Max                        | Unit     |
|---------------------|---|----------------------------|------------------|----------------------------|----------|
| $I_{DD\_SLVS}$      | Supply Current ( $PWR_{HiSPi}$ ) (Driving 100 $\Omega$ Load)  | –                          | 10               | 15                         | mA       |
| $V_{CMD}$           | HiSPi Common Mode Voltage (Driving 100 $\Omega$ Load)         | $V_{DD\_SLVS} \times 0.45$ | $V_{DD\_SLVS}/2$ | $V_{DD\_SLVS} \times 0.55$ | V        |
| $ V_{OD} $          | HiSPi Differential Output Voltage (Driving 100 $\Omega$ Load) | $V_{DD\_SLVS} \times 0.36$ | $V_{DD\_SLVS}/2$ | $V_{DD\_SLVS} \times 0.64$ | V        |
| $\Delta V_{CM}$     | Change in $V_{CM}$ between Logic 1 and 0                      | –                          | –                | 25                         | mV       |
| $ V_{OD} $          | Change in $ V_{OD} $ between Logic 1 and 0                    | –                          | –                | 25                         | mV       |
| NM                  | $V_{OD}$ Noise Margin   | –                          | –                | 30                         | %        |
| $ \Delta V_{CM} $   | Difference in $V_{CM}$ between any Two Channels               | –                          | –                | 50                         | mV       |
| $ \Delta V_{OD} $   | Difference in $V_{OD}$ between any Two Channels               | –                          | –                | 100                        | mV       |
| $\Delta V_{CM\_ac}$ | Common-mode AC Voltage (pk) without $V_{CM}$ Cap Termination  | –                          | –                | 50                         | mV       |
| $\Delta V_{CM\_ac}$ | Common-mode AC Voltage (pk) with $V_{CM}$ Cap Termination     | –                          | –                | 30                         | mV       |
| $V_{OD\_ac}$        | Max Overshoot Peak $ V_{OD} $                                 | –                          | –                | $1.3 \times  V_{OD} $      | V        |
| $V_{diff\_pkpk}$    | Max Overshoot $V_{diff}$ pk-pk                                | –                          | –                | $2.6 \times  V_{OD} $      | V        |
| $V_{eye}$           | Eye Height  | $1.4 \times V_{OD}$        | –                | –                          |          |
| $R_o$               | Single-ended Output Impedance                                 | 35                         | 50               | 70                         | $\Omega$ |
| $\Delta R_o$        | Output Impedance Mismatch                                     | –                          | –                | 20                         | %        |

## AR0134CS



**Figure 16. Differential Output Voltage for Clock and Data Pairs**

**Table 17. RISE AND FALL TIMES**

(Measurement Conditions: HiSPi Power Supply 0.4 V, Max Freq. 700 MHz)

| Symbol                 | Parameter                                     | Min    | Typ     | Max  | Unit |
|------------------------|---|--------|---------|------|------|
| 1/UI                   | Data Rate                                     | 280    | –       | 700  | Mb/s |
| TxPRE                  | Max Setup Time from Transmitter (Note 17)     | 0.3    | –       | –    | UI   |
| TxPost                 | Max Hold Time from Transmitter                | 0.3    | –       | –    | UI   |
| RISE                   | Rise Time (20% – 80%)                         | –      | 0.25 UI | –    |      |
| FALL                   | Fall Time (20% – 80%)                         | 150 ps | 0.25 UI | –    |      |
| PLL_DUTY               | Clock Duty                                    | 45     | 50      | 55   | %    |
| t <sub>pw</sub>        | Bitrate Period (Note 17)                      | 1.43   | –       | 3.57 | ns   |
| t <sub>eye</sub>       | Eye Width (Notes 17, 18)                      | 0.3    | –       | –    | UI   |
| t <sub>totaljit</sub>  | Data Total Jitter (pk pk)@1e–9 (Notes 17, 18) | –      | –       | 0.2  | UI   |
| t <sub>ckjit</sub>     | Clock Period Jitter (RMS) (Note 18)           | –      | –       | 50   | ps   |
| t <sub>cyjit</sub>     | Clock Cycle to Cycle Jitter (RMS) (Note 18)   | –      | –       | 100  | ps   |
| t <sub>chskew</sub>    | Clock to Data Skew (Notes 17, 18)             | –0.1   | –       | 0.1  | UI   |
| t <sub> PHYskew </sub> | PHY-to-PHY Skew (Notes 17, 21)                | –      | –       | 2.1  | UI   |
| t <sub>DIFFSKEW</sub>  | Mean Differential Skew (Note 22)              | –100   | –       | 100  | ps   |

17. One UI is defined as the normalized mean time between one edge and the following edge of the clock.

18. Taken from 0 V crossing point.

19. Also defined with a maximum loading capacitance of 10 pF on any pin. The loading capacitance may also need to be less for higher bitrates so the rise and fall times do not exceed the maximum 0.3 UI.

20. The absolute mean skew between the Clock lane and any Data Lane in the same PHY between any edges.

21. The absolute mean skew between any Clock in one PHY and any Data lane in any other PHY between any edges.

22. Differential skew is defined as the skew between complementary outputs. It is measured as the absolute time between the two complementary edges at mean  $V_{CM}$  point.

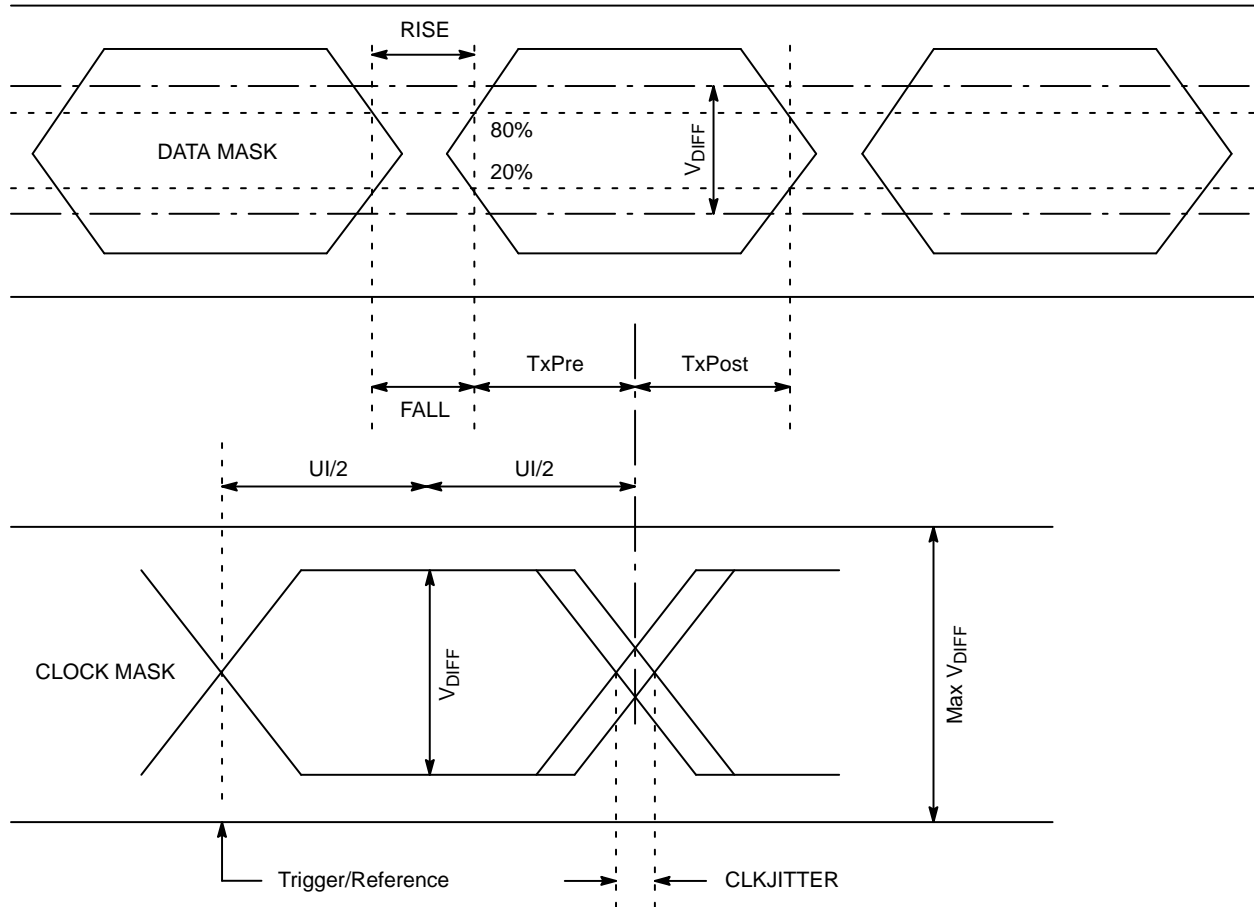


Figure 17. Eye Diagram for Clock and Data Signals

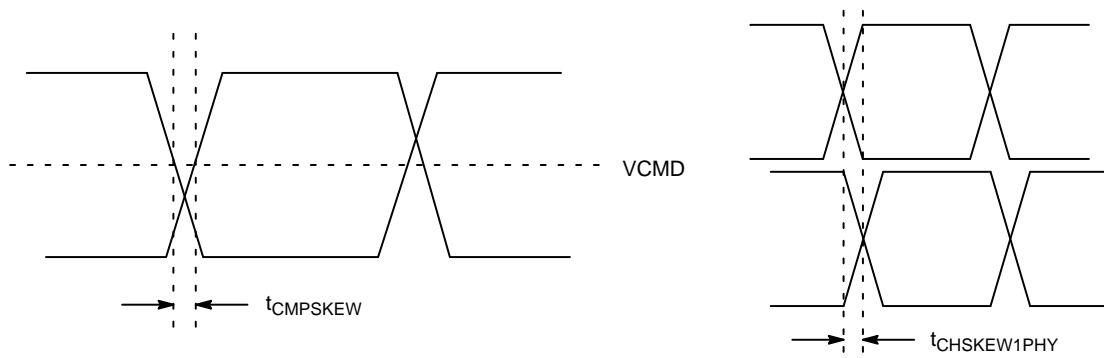


Figure 18. Skew within the PHY and Output Channels

## POWER-ON RESET AND STANDBY TIMING

### Power-Up Sequence

The recommended power-up sequence for the AR0134CS is shown in Figure 19. The available power supplies ( $V_{DD\_IO}$ ,  $V_{DD}$ ,  $V_{DD\_SLVS}$ ,  $V_{DD\_PLL}$ ,  $V_{AA}$ ,  $V_{AA\_PIX}$ ) must have the separation specified below.

1. Turn on  $V_{DD\_PLL}$  power supply.
2. After 0–10  $\mu$ s, turn on  $V_{AA}$  and  $V_{AA\_PIX}$  power supply.
3. After 0–10  $\mu$ s, turn on  $V_{DD\_IO}$  power supply.
4. After the last power supply is stable, enable EXTCLK.
5. If RESET\_BAR is in a LOW state, hold RESET\_BAR LOW for at least 1 ms. If RESET\_BAR is in a HIGH state, assert RESET\_BAR for at least 1 ms.
6. Wait 160000 EXTCLKs (for internal initialization into software standby).
7. Configure PLL, output, and image settings to desired values.
8. Wait 1 ms for the PLL to lock.
9. Set streaming mode ( $R0x301a[2] = 1$ ).

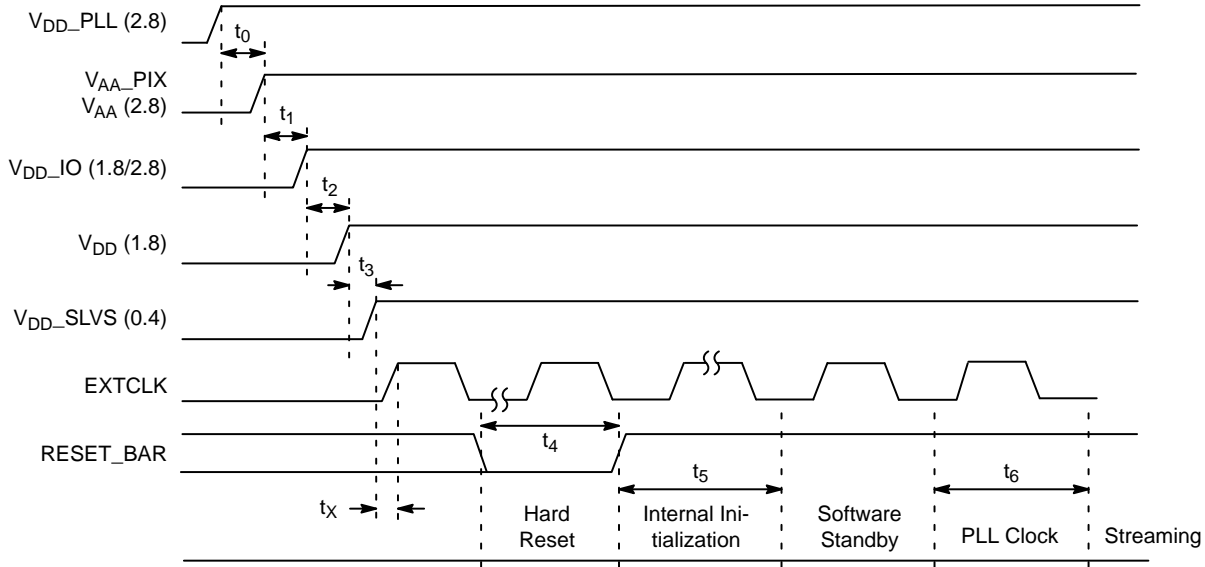


Figure 19. Power Up

Table 18. POWER-UP SEQUENCE

| Symbol | Definition                            | Min         | Typ          | Max | Unit    |
|--------|---------------------------------------|-------------|--------------|-----|---------|
| $t_0$  | $V_{DD\_PLL}$ to $V_{AA}/V_{AA\_PIX}$ | 0           | 10           | –   | $\mu$ s |
| $t_1$  | $V_{AA}/V_{AA\_PIX}$ to $V_{DD\_IO}$  | 0           | 10           | –   | $\mu$ s |
| $t_2$  | $V_{DD\_IO}$ to $V_{DD}$              | 0           | 10           | –   | $\mu$ s |
| $t_3$  | $V_{DD}$ to $V_{DD\_SLVS}$            | 0           | 10           | –   | $\mu$ s |
| $t_X$  | Xtal Settle Time                      | –           | 30 (Note 23) | –   | ms      |
| $t_4$  | Hard Reset                            | 1 (Note 24) | –            | –   | ms      |
| $t_5$  | Internal Initialization               | 160000      | –            | –   | EXTCLKs |
| $t_6$  | PLL Lock Time                         | 1           | –            | –   | ms      |

23. Xtal settling time is component-dependent, usually taking about 10–100 ms.

24. Hard reset time is the minimum time required after power rails are settled. In a circuit where hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.

25. It is critical that  $V_{DD\_PLL}$  is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that  $V_{DD\_PLL}$  is powered after other supplies then the sensor may have functionality issues and will experience high current draw on this supply.

### Power-Down Sequence

The recommended power-down sequence for the AR0134CS is shown in Figure 20. The available power supplies ( $V_{DD\_IO}$ ,  $V_{DD}$ ,  $V_{DD\_SLVS}$ ,  $V_{DD\_PLL}$ ,  $V_{AA}$ ,  $V_{AA\_PIX}$ ) must have the separation specified below.

1. Disable streaming if output is active by setting standby  $R0x301a[2] = 0$ .
2. The standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off  $V_{DD\_SLVS}$ .
4. Turn off  $V_{DD}$ .
5. Turn off  $V_{DD\_IO}$ .
6. Turn off  $V_{AA}/V_{AA\_PIX}$ .
7. Turn off  $V_{DD\_PLL}$ .

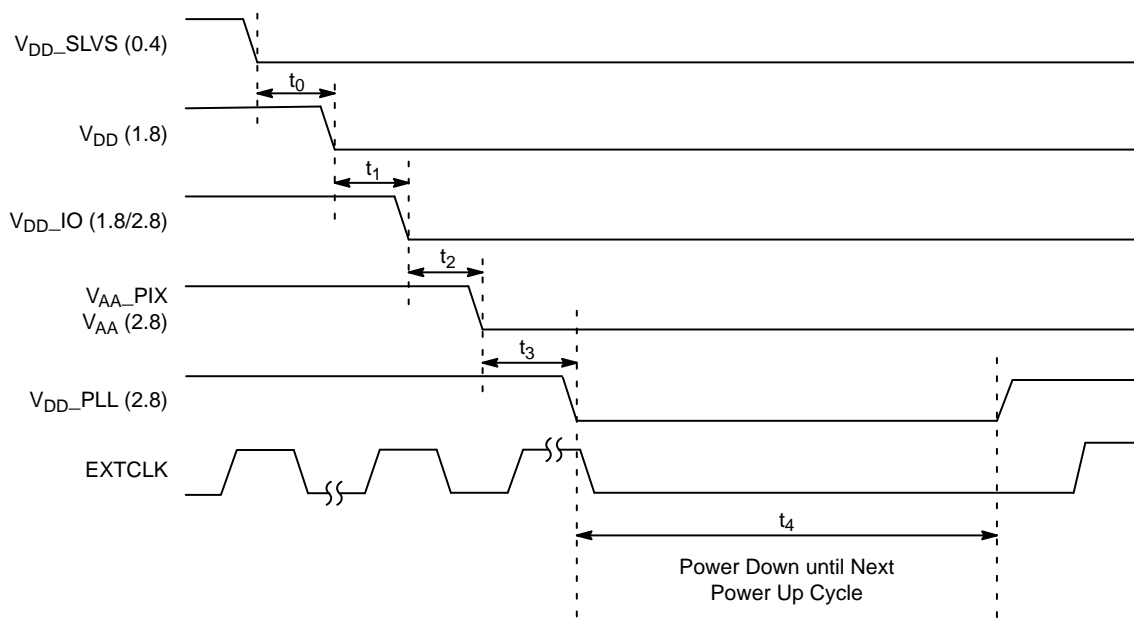


Figure 20. Power Down

Table 19. POWER-DOWN SEQUENCE

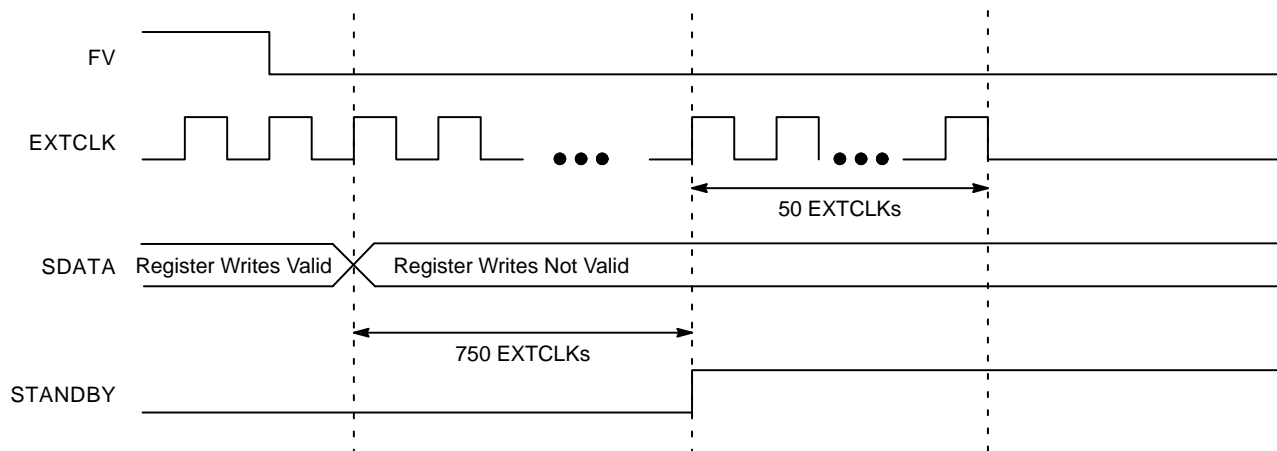
| Symbol | Parameter                             | Min | Typ | Max | Unit    |
|--------|---------------------------------------|-----|-----|-----|---------|
| $t_0$  | $V_{DD\_SLVS}$ to $V_{DD}$            | 0   | —   | —   | $\mu s$ |
| $t_1$  | $V_{DD}$ to $V_{DD\_IO}$              | 0   | —   | —   | $\mu s$ |
| $t_2$  | $V_{DD\_IO}$ to $V_{AA}/V_{AA\_PIX}$  | 0   | —   | —   | $\mu s$ |
| $t_3$  | $V_{AA}/V_{AA\_PIX}$ to $V_{DD\_PLL}$ | 0   | —   | —   | $\mu s$ |
| $t_4$  | PwrDn until Next PwrUp Time           | 100 | —   | —   | ms      |

26.  $t_4$  is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

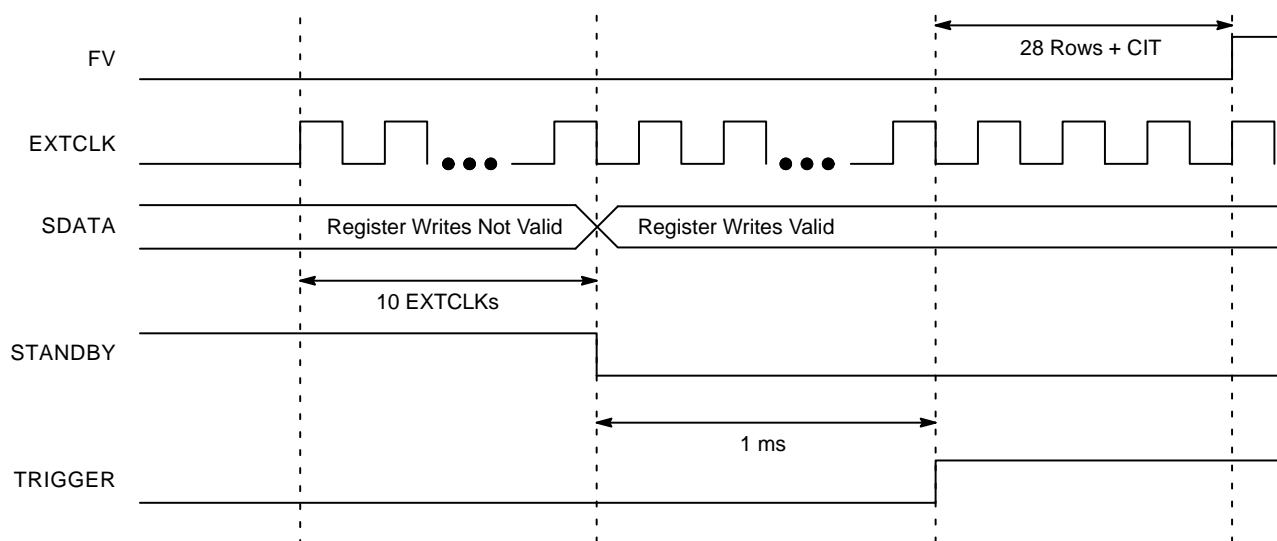
**Standby Sequence**

Figure 21 and Figure 22 show timing diagrams for entering and exiting standby. Delays are shown indicating

the last valid register write prior to entering standby as well as the first valid write upon exiting standby. Also shown is timing if the EXTCLK is to be disabled during standby.



**Figure 21. Enter Standby Timing**



**Figure 22. Exit Standby Timing**



## AR0134CS

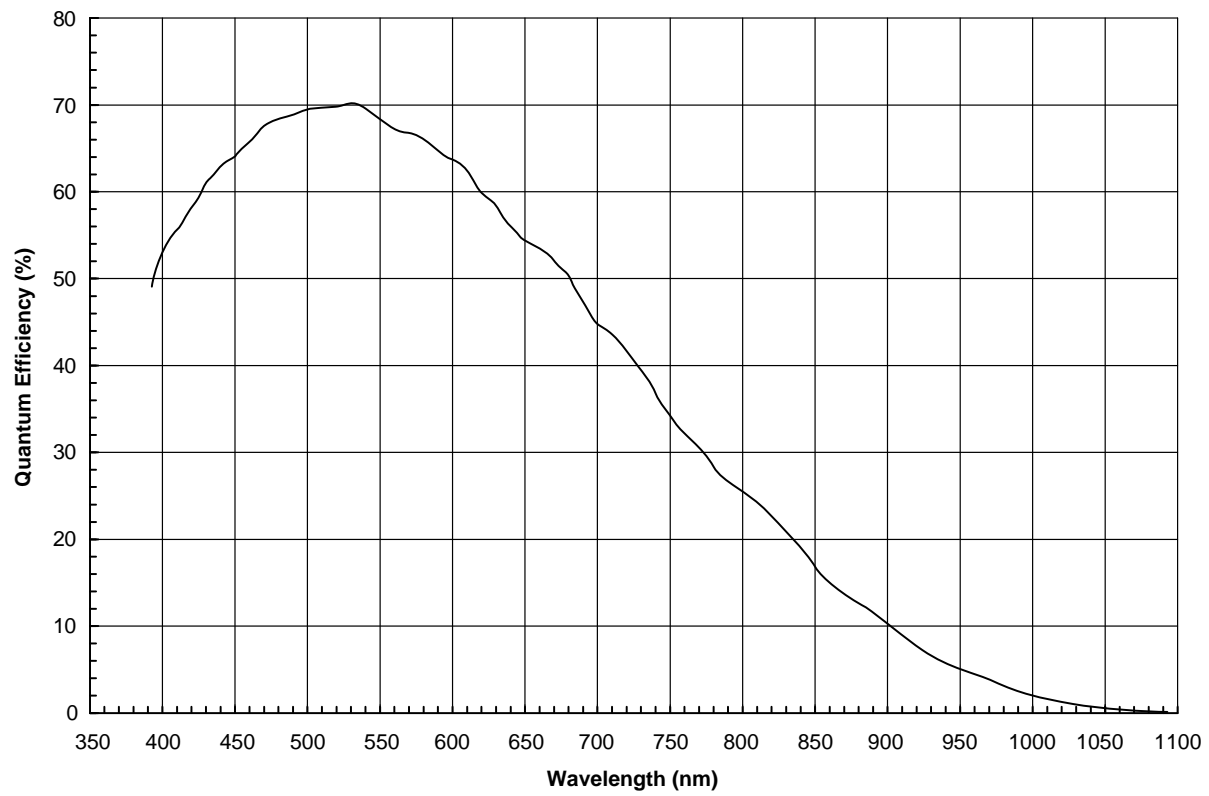


Figure 23. Quantum Efficiency – Monochrome Sensor (Typical)

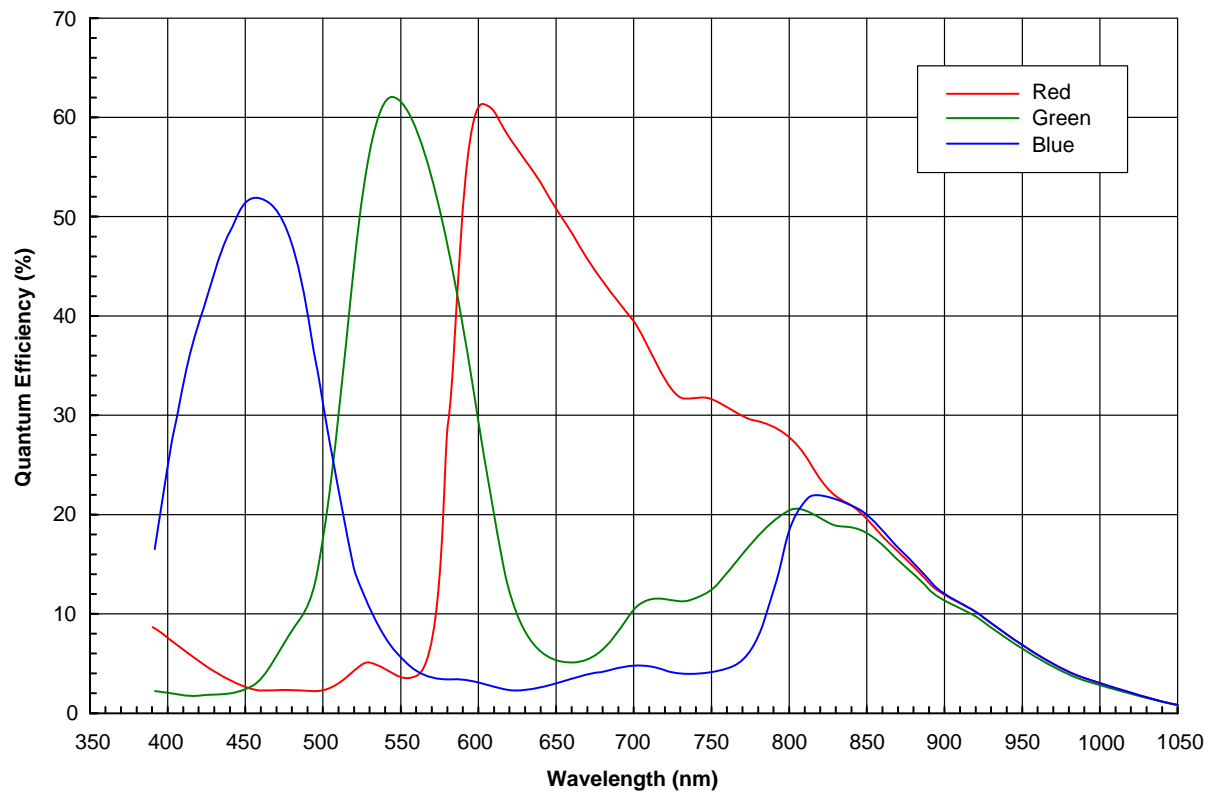


Figure 24. Quantum Efficiency – Color Sensor (Typical)

# AR0134CS

CRA vs. Image Height Plot

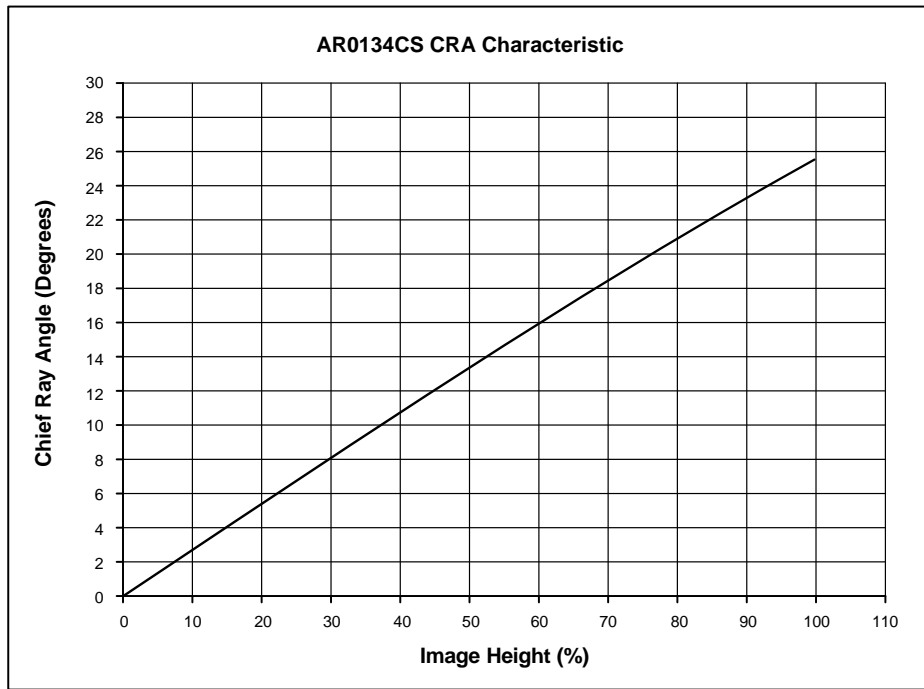


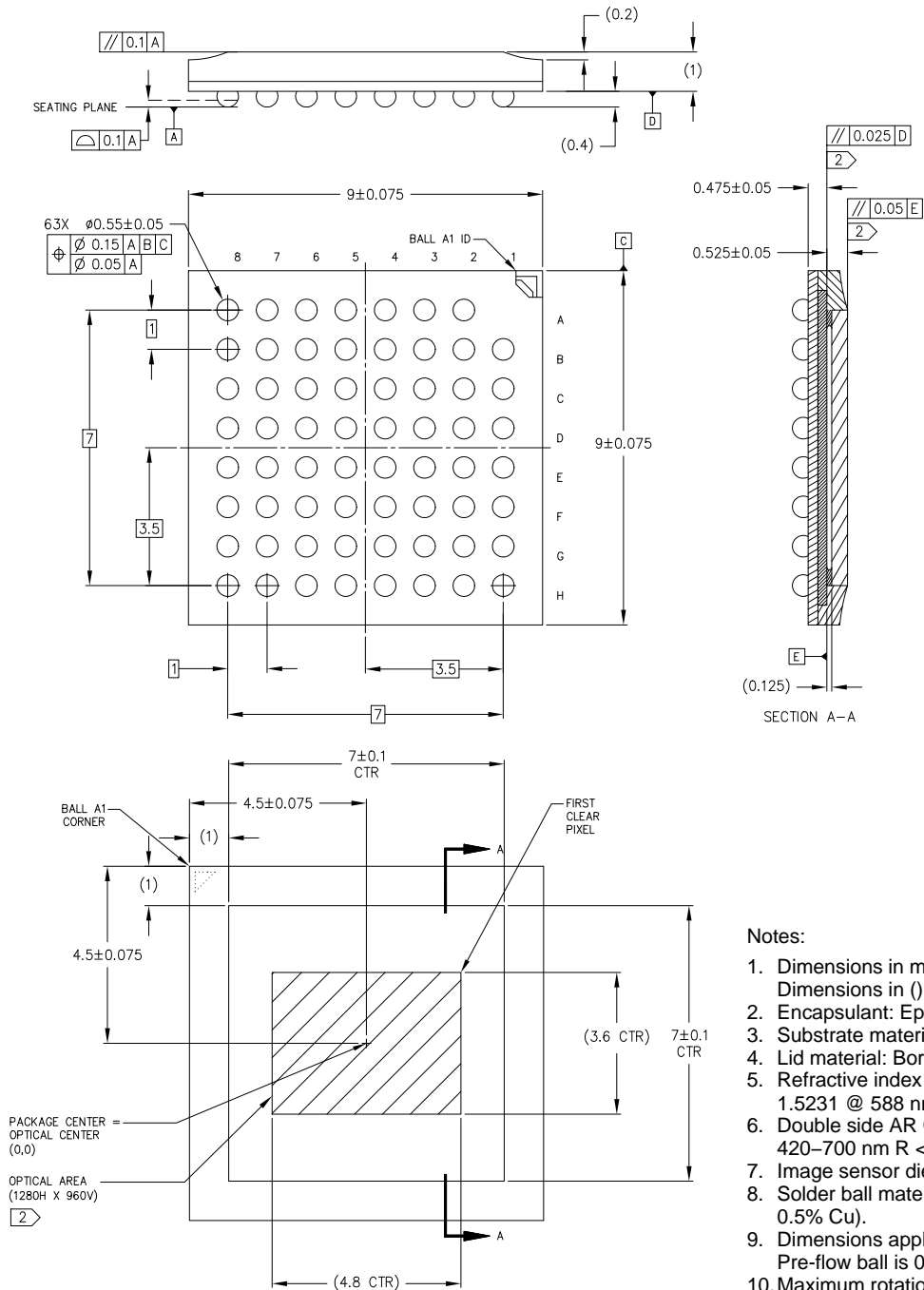
Figure 25. Chief Ray Angle – 25° Mono

| Image Height |       | CRA   |
|--------------|-------|-------|
| (%)          | (mm)  | (deg) |
| 0            | 0     | 0     |
| 5            | 0.150 | 1.35  |
| 10           | 0.300 | 2.70  |
| 15           | 0.450 | 4.04  |
| 20           | 0.600 | 5.39  |
| 25           | 0.750 | 6.73  |
| 30           | 0.900 | 8.06  |
| 35           | 1.050 | 9.39  |
| 40           | 1.200 | 10.71 |
| 45           | 1.350 | 12.02 |
| 50           | 1.500 | 13.33 |
| 55           | 1.650 | 14.62 |
| 60           | 1.800 | 15.90 |
| 65           | 1.950 | 17.16 |
| 70           | 2.100 | 18.41 |
| 75           | 2.250 | 19.64 |
| 80           | 2.400 | 20.85 |
| 85           | 2.550 | 22.05 |
| 90           | 2.700 | 23.22 |
| 95           | 2.850 | 24.38 |
| 100          | 3.000 | 25.51 |

# AR0134CS

## PACKAGE DIMENSIONS

IBGA63 9x9  
CASE 503AG  
ISSUE O

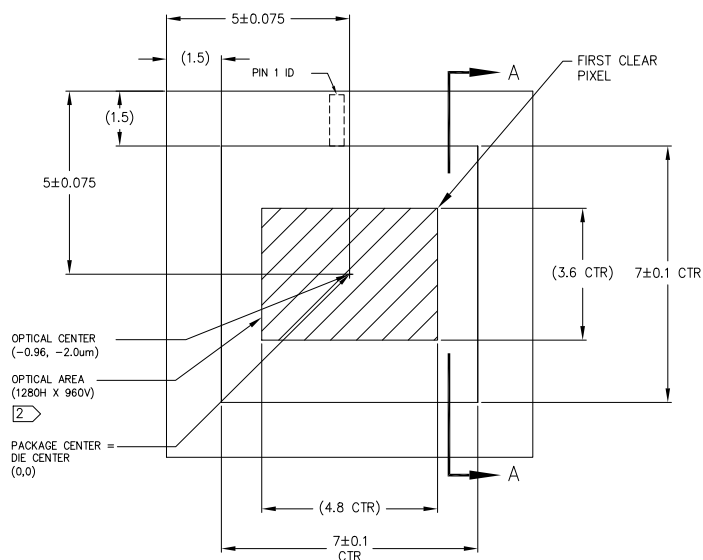
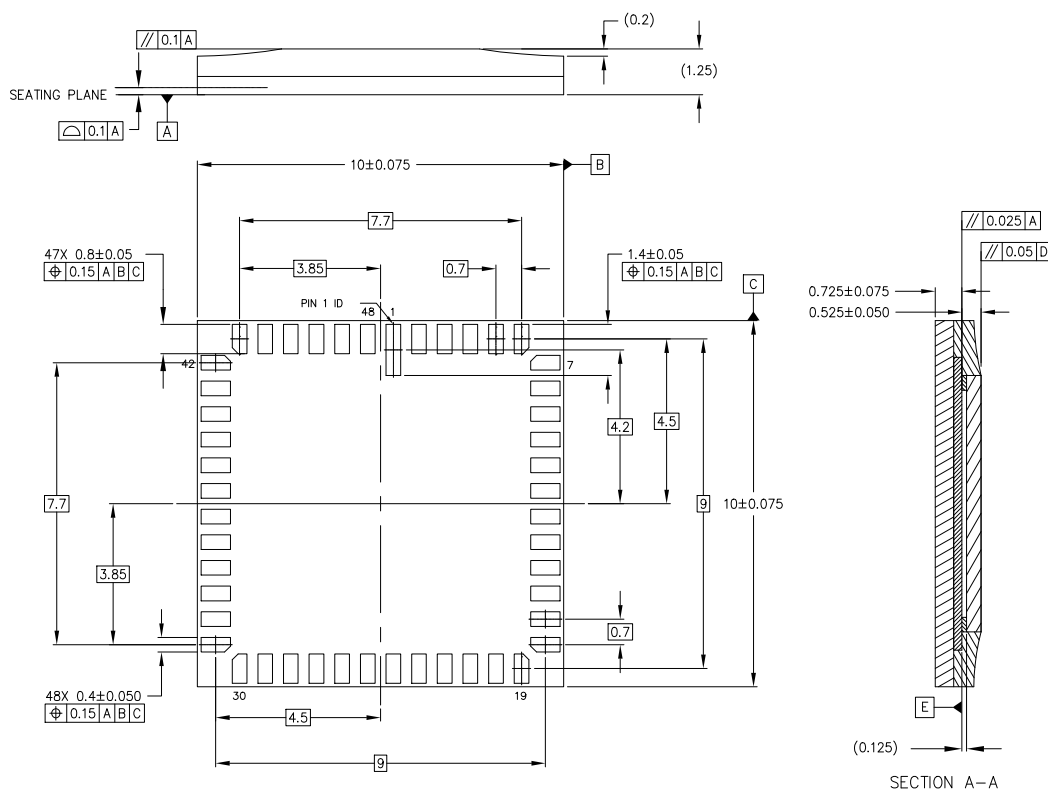


| NOTES |   |
|-------|---|
| 1     | DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.   |
| 2     | MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°.<br>MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SUBSTRATE PLANE [D]: 25 MICRONS.<br>MAXIMUM TILT OF COVER GLASS RELATIVE TO OPTICAL AREA PLANE [E]: 50 MICRONS. |

### Notes:

1. Dimensions in mm.  
Dimensions in ( ) are for reference only.
2. Encapsulant: Epoxy.
3. Substrate material: Plastic laminate 0.25 thickness.
4. Lid material: Borosilicate glass  $0.4 \pm 0.04$  thickness.
5. Refractive index at 20C = 1.5255 @ 546 nm and 1.5231 @ 588 nm.
6. Double side AR Coating: 530–570 nm R < 1%; 420–700 nm R < 2%.
7. Image sensor die: 0.2 mm thickness.
8. Solder ball material: SAC305 (95% Sn, 3% Ag, 0.5% Cu).
9. Dimensions apply to solder balls post reflow.  
Pre-flow ball is 0.5 on a  $\phi 0.4$  SMD ball pad.
10. Maximum rotation of optical area relative to package edges: 1°.
11. Maximum tilt of optical area relative to substrate plane D: 25  $\mu$ m.
12. Maximum tilt of cover glass relative to optical area plane E: 50  $\mu$ m.


ILCC48 10x10  
CASE 847AE  
ISSUE O



| NOTES |  |  |
|-------|--|--|
| 1     | DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.  |  |
| 2     | MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 0.75°<br>MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SUBSTRATE PLANE $\square$ : 25 MICRONS<br>MAXIMUM TILT OF COVER GLASS RELATIVE TO OPTICAL AREA PLANE $\square$ : 50 MICRONS. |  |

Notes:

1. Dimensions in mm.  
Dimensions in ( ) are for reference only.
2. Encapsulant: Epoxy.
3. Substrate material: Plastic laminate 0.25 thickness.
4. Lid material: Borosilicate glass  $0.4 \pm 0.04$  thickness.
5. Refractive index at 20C = 1.5255 @ 546 nm and 1.5231 @ 588 nm.
6. Double side AR Coating: 530–570 nm R < 1%; 420–700 nm R < 2%.
7. Lead finish: Gold plating, 0.5  $\mu\text{m}$  min. thickness.
8. Image sensor die: 0.2 mm thickness.
9. Maximum rotation of optical area relative to package edges: 0.75°.
10. Maximum tilt of optical area relative to substrate plane D: 25  $\mu\text{m}$ .
11. Maximum tilt of cover glass relative to optical area plane E: 50  $\mu\text{m}$ .

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