AR0134 Register Reference, Rev. D

For more information, refer to the data sheet on Aptina's Web site: www.aptina.com

AR0134 Register Reference

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Introduction

This register reference is provided for engineers who are designing cameras that use the AR0134.

Conventions and Notations

This document follows the conventions and notations described below.

- Hexadecimal numbers have a 0x prefix
- Binary numbers have 0b prefix
  Example: 0b1010 = 0xA

Register Address Space

The AR0134 provides a 16-bit register address space accessed through a serial interface. Each register location is 8 or 16 bits in size.

The address space is divided into the five major regions shown in Table 1.

Table 1: Address Space Regions

Address Range	Description
0x0000–0x0FFF	Reserved
0x1000–0x1FFF	Reserved
0x2000–0x2FFF	Reserved
0x3000–0x3FFF	Manufacturer-specific registers (read-only and read-write dynamic registers)
0x4000–0xFFFF	Reserved (undefined)

Register Notation

The underlying mechanism for reading and writing registers provides byte write capability. However, it is convenient to consider some registers as multiple adjacent bytes. The AR0134uses 8-bit, 16-bit, and 32-bit registers, all implemented as 1 or more bytes at naturally aligned, contiguous locations in the address space.

In this document, registers are described either by address or by name. When registers are described by address, the size of the registers is explicit. For example, R0x3024 is an 8-bit register at address 0x3024, and R0x3000–1 is a 16-bit register at address 0x3000–0x3001. When registers are described by name, the size of the register is implicit. It is necessary to refer to the register table to determine that model_id is a 16-bit register.

Register Aliases

A consequence of the internal architecture of the AR0134 is that some registers are decoded at multiple addresses. Some registers in “configuration space” are also decoded in “manufacturer-specific space.” To provide unique names for all registers, the name of the register within manufacturer-specific register space has a trailing underscore. For example, R0x0000–1 is model_id, and R0x3000–1 is model_id_. The effect of reading or writing a register through any of its aliases is identical.

Bit Fields

Some registers provide control of several different pieces of related functionality, and this makes it necessary to refer to bit fields within registers. As an example of the notation used for this, the least significant 4 bits of the model_id register are referred to as model_id[3:0] or R0x0000–1[3:0].

Bit Field Aliases

In addition to the register aliases described above, some register fields are aliased in multiple places. For example, R0x0100 (mode_select) only has one operational bit, R0x0100[0]. This bit is aliased to R0x301A–B[2]. The effect of reading or writing a bit field through any of its aliases is identical.

Byte Ordering

Registers that occupy more than 1 byte of address space are shown with the lowest address in the highest-order byte lane to match the byte-ordering on the bus. For example, the model_id register is R0x0000–1. In the register table the default value is shown as 0x2600. This means that a READ from address 0x0000 would return 0x26, and a READ from address 0x0001 would return 0x00. When reading this register as two 8-bit transfers on the serial interface, the 0x26 will appear on the serial interface first, followed by the 0x00.

Address Alignment

All register addresses are aligned naturally. Registers that occupy two bytes of address space are aligned to even 16-bit addresses, and registers that occupy four bytes of address space are aligned to 16-bit addresses that are an integer multiple of 4.

Bit Representation

For clarity, 32-bit hex numbers are shown with an underscore between the upper and lower 16 bits. For example: 0x3000_01AB.

Data Format

Most registers represent an unsigned binary value or set of bit fields. For all other register formats, the format is stated explicitly at the start of the register description. The notation for these formats is shown in Table 2.

Table 2: Data Formats

Name	Description
FIX16	Signed fixed-point, 16-bit number: two's complement number, 8 fractional bits. Examples: 0x0100 = 1.0, 0x8000 = –128, 0xFFFF = –0.0039065
UFIX16	Unsigned fixed-point, 16-bit number: 8.8 format. Examples: 0x0100 = 1.0, 0x280 = 2.5
FLP32	Signed floating-point, 32-bit number: IEEE 754 format. Example: 0x4280_0000 = 64.0

Register Behavior

Registers vary from "read-only," "read/write," and "read, write-1-to-clear."

Double-Buffered Registers

Some sensor settings cannot be changed during frame readout. For example, changing x_addr_start partway through frame readout would result in inconsistent row lengths within a frame. To avoid this, the AR0134 double-buffers many registers by implementing a "pending" and a "live" version. READs and WRITEs access the pending register; the live register controls the sensor operation.

The value in the pending register is transferred to a live register at a fixed point in the frame timing, called frame start. Frame start is defined as the point at which the first dark row is read out internally to the sensor. In the register tables the "Buffering" column shows which registers or register fields are single- or double-buffered

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame.

Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. If the masked bad frame option is enabled, both LV and FV are inhibited for these frames so that the vertical blanking time between frames is extended by the frame time.

In the register tables, the "Bad Frame" column shows where changing a register or register field will cause a bad frame. This notation is used:

N—No. Changing the register value will not produce a bad frame.
Y—Yes. Changing the register value might produce a bad frame.
YM—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x301A[9]) is set to "1."

Register Summary Tables

Note: Green1 corresponds to greenR; green2 corresponds to greenB.

Caution **Writing and changing the value of a reserved register (word or bit) puts the device in an unknown state and may damage the device.**

Manufacturer-Specific Registers

Table 3: Manufacturer-Specific Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12288 (R0x3000)	chip_version_reg	dddd dddd dddd dddd	9222 (0x2406)
R12290 (R0x3002)	y_addr_start	0000 00dd dddd dddd	0 (0x0000)
R12292 (R0x3004)	x_addr_start	0000 0ddd dddd dddd	0 (0x0000)
R12294 (R0x3006)	y_addr_end	0000 00dd dddd dddd	959 (0x03BF)
R12296 (R0x3008)	x_addr_end	0000 0ddd dddd dddd	1279 (0x04FF)
R12298 (R0x300A)	frame_length_lines	dddd dddd dddd dddd	990 (0x03DE)
R12300 (R0x300C)	line_length_pck	dddd dddd dddd ddd0	1388 (0x056C)
R12302 (R0x300E)	revision_number	dddd dddd	19 (0x13)
R12306 (R0x3012)	coarse_integration_time	dddd dddd dddd dddd	100 (0x0064)
R12308 (R0x3014)	fine_integration_time	dddd dddd dddd dddd	0 (0x0000)
R12310 (R0x3016)	coarse_integration_time_cb	dddd dddd dddd dddd	16 (0x0010)
R12312 (R0x3018)	fine_integration_time_cb	dddd dddd dddd dddd	0 (0x0000)
R12314 (R0x301A)	reset_register	d00d dddd dddd dddd	4312 (0x10D8)
R12318 (R0x301E)	data_pedestal	0000 dddd dddd dddd	300 (0x012C)
R12326 (R0x3026)	gpi_status	0000 0000 0000 ????	0 (0x0000)
R12328 (R0x3028)	row_speed	0000 0000 0ddd 0000	16 (0x0010)
R12330 (R0x302A)	vt_pix_clk_div	0000 0000 dddd dddd	8 (0x0008)
R12332 (R0x302C)	vt_sys_clk_div	0000 0000 000d dddd	1 (0x0001)

Table 3: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12334 (R0x302E)	pre_pll_clk_div	0000 0000 00dd dddd	2 (0x0002)
R12336 (R0x3030)	pll_multiplier	0000 0000 dddd dddd	44 (0x002C)
R12338 (R0x3032)	digital_binning	0000 0000 00dd 00dd	0 (0x0000)
R12346 (R0x303A)	frame_count	dddd dddd dddd dddd	0 (0x0000)
R12348 (R0x303C)	frame_status	0000 0000 0000 00??	0 (0x0000)
R12352 (R0x3040)	read_mode	dd00 0000 0000 0000	0 (0x0000)
R12356 (R0x3044)	dark_control	000d ddd0 d000 dd00	1028 (0x0404)
R12358 (R0x3046)	flash	??00 000d d000 0000	0 (0x0000)
R12374 (R0x3056)	green1_gain	0000 0000 dddd dddd	32 (0x0020)
R12376 (R0x3058)	blue_gain	0000 0000 dddd dddd	32 (0x0020)
R12378 (R0x305A)	red_gain	0000 0000 dddd dddd	32 (0x0020)
R12380 (R0x305C)	green2_gain	0000 0000 dddd dddd	32 (0x0020)
R12382 (R0x305E)	global_gain	0000 0000 dddd dddd	32 (0x0020)
R12388 (R0x3064)	embedded_data_ctrl	000d dddd d0d0 dddd	6530 (0x1982)
R12398 (R0x306E)	datapath_select	dddd dd0d 000d 00dd	36864 (0x9000)
R12400 (R0x3070)	test_pattern_mode	0000 000d 0000 0ddd	0 (0x0000)
R12402 (R0x3072)	test_data_red	0000 dddd dddd dddd	0 (0x0000)
R12404 (R0x3074)	test_data_greenr	0000 dddd dddd dddd	0 (0x0000)
R12406 (R0x3076)	test_data_blue	0000 dddd dddd dddd	0 (0x0000)
R12408 (R0x3078)	test_data_greenb	0000 dddd dddd dddd	0 (0x0000)
R12410 (R0x307A)	test_raw_mode	0000 0000 0000 00dd	0 (0x0000)
R12422 (R0x3086)	seq_data_port	dddd dddd dddd dddd	0 (0x0000)
R12424 (R0x3088)	seq_ctrl_port	?d00 000d dddd dddd	49152 (0xC000)
R12426 (R0x308A)	x_addr_start_cb	0000 0ddd dddd dddd	2 (0x0002)

Table 3: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12428 (R0x308C)	y_addr_start_cb	0000 00dd dddd dddd	4 (0x0004)
R12430 (R0x308E)	x_addr_end_cb	0000 0ddd dddd dddd	1281 (0x0501)
R12432 (R0x3090)	y_addr_end_cb	0000 00dd dddd dddd	963 (0x03C3)
R12448 (R0x30A0)	x_even_inc	0000 0000 0000 000?	1 (0x0001)
R12450 (R0x30A2)	x_odd_inc	0000 0000 0000 000d	1 (0x0001)
R12452 (R0x30A4)	y_even_inc	0000 0000 0000 000?	1 (0x0001)
R12454 (R0x30A6)	y_odd_inc	0000 0000 0ddd dddd	1 (0x0001)
R12456 (R0x30A8)	y_odd_inc_cb	0000 0000 0ddd dddd	63 (0x003F)
R12458 (R0x30AA)	frame_length_lines_cb	dddd dddd dddd dddd	90 (0x005A)
R12460 (R0x30AC)	frame_exposure	???? ???? ???? ????	16 (0x0010)
R12464 (R0x30B0)	digital_test	dddd dddd dddd 0000	128 (0x0080)
R12466 (R0x30B2)	tempsens_data	0000 00dd dddd dddd	0 (0x0000)
R12468 (R0x30B4)	tempsens_ctrl	0000 0000 00dd dddd	0 (0x0000)
R12476 (R0x30BC)	green1_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12478 (R0x30BE)	blue_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12480 (R0x30C0)	red_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12482 (R0x30C2)	green2_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12484 (R0x30C4)	global_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12486 (R0x30C6)	tempsens_calib1	dddd dddd dddd dddd	0 (0x0000)
R12488 (R0x30C8)	tempsens_calib2	dddd dddd dddd dddd	0 (0x0000)
R12490 (R0x30CA)	tempsens_calib3	dddd dddd dddd dddd	0 (0x0000)
R12492 (R0x30CC)	tempsens_calib4	dddd dddd dddd dddd	0 (0x0000)
R12500 (R0x30D4)	column_correction	ddd0 0000 0000 dddd	57351 (0xE007)
R12544 (R0x3100)	ae_ctrl_reg	0000 0000 0ddd dddd	0 (0x0000)

Table 3: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12546 (R0x3102)	ae_luma_target_reg	dddd dddd dddd dddd	1280 (0x0500)
R12552 (R0x3108)	ae_min_ev_step_reg	dddd dddd dddd dddd	112 (0x0070)
R12554 (R0x310A)	ae_max_ev_step_reg	dddd dddd dddd dddd	8 (0x0008)
R12556 (R0x310C)	ae_damp_offset_reg	dddd dddd dddd dddd	512 (0x0200)
R12558 (R0x310E)	ae_damp_gain_reg	dddd dddd dddd dddd	8192 (0x2000)
R12560 (R0x3110)	ae_damp_max_reg	dddd dddd dddd dddd	320 (0x0140)
R12572 (R0x311C)	ae_max_exposure_reg	dddd dddd dddd dddd	672 (0x02A0)
R12574 (R0x311E)	ae_min_exposure_reg	dddd dddd dddd dddd	1 (0x0001)
R12580 (R0x3124)	ae_dark_cur_thresh_reg	dddd dddd dddd dddd	32767 (0x7FFF)
R12586 (R0x312A)	ae_current_gains	0000 00?? ???? ????	32 (0x0020)
R12608 (R0x3140)	ae_roi_x_start_offset	0000 0ddd dddd ddd0	0 (0x0000)
R12610 (R0x3142)	ae_roi_y_start_offset	0000 00dd dddd ddd0	0 (0x0000)
R12612 (R0x3144)	ae_roi_x_size	0000 0ddd dddd ddd0	1280 (0x0500)
R12614 (R0x3146)	ae_roi_y_size	0000 00dd dddd ddd0	960 (0x03C0)
R12626 (R0x3152)	ae_mean_l	???? ???? ???? ????	0 (0x0000)
R12644 (R0x3164)	ae_coarse_integration_time	???? ???? ???? ????	0 (0x0000)
R12646 (R0x3166)	ae_ag_exposure_hi	dddd dddd dddd dddd	986 (0x03DA)
R12648 (R0x3168)	ae_ag_exposure_lo	dddd dddd dddd dddd	419 (0x01A3)
R12680 (R0x3188)	delta_dk_level	???? ???? ???? ????	0 (0x0000)
R12736 (R0x31C0)	hispi_timing	0ddd dddd dddd dddd	0 (0x0000)
R12742 (R0x31C6)	hispi_control_status	??00 00dd dddd dd00	32768 (0x8000)
R12744 (R0x31C8)	hispi_crc_0	???? ???? ???? ????	65535 (0xFFFF)
R12746 (R0x31CA)	hispi_crc_1	???? ???? ???? ????	65535 (0xFFFF)
R12748 (R0x31CC)	hispi_crc_2	???? ???? ???? ????	65535 (0xFFFF)

Table 3: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12750 (R0x31CE)	hispi_crc_3	???? ???? ???? ????	65535 (0xFFFF)
R12754 (R0x31D2)	stat_frame_id	dddd dddd dddd dddd	0 (0x0000)
R12758 (R0x31D6)	i2c_wrt_checksum	dddd dddd dddd dddd	65535 (0xFFFF)
R12776 (R0x31E8)	horizontal_cursor_position	0000 00dd dddd dddd	0 (0x0000)
R12778 (R0x31EA)	vertical_cursor_position	0000 0ddd dddd dddd	0 (0x0000)
R12780 (R0x31EC)	horizontal_cursor_width	0000 00dd dddd dddd	0 (0x0000)
R12782 (R0x31EE)	vertical_cursor_width	0000 0ddd dddd dddd	0 (0x0000)
R12796 (R0x31FC)	i2c_ids	dddd dddd dddd dddd	12320 (0x3020)

Detailed Register Descriptions

Manufacturer-Specific Registers

Table 4: Manufacturer-Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12288 R0x3000	15:0	0x2406	chip_version_reg (R/W)	N	N	
	Model ID. Read-only. Can be made read/write by clearing R0x301A[3].					
12290 R0x3002	15:0	0x0000	y_addr_start (R/W)	Y	YM	D
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.					
12292 R0x3004	15:0	0x0000	x_addr_start (R/W)	Y	N	D
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value.					
12294 R0x3006	15:0	0x03BF	y_addr_end (R/W)	Y	YM	D
	The last row of visible pixels to be read out.					
12296 R0x3008	15:0	0x04FF	x_addr_end (R/W)	Y	N	D
	The last column of visible pixels to be read out.					
12298 R0x300A	15:0	0x03DE	frame_length_lines (R/W)	Y	YM	D
	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines.					
12300 R0x300C	15:0	0x056C	line_length_pck (R/W)	Y	YM	S
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. The minimum supported value is 0x056C.					
12302 R0x300E	7:0	0x13	revision_number (R/W) The upper four bits represent silicon revision, the lower four bits indicate OTPM version.	N	N	
12306 R0x3012	15:0	0x0064	coarse_integration_time (R/W)	Y	N	S
	Integration time specified in multiples of line_length_pck_.					
12308 R0x3014	15:0	0x0000	fine_integration_time (R/W)	Y	N	D
	The fine integration time increases the integration time. The resolution is 1 pixel clock time.					
12310 R0x3016	15:0	0x0010	coarse_integration_time_cb (R/W)	N	N	S
	Coarse integration time in context B.					
12312 R0x3018	15:0	0x0000	fine_integration_time_cb (R/W)	N	N	D
	Fine integration time in context B.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12314 R0x301A	15:0	0x10D8	reset_register (R/W)	N	Y	
	15	0x0000	grouped_parameter_hold 0: Register updates are synchronized to next frame start. 1: Register changes will remain pending until this bit is returned to 0, after which the register updates will take effect at the next frame start.	N	N	
	14:13	X	Reserved			
	12	0x0001	smia_serialiser_dis This bit disables the serial (HiSPi) interface	N	N	
	11	0x0000	forced_pll_on When set, forces the PLL on, no matter sensor state.	N	N	
	10	0x0000	restart_bad 1: A restart is forced any time a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay for masking out a bad frame will be the integration time rather than the full-frame time.	N	N	
	9	0x0000	mask_bad 0: The sensor will produce bad (corrupted) frames as a result of some register changes. 1: Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame.	N	N	
	8	0x0000	gpi_en 0: The primary input buffers associated with the OUTPUT_ENABLE_N, TRIGGER and STANDBY inputs are powered down and cannot be used. 1: The input buffers are enabled and can be read through R0x3026.	N	N	
	7	0x0001	parallel_en 0: The parallel data interface (DOUT[9:0], LINE_VALID, FRAME_VALID, and PIXCLK) is disabled and the outputs are placed in a high-impedance state. 1: The parallel data interface is enabled. The output signals can be switched between a driven and a high-impedance state using output-enable control.	N	N	
	6	0x0001	drive_pins 0: The parallel data interface (DOUT[9:0], LINE_VALID, FRAME_VALID, and PIXCLK) may enter a high-impedance state (depending upon the configuration of R0x3026). 1: The parallel data interface is driven. This bit is “do not care” unless bit[7]=1.	N	N	
	5	X	Reserved			
	4	0x0001	stdby_eof 0: Transition to standby is synchronized to the end of a sensor row readout (held-off until LINE_VALID has fallen). 1: Transition to standby is synchronized to the end of a frame.	N	Y	
	3	0x0001	lock_reg Many parameter limitation registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows such registers to be written.	N	N	

Table 4: Manufacturer-Specific Register Descriptions (continued)

R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
	2	0x0000	stream Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	Y	N	
	1	0x0000	restart This bit always reads as 0. Setting this bit has two effects: first, the current frame is read out and the sensor enters standby. Second, any writes to frame-synchronized registers and the shutter width registers take effect immediately, and a new frame starts. The current frame completes before the new frame is started, so the time between issuing the Restart and the beginning of the next frame is a maximum of t_{FRAME}	N	Y	
	0	0x0000	reset This bit always reads as 0. Setting this bit initiates a reset sequence: the frame being generated will be truncated.	N	Y	
	Controls the operation of the sensor. For details see the bit field descriptions.					
12318 R0x301E	15:0	0x012C	data_pedestal (R/W)	N	Y	
	Constant offset that is added to pixel values at the end of datapath (after all corrections).					
12326 R0x3026	15:0	0x0000	gpi_status (RO)	N	N	
	15:4	X	Reserved			
	3	RO	standby Read-only. Return the current state of the STANDBY input pin. Invalid if R0x301A[8]=0.	N	N	
	2	RO	trigger Read-only. Return the current state of the TRIGGER input pin. Invalid if R0x301A[8]=0.	N	N	
	1	RO	oe_n Read-only. Return the current state of the OUTPUT_ENABLE_N input pin. Invalid if R0x301A[8]=0.	N	N	
	0	RO	saddr Read-only. Return the current state of the pin SADDR input pin. Invalid if R0x301A[8]=0.	N	N	
	Reflects the status of the input pins: STANDBY(3), TRIGGER(2), OUTPUT_ENABLE_N(1). Bit 0 is not used.					
12328 R0x3028	15:0	0x0010	row_speed (R/W)	N	N	
	Bits [6:4] of this register define the phase of the output pixclk. 2 sets of values are valid: a) 000, 010, 100, 110 => 0 delay (rising edge of PIXCLK coincides DOUT change). b) 001, 011, 101, 111 => 1/2 clk delay (falling edge of pixclk coincides DOUT change).					
12330 R0x302A	15:0	0x0008	vt_pix_clk_div (R/W)	N	N	
	Sets the ratio of the serial output clock and sensor operation clock (P2 clock divider in PLL).					
12332 R0x302C	15:0	0x0001	vt_sys_clk_div (R/W)	N	N	
	Sets the ratio of the VCO clk and the serial output clock (P1 divider in PLL).					
12334 R0x302E	15:0	0x0002	pre_pll_clk_div (R/W)	N	N	
	Referring to the PLL documentation: shows the n value.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12336 R0x3030	15:0	0x002C	pll_multiplier (R/W)	N	N	
	PLL_MULTIPLIER: shows m value.					
12338 R0x3032	15:0	0x0000	digital_binning (R/W)	N	N	
	15:6	X	Reserved			
	5:4	0x0000	digital_binning_cb DIGITAL_BINNING for context B 00: No binning 01: Horizontal only binning 10: Horizontal and Vertical binning	N	N	
	3:2	X	Reserved			
	1:0	0x0000	digital_binning_ca DIGITAL_BINNING for context A 00: No binning 01: Horizontal only binning 10: Horizontal and Vertical binning	N	N	
12346 R0x303A	15:0	0x0000	frame_count (R/W)	N	N	
	Counts the number of output frames. At the startup is initialized to 0xffff.					
12348 R0x303C	15:0	0x0000	frame_status (RO)	N	N	
	15:2	X	Reserved			
	1	RO	standby_status This bit indicates whether the sensor is in standby state. Can be polled after standby is entered to see when the real low-power state is entered; which can happen at the end of row or frame depending on bit R0x301A[4].	N	N	
	0	RO	framesync Set on register write and reset on frame synchronization. Acts as debug flag to verify that register writes completed before last frame synchronization.	N	N	
12352 R0x3040	15:0	0x0000	read_mode (R/W)	Y	YM	
	15	0x0000	vert_flip 0: Normal readout 1: Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ is read out of the sensor first. Setting this bit will change the Bayer pixel order.	Y	YM	D
	14	0x0000	horiz_mirror 0: Normal readout 1: Readout is mirrored horizontally so that the column specified by x_addr_end_ is read out of the sensor first. Setting this bit will change the Bayer pixel order.	Y	YM	D
	13:0	X	Reserved			

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12356 R0x3044	15:0	0x0404	dark_control (R/W)	N	N	
	15:13	X	Reserved			
	12	0x0000	show_colcorr_rows When set, the column correction and delta dark rows are included in the frame valid and are output from the chip. The order of lines in frame valid will be: col_corr, delta dark, embedded data, image data,.. No correction will be applied to the data.	N	N	
	11	0x0000	show_dark_extra_rows When set, the delta dark rows (including the guard/extra rows) will be included in frame valid and output. The order of rows will be: delta dark rows, embedded data, image data, .. No correction will be applied to the dark row data.	N	N	
	10	0x0001	row_noise_correction_en 0: Row-noise cancellation algorithm is disabled 1: Row-noise cancellation algorithm is enabled.	N	N	
	9	0x0000	show_dark_cols When set, the row noise correction columns (tied pixels) will be added to line valid and output. No correction will be applied to the dark row data.	N	N	
	8:0	X	Reserved			
12358 R0x3046	15:0	0x0000	flash (R/W)	Y	Y	
	15	RO	strobe Reflects the current state of the FLASH output signal. Read-only.	N	N	
	14	RO	triggered Indicates that the FLASH output signal was asserted for the current frame. Read-only.	N	N	
	13:9	X	Reserved			
	8	0x0000	en_flash Enables LED flash. The flash is asserted with the start integration. The flash is de-asserted when the integration is complete.	Y	Y	S
	7	0x0000	invert_flash Invert flash output signal. When set, the FLASH output signal will be active low.	N	N	
	6:0	X	Reserved			
12374 R0x3056	15:0	0x0020	green1_gain (R/W)	Y	N	D
	Digital gain for green1 (Gr) pixels, in format of xxx.yyyyy.					
12376 R0x3058	15:0	0x0020	blue_gain (R/W)	Y	N	D
	Digital gain for Blue pixels,, in format of xxx.yyyyy.					
12378 R0x305A	15:0	0x0020	red_gain (R/W)	Y	N	D
	Digital gain for Red pixels, in format of xxx.yyyyy.					
12380 R0x305C	15:0	0x0020	green2_gain (R/W)	Y	N	D
	Digital gain for green2 (Gb) pixels in format of xxx.yyyyy.					
12382 R0x305E	15:0	0x0020	global_gain (R/W)	Y	N	D
	Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain registers. Reading from this register returns the value most recently written to the green1_gain register.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12388 R0x3064	15:0	0x1982	embedded_data_ctrl (R/W)	N	N	
	15:13	X	Reserved			
	12	X	Reserved			
	11:10	X	Reserved			
	9	X	Reserved			
	8	0x0001	embedded_data 0: Frames out of the sensor exclude the embedded data. 1: Frames out of the sensor include 2 rows of embedded data. This register field should only be changed while the sensor is in software standby.	N	N	
	7	0x0001	embedded_stats_en Enables two rows of statistical data (used by external auto-exposure), after the transmission image data. Cannot be enabled unless EMBEDDED_DATA_EN is enabled.	N	Y	
	6:4	X	Reserved			
	3:0	X	Reserved			
12398 R0x306E	15:0	0x9000	datapath_select (R/W)	N	N	
	15:13	0x0004	slew_rate_ctrl_parallel Selects the slew (edge) rate for the DOUT[9:0], FRAME_VALID, LINE_VALID and FLASH outputs. Only affects FLASH outputs when parallel data output is disabled. The value 7 results in the fastest edge rates on these signals. Slowing down the edge rate can reduce ringing and electromagnetic emissions.	N	N	
	12:10	0x0004	slew_rate_ctrl_pixclk Selects the slew (edge) rate for the PIXCLK output. Has no effect when parallel data output is disabled. The value 7 results in the fastest edge rates on this signal. Slowing down the edge rate can reduce ringing and electromagnetic emissions.	N	N	
	9	X	Reserved			
	8	0x0000	postscaler_data_sel 0: Statistics data are generated from pixel data before scaler. 1: Statistics data are generated from pixel data after scaler.	N	N	
	7:5	X	Reserved			
	4	0x0000	true_bayer Enables true Bayer scaling mode.	N	N	
	3:2	X	Reserved			
	1:0	0x0000	special_line_valid 00: Normal behavior of LINE_VALID 01: LINE_VALID is driven continuously (continue generating LINE_VALID during vertical blanking) 10: LINE_VALID is driven continuously as LINE_VALID XOR FRAME_VALID	N	N	
12400 R0x3070	15:0	0x0000	test_pattern_mode (R/W)	N	Y	
	0: Normal operation: Generate output data from pixel array 1: Solid color test pattern. 2: 100% color bar test pattern 3: Fade to gray color bar test pattern 256 : Walking 1s test pattern (12 bit) Other: Reserved.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12402 R0x3072	15:0	0x0000	test_data_red (R/W)	N	Y	
	The value for red pixels in the Bayer data used for the solid color test pattern and the test cursors.					
12404 R0x3074	15:0	0x0000	test_data_greenr (R/W)	N	Y	
	The value for green pixels in red/green rows of the Bayer data used for the solid color test pattern and the test cursors.					
12406 R0x3076	15:0	0x0000	test_data_blue (R/W)	N	Y	
	The value for blue pixels in the Bayer data used for the solid color test pattern and the test cursors.					
12408 R0x3078	15:0	0x0000	test_data_greenb (R/W)	N	Y	
	The value for green pixels in blue/green rows of the Bayer data used for the solid color test pattern and the test cursors.					
12422 R0x3086	15:0	0x0000	seq_data_port (R/W)	N	N	
	Register used to write to or read from the sequencer RAM.					
12424 R0x3088	15:0	0xC000	seq_ctrl_port (R/W)	N	N	
	15	RO	sequencer_stopped Showing that sequencer is stopped (STANDBY mode) and the RAM is available for read or write.	N	N	
	14	0x0001	auto_inc_on_read 1: The access_address is incremented (by 1) after each read operation from seq_data_port (which returns only1 byte)	N	N	
	13:9	X	Reserved			
	8:0	0x0000	access_address When in STANDBY (not streaming) mode: address pointer to the sequencer RAM.	N	N	
	Register controlling the read and write to sequencer RAM.					
12426 R0x308A	15:0	0x0002	x_addr_start_cb (R/W)	N	N	D
	x_address_start context B					
12428 R0x308C	15:0	0x0004	y_addr_start_cb (R/W)	N	N	D
	y_addr_start for context B					
12430 R0x308E	15:0	0x0501	x_addr_end_cb (R/W)	N	N	D
	x_addr_end for context B					
12432 R0x3090	15:0	0x03C3	y_addr_end_cb (R/W)	N	N	D
	Y_ADDR_END for context B					
12448 R0x30A0	15:0	0x0001	x_even_inc (RO)	N	N	
	Read-only.					
12450 R0x30A2	15:0	0x0001	x_odd_inc (R/W)	Y	YM	
	Not supported.					
12452 R0x30A4	15:0	0x0001	y_even_inc (RO)	N	N	
	Read-only.					
12454 R0x30A6	15:0	0x0001	y_odd_inc (R/W)	Y	YM	D
	Row skip factor: 1: No Skip 3: Skip Factor 2 7: Skip Factor 4 15: Skip Factor 8 31: Skip Factor 16 63: Skip Factor 32 127: Skip Factor 64					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12456 R0x30A8	15:0	0x003F	y_odd_inc_cb (R/W)	N	N	D
	y_odd_inc for context B					
12458 R0x30AA	15:0	0x005A	frame_length_lines_cb (R/W)	N	N	D
	frame_length_lines for context B.					
12460 R0x30AC	15:0	0x0010	frame_exposure (LK)	N	N	
	Shows the current frame exposure time in rows.					
12464 R0x30B0	15:0	0x0080	digital_test (R/W)	N	Y	
	15	X	Reserved			
	14	0x0000	pll_complete_bypass When set, the EXTCLK will be used and PLL will be completely bypassed. Note that the serial interface would not function.	N	N	
	13	0x0000	context_b 0: Use context A 1: Use Context B	N	N	
	12:11	X	Reserved			
	10	0x0000	enable_short_llpck This bit allows the line length to be reduced to 1388 and must be set to 1 for correct line timing for non-skipping modes. It must be set to 0 for skip modes. Triggered mode does not support short line lengths - so it must be set to 0 for trigger mode.	N	N	
	9:8	0x0000	col_gain_cb Column gain for Context B 00: 1 01: 2 10: 4 11: 8	N	N	D
	7	0x0001	mono_chrome When set the CFA is monochrome and not color. Some features like skipping and corrections are affected.	N	N	
	6	X	Reserved			
	5:4	0x0000	col_gain Column gain: 00: 1 01: 2 10: 4 11: 8	N	N	D
	3:0	X	Reserved			
12466 R0x30B2	15:0	0x0000	tempsens_data (R/W)	N	N	
	Data from temperature sensor					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12468 R0x30B4	15:0	0x0000	tempsens_ctrl (R/W)	N	N	
	15:6	X	Reserved			
	5	0x0000	temp_clear_value	N	N	
	4	0x0000	temp_start_conversion	N	N	
	3:1	0x0000	tempsens_test_ctrl	N	N	
	0	0x0000	tempsens_power_on	N	N	
	Control register for temp sensor: Bit[0]: Tempsens power on when set. Bits [3:1]: Tempsens test ctrl Bit [4]: Tempsens starts conversion when set Bit [5]: Tempsens clears value when set.					
12476 R0x30BC	15:0	0x0020	green1_gain_cb (R/W)	N	N	D
	Digital gain green1 context B					
12478 R0x30BE	15:0	0x0020	blue_gain_cb (R/W)	N	N	D
	digital gain blue context B					
12480 R0x30C0	15:0	0x0020	red_gain_cb (R/W)	N	N	D
	digital gain red context B					
12482 R0x30C2	15:0	0x0020	green2_gain_cb (R/W)	N	N	D
	digital gain green 2 context B					
12484 R0x30C4	15:0	0x0020	global_gain_cb (R/W)	N	N	D
	global digital gain context B					
12486 R0x30C6	15:0	0x0000	tempsens_calib1 (R/W) This register will read out sensor-specific calibration data.	N	N	
12488 R0x30C8	15:0	0x0000	tempsens_calib2 (R/W) This register will read out sensor-specific calibration data.	N	N	
12490 R0x30CA	15:0	0x0000	tempsens_calib3 (R/W) This register is not used.	N	N	
12492 R0x30CC	15:0	0x0000	tempsens_calib4 (R/W) This register is not used.			
12500 R0x30D4	15:0	0xE007	column_correction (R/W)	N	N	
	15	0x0001	enable Enable column correction.	N	N	
	14	0x0001	double_range Doubles the range of the correction value but halves the precision.	N	N	
	13	0x0001	double_samples Makes the column correction use 128 rows instead of 64. Adds 64 to the minimum frame blanking.	N	N	
	12:4	X	Reserved			
	3:0	0x0007	colcorr_rows Value showing the number of column correction rows - 1.	N	N	

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12544 R0x3100	15:0	0x0000	ae_ctrl_reg (R/W)			
	15:7	X	Reserved			
	6:5	0x0000	min_ana_gain Minimum analog gain to be used by AE. 00:1x (default) 01: 2x 10: 4x 11: 8x	N	N	
	4	0x0000	auto_dg_en Automatic control of digital gain by AE is enabled.	N	N	
	3:2	X	Reserved			
	1	0x0000	auto_ag_en When set, enables the automatic AE control of analog gain.	N	N	
	0	0x0000	ae_enable 1: Enables the on-chip AE algorithm. Auto Exposure also requires embedded_data_en R0x3064[8] and embedded_stats_en R0x3064[7] to be set to 1 for proper operation.	N	N	
12546 R0x3102	15:0	0x0500	ae_luma_target_reg (R/W)	N	N	
	Average luma target value to be reached by the auto exposure					
12552 R0x3108	15:0	0x0070	ae_min_ev_step_reg (R/W)	N	N	
	Minimum exposure value step size [15:8]: Reserved [7:0] : Min_EV_stepsize = (min step size)*256. Since Min_EV_step sizes are small and they are typically less than 1 e.g. 1/16, 7/16 etc... these are multiplied by 256 and then the value is written to this register.					
12554 R0x310A	15:0	0x0008	ae_max_ev_step_reg (R/W)	N	N	
	Maximum exposure value step size. Note that since this value is always greater than 1 there is no need to multiply by 256 as in the case of min_EV_stepsize.					
12556 R0x310C	15:0	0x0200	ae_damp_offset_reg (R/W)	N	N	
	Adjusts step size and settling speed.					
12558 R0x310E	15:0	0x2000	ae_damp_gain_reg (R/W)	N	N	
	Adjusts step size and settling speed.					
12560 R0x3110	15:0	0x0140	ae_damp_max_reg (R/W)			
	Max value allowed for recursiveDamp (multiplied by 256 since internal value is typical <1). For most applications, the value of recursiveDamp should be <1, otherwise AE will overshoot the target. For applications with fast settling required, it may be desirable to allow recursiveDamp >1. Default value: 0.875 * 256 = 0x00E0					
12572 R0x311C	15:0	0x02A0	ae_max_exposure_reg (R/W)	N	N	
	Maximum integration (exposure) time in rows to be used by AE.					
12574 R0x311E	15:0	0x0001	ae_min_exposure_reg (R/W)			
	Minimum integration (exposure) time in rows to be used by AE.					
12580 R0x3124	15:0	0x7FFF	ae_dark_cur_thresh_reg (R/W)			
	The dark current level that stops AE from increasing integration time. Note that increased integration time would increase dark current as well and signal level (SNR) would drop because photo diode well capacity is limited.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12586 R0x312A	15:0	0x0020	ae_current_gains (RO)			
	15:10	X	Reserved			
	9:8	RO	ae_ana_gain The gain decided by AE, when it is enabled and can control the analog gain.	N	N	
	7:0	RO	ae_dig_gain The gain decided by AE, when it is enabled and can control the digital gain.	N	N	
	Shows the gain settings decided by AE.					
12608 R0x3140	15:0	0x0000	ae_roi_x_start_offset (R/W)			
	Number of pixels into each row before the ROI starts NOTE: if statistics are being gathered from a scaled image then the 'number of pixels' value must be the number of scaled pixels					
12610 R0x3142	15:0	0x0000	ae_roi_y_start_offset (R/W)			
	Number of rows into each frame before the ROI starts					
12612 R0x3144	15:0	0x0500	ae_roi_x_size (R/W)			
	Number of columns in the ROI					
12614 R0x3146	15:0	0x03C0	ae_roi_y_size (R/W)			
	Number of rows in the ROI					
12626 R0x3152	15:0	0x0000	ae_mean_l (RO)			
	The true mean of all Gr pixels in the ROI (16 least significant bits)					
12644 R0x3164	15:0	0x0000	ae_coarse_integration_time (RO)			
	The integration time decided by AE.					
12646 R0x3166	15:0	0x03DA	ae_ag_exposure_hi (R/W)			
	At this integration time, the analog gain is increased (when AE is enabled to control also the analog gain).					
12648 R0x3168	15:0	0x01A3	ae_ag_exposure_lo (R/W)	N	N	
	At this integration time, the AE is reduced (when AE is enabled to control the analog gain also),					
12680 R0x3188	15:0	0x0000	delta_dk_level (RO)	N	N	
	Measured dark current.					
12736 R0x31C0	15:0	0x0000	hispi_timing (R/W)	N	N	
	Bits [2:0]: DLL delay setting for data lane 0 Bits [5:3]: DLL delay setting for data lane 1 Bits [8:6]: DLL delay setting for data lane 2 Bits [11:9]: DLL delay setting for data lane 3 Bits [14:12]: DLL delay setting for clock lane The delay setting selects a tap along a delay element. Each stage is 1/8 of a symbol period. When the delay is set to zero, the delay element is powered down.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12742 R0x31C6	15:0	0x8000	hispi_control_status (R/W)	N	N	
	15:14	RO	hispi_status	N	N	
	13:10	X	Reserved			
	9:2	0x0000	hispi_control Bit[2]: Stream mode enable. Bit[3]: Enable 3 lanes for compressed data Bit[6:4]: Test mode: ///////////////////////////////// 000: Transmit constant 0 on all enabled data lanes. 001: Transmit constant 1 on all enabled data lanes. 010: Transmit square wave at the half the potential serial data rate on all the enabled lanes. 011: Transmit square wave at the pixel data rate on all the enabled lanes. 100: Transmit a continuous, repeated, sequence of pseudo random data, with no SAV code, copied on all enabled data lanes. 101: Replace pixel data with a known sequence (PN9), copied on all the enabled data lanes. /// Bit[7]: Test mode enable Bit[8]: IO test enable Bit[9]: Frame wide checksum test enable	N	N	
	1:0	X	Reserved			
12744 R0x31C8	15:0	0xFFFF	hispi_crc_0 (RO)	N	N	
12746 R0x31CA	15:0	0xFFFF	hispi_crc_1 (RO)			
12748 R0x31CC	15:0	0xFFFF	hispi_crc_2 (RO)	N	N	
12750 R0x31CE	15:0	0xFFFF	hispi_crc_3 (RO)			
12754 R0x31D2	15:0	0x0000	stat_frame_id (R/W)	N	N	
12758 R0x31D6	15:0	0xFFFF	i2c_wrt_checksum (R/W)	N	N	
	Checksum of I^2C write operations.					
12776 R0x31E8	15:0	0x0000	horizontal_cursor_position (R/W)	N	N	
	Specifies the start row for the test cursor.					
12778 R0x31EA	15:0	0x0000	vertical_cursor_position (R/W)	N	N	
	Specifies the start column for the test cursor.					
12780 R0x31EC	15:0	0x0000	horizontal_cursor_width (R/W)	N	N	
	Specifies the width, in rows, of the horizontal test cursor. A width of 0 disables the cursor.					
12782 R0x31EE	15:0	0x0000	vertical_cursor_width (R/W)			
	Specifies the width, in columns, of the vertical test cursor. A width of 0 disables the cursor.					
12796 R0x31FC	15:0	0x3020	i2c_ids (R/W)	N	N	
	I^2C addresses.					

Revision History

Rev. D **6/12/14**

- Updated corporate address on last page
- Deleted lock_control from Table 3, "Manufacturer-Specific Register List," on page 7 and Table 4, "Manufacturer-Specific Register Descriptions," on page 12
- Updated descriptions of register field "restart" and "enable_short_llpck" in Table 3, "Manufacturer-Specific Register List," on page 7 and Table 4, "Manufacturer-Specific Register Descriptions," on page 12
- Updated description of register field "col_gain_cb" in Table 4.

Rev. C **4/25/13**

- Updated to Production
- Updated default values of:
  - frame_length_lines
  - digital_test
  - enable_short_llpck
  - revision_number
- Updated description of ae_enable

Rev. B **1/23/13**

- Updated to Preliminary
- Updated the default values for:
  - revision_number
  - reset_register
  - digital_test
  - tempsens_calib1
  - tempsens_calib2
  - tempsens_calib3
  - tempsens_calib4
- Updated the descriptions for:
  - frame_length_lines
  - line_length_pck
  - show_dark_extra_rows
  - show_dark_cols
  - enable_short_llpck
  - tempsens_calib1
  - tempsens_calib2
  - tempsens_calib3
  - tempsens_calib4
  - grouped_parameter_hold
- Added description for bit 10 of R0x30B0
- Updated "Bad Frames" on page 6

Revision A **11/2/12**

- Initial release

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