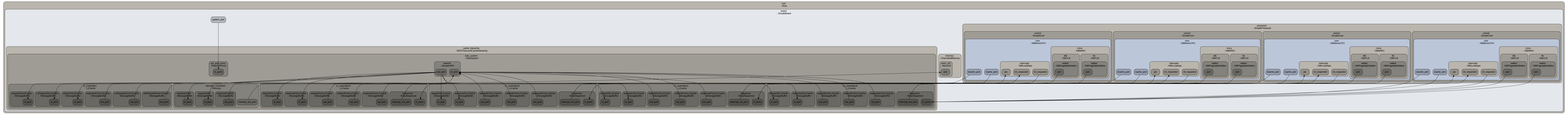

root
: Root
board
: SimpleBoard
system_port
cache_hierarchy
: MESITwoLevelCacheHierarchy
ruby_system
: RubySystem
sys_port_proxy
: RubyPortProxy
in_ports
network
: SimplePt2Pt
out_port
in_port
l2_controllers
: L2Cache
responseToL2Cache
: MessageBuffer
in_port
L1RequestToL2Cache
: MessageBuffer
in_port
unblockToL2Cache
: MessageBuffer
in_port
responseFromL2Cache
: MessageBuffer
out_port
L1RequestFromL2Cache
: MessageBuffer
out_port
DirRequestFromL2Cache
: MessageBuffer
out_port
directory_controllers
: Directory
responseToDir
: MessageBuffer
in_port
requestToDir
: MessageBuffer
in_port
responseFromDir
: MessageBuffer
out_port
memory_out_port
l1_controllers3
: L1Cache
requestToL1Cache
: MessageBuffer
in_port
responseToL1Cache
: MessageBuffer
in_port
requestFromL1Cache
: MessageBuffer
out_port
unblockFromL1Cache
: MessageBuffer
out_port
responseFromL1Cache
: MessageBuffer
out_port
sequencer
: RubySequencer
interrupt_out_port
in_ports
l1_controllers2
: L1Cache
requestToL1Cache
: MessageBuffer
in_port
responseToL1Cache
: MessageBuffer
in_port
requestFromL1Cache
: MessageBuffer
out_port
unblockFromL1Cache
: MessageBuffer
out_port
responseFromL1Cache
: MessageBuffer
out_port
sequencer
: RubySequencer
interrupt_out_port
in_ports
l1_controllers1
: L1Cache
requestToL1Cache
: MessageBuffer
in_port
responseToL1Cache
: MessageBuffer
in_port
requestFromL1Cache
: MessageBuffer
out_port
unblockFromL1Cache
: MessageBuffer
out_port
responseFromL1Cache
: MessageBuffer
out_port
sequencer
: RubySequencer
interrupt_out_port
in_ports
l1_controllers0
: L1Cache
requestToL1Cache
: MessageBuffer
in_port
responseToL1Cache
: MessageBuffer
in_port
requestFromL1Cache
: MessageBuffer
out_port
unblockFromL1Cache
: MessageBuffer
out_port
responseFromL1Cache
: MessageBuffer
out_port
sequencer
: RubySequencer
interrupt_out_port
in_ports
memory
: ChanneledMemory
mem_ctrl
: MemCtrl
port
processor
: SimpleProcessor
cores3
: SimpleCore
core
: X86MinorCPU
mmu
: X86MMU
dtb
: X86TLB
walker
: X86PagetableWalker
port
itb
: X86TLB
walker
: X86PagetableWalker
port
interrupts
: X86LocalApic
pio
int_responder
int_requestor
dcache_port
icache_port
cores2
: SimpleCore
core
: X86MinorCPU
mmu
: X86MMU
dtb
: X86TLB
walker
: X86PagetableWalker
port
itb
: X86TLB
walker
: X86PagetableWalker
port
interrupts
: X86LocalApic
pio
int_responder
int_requestor
dcache_port
icache_port
cores1
: SimpleCore
core
: X86MinorCPU
mmu
: X86MMU
dtb
: X86TLB
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: X86PagetableWalker
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