SANTA CLARA UNIVERSITY	ELEN 153	TA: Vinay Krishna Andra
Laboratory #8: Hierarchical Design Part 2– Four-Bit Adder Layout		

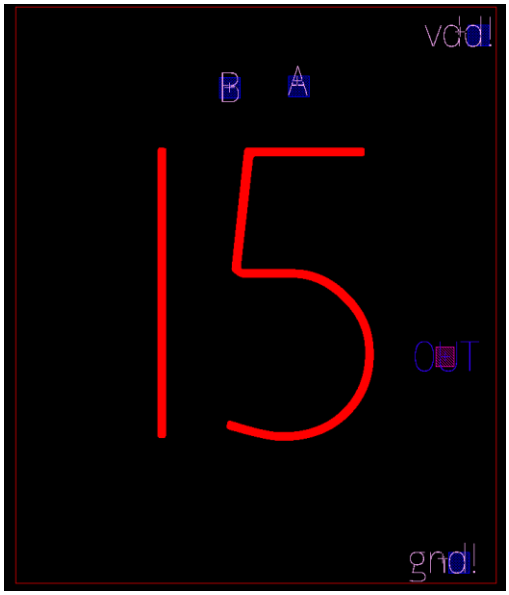
I. OBJECTIVES

- To learn how to create complex layouts using bottom-up hierarchical design.
- To create a four-bit adder layout and verify it with DRC and LVS

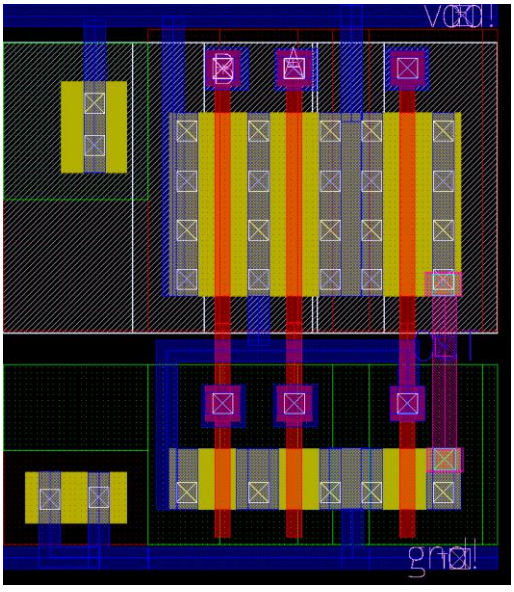
II. LAB PROCEDURE

- **Layout View Change: To view all the layers of the layout block that you import to your layout use 'SHIFT+F' and to navigate back to the block view (to not see all the layers) use 'CTRL+F'. To make sure that you make the right connections while working with multiple such layout blocks, try to work with all the layers visible.**

CTRL+F



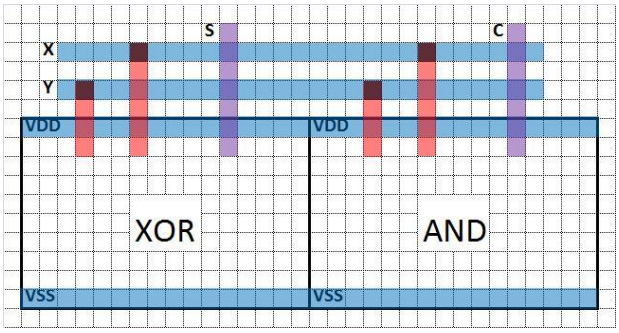
SHIFT+F



NOTE: Below floor plans are for reference only. The connections might change based upon your schematics.

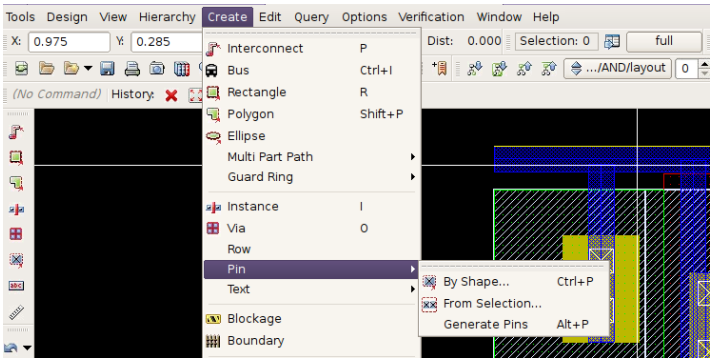
1. Half Adder

- Create the Half-adder layout as shown below, using AND, and XOR primitive cells.
- To add the AND and XOR gate layout. Select Create→ instance, or press " i" for its keyboard shortcut. Then select the layout you desire and place it as shown below.

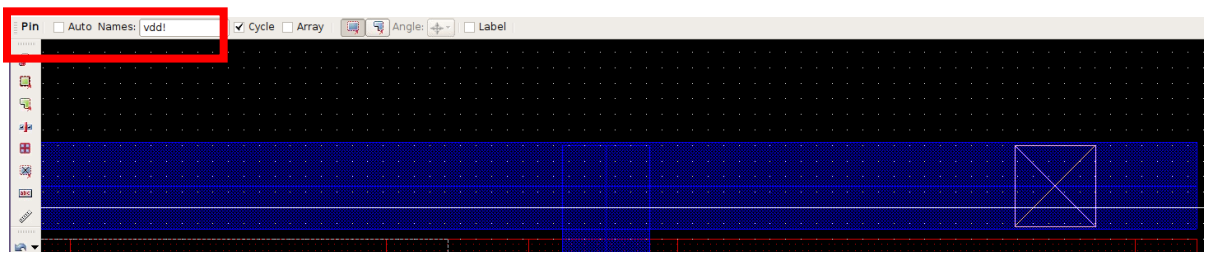


Floor Plan of Half Adder

- **Adding Terminals/Pins**: In order to clearly show input/output terminals when used in the hierarchy to build the next stages, it is important to also add Terminals. Follow this procedure to create them:
  a) It involves two steps. Creating a **Pin** and placing a **Label**
  b) **Pin:** Click Create → Pin → By Shape.



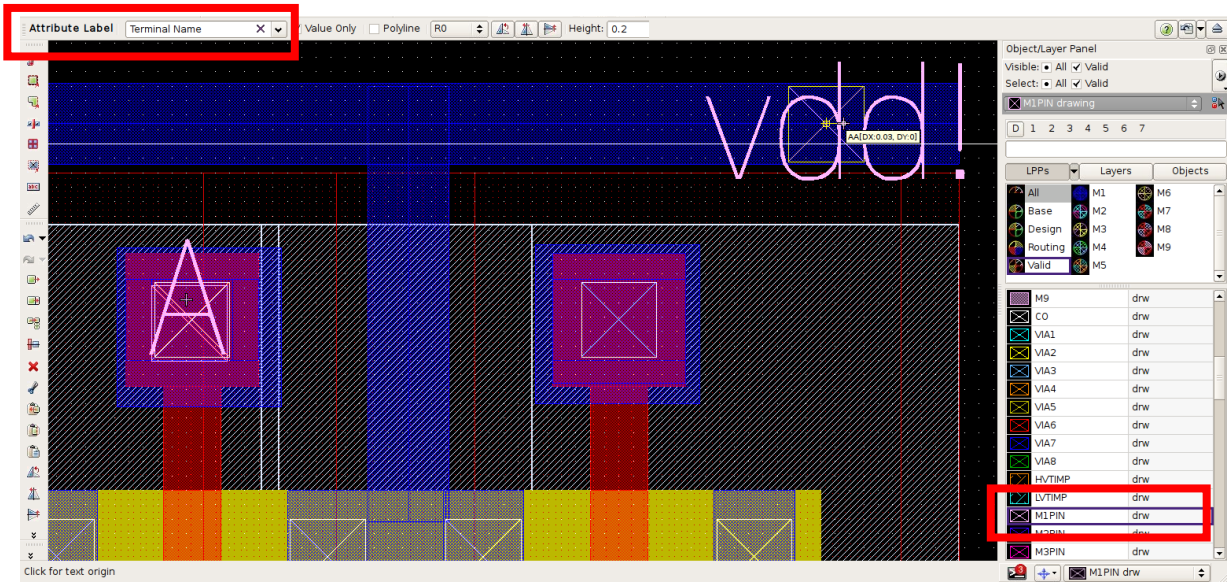
  c) Add the name of your pin, in this example we are creating the vdd! Pin. And then use the same M1 or M2 layer to draw a metal rectangle. Since vdd! is made of M1 layer, so use M1 layer as a metal and draw a rectangle.



  d) **Label:** Select Create → text → attribute label (keyboard shortcut shift+l).
  e) From the drop down menu select Terminal Name and select the metal rectangle you drew in step c.

f) The vdd! Label will show up, but will be in metal layer by default, before placing it, adjust the label to the proper metal pin. (M1pin/M2pin). As this is for vdd! made of M1 layer then use M1 Pin layer as a label.

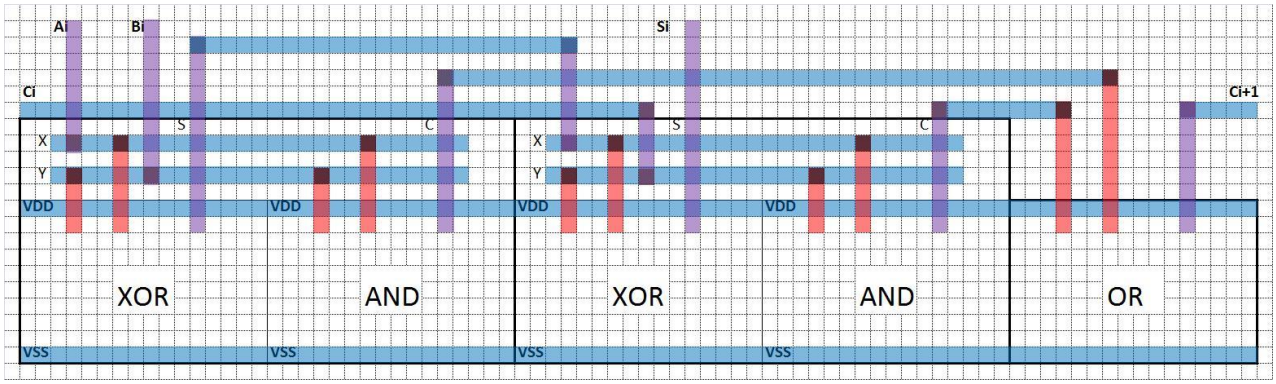
g) Place the label.



h) Repeat these steps for all your input/output pins

2. Full Adder

- Create the Full-adder cell as below, using the Half-adder and OR cell layouts.
- Note that you will need to add vdd! and gnd! Pins at each level of the hierarchy.
- Perform DRC and LVS on the full adder to make sure it is correct before moving to the next stage.



Floor Plan of Full Adder

3. Four-Bit Adder

- Create the 4-bit Adder cell, using the Full-adder cell layout. Figure out the floor plan by using schematics and above floor plans as reference.
- Design your layout to minimize mismatch in delay between the different inputs and outputs. It is best to utilize traces (metal lines) of equal length across the adder for your inputs and outputs. Having one input metal traces much shorter than others will cause their respective delays to be different and can potentially affect performance.

4. DRC and LVS

- Perform a Design Rules Check (DRC) as well as a Layout vs. Schematic (LVS) test for all the layouts.
- Adjust your layout if necessary to fix any errors.
- Refer to your tutorial as a reference for different steps. Also note that the tutorial includes a troubleshooting guide.

Question:

1) Why do we use M1 and M2?
2) What is the purpose of VIA12 in the layout?

III. REPORT

Write a short laboratory report that details all the work done. Describe the objective and procedures of this lab with your own words. The lab report should contain the following:

a) All schematics and layouts (every stage) in your lab.
b) Screenshots to show your design passes DRC and LVS at each stage
c) Answer any questions in the lab assignment.
d) Conclusions