SANTA CLARA UNIVERSITY	ELEN 153	Prepared by Vinay Krishna
Laboratory #3: CMOS Inverter Layout		

I. OBJECTIVES

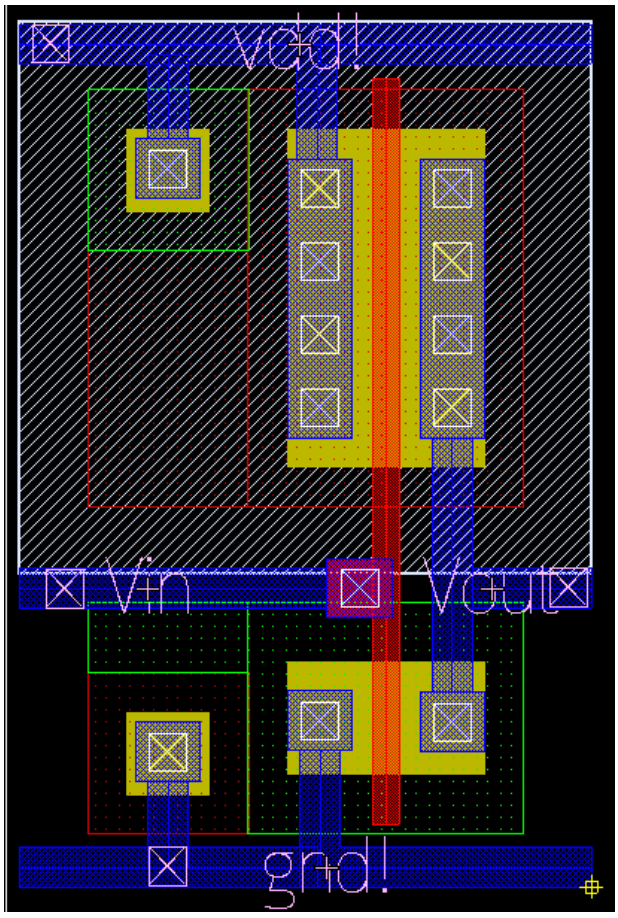
- To develop skills for CMOS layout using Synopsys Custom Compiler.
- To create an inverter layout and verify it using DRC and LVS.
- To perform parasitic extraction and post-layout simulations.

II. LAB PROCEDURE

1. Inverter Layout

In lab 2, an inverter schematic and symbol were created. In this lab assignment, we will create a layout for that same inverter.

- Re-open the tutorial library where you created the inverter schematic/symbol in the previous assignment.
- Follow the Synopsys Tutorial Part 2, pages 1-20 to complete the layout of the inverter.



Question:

1) For your lab report, include a table of all the layout layers along with contact layers you used, and their corresponding names in Synopsys tools (ex. Metal 1 : M1)

2) Mention the layer that provide PMOS & NMOS channel length and width dimensions. Looking at 2D image of the layout, mention the axis that determines Length and Width of the transistors. (ex. X-axis : _____)

2. DRC and LVS

To verify that the layout is correct, a Design Rules Check (DRC) must be performed to verify that the layout complies with design rules for this 90nm process. Furthermore, a Layout vs. Schematic (LVS) check must be performed to verify that layout you created actually matches the schematic of the desired inverter.

- Follow the Layout Verification section in your tutorial, pages 21-28 to perform DRC and LVS. Adjust your layout if necessary to fix any errors. The tutorial includes a troubleshooting guide.

3. LPE and Post-Layout Simulations

Layout Parasitic Extraction (LPE) extracts parasitic resistive and capacitive elements. These parasitics affect the performance of your design. A good layout attempts to minimize them. In this section, you will perform an LPE, and they you will incorporate these parasitics into your simulations, by performing a post-layout simulation and comparing the results to the pre-layout simulation.

- Follow the LPE and Post-layout simulation sections in your tutorial, pages 29-36.

III. REPORT

Write a short laboratory report that details all the work done. Describe the objective and procedures of this lab with your own words. The lab report should contain the following:

a) All schematics and layouts used in your lab.
b) Screenshots showing your design passed DRC and LVS
c) Screenshots for LPE.
d) Pre- and post-layout simulation waveforms.
e) Answer any questions in the lab assignment
f) Conclusions