SANTA CLARA UNIVERSITY	ELEN 153	Prepared by Vinay Krishna Andra
Laboratory #5: Hierarchy Design Part -1 Two-Input XNOR Layout		

I. OBJECTIVES

- To create a layout for the Two-input XNOR gate
- To perform DRC and LVS.

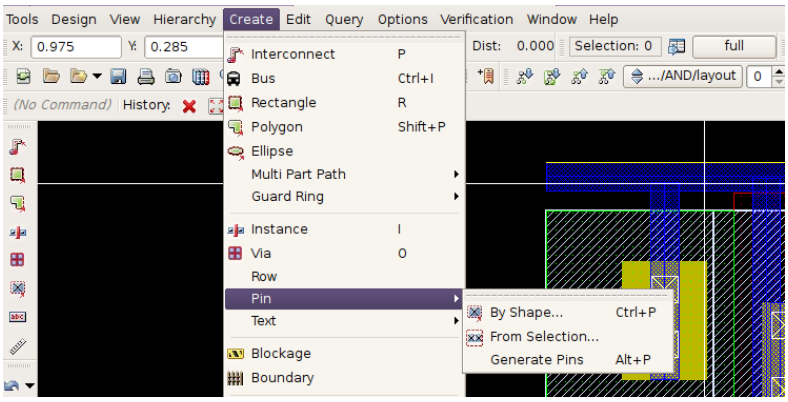
II. LAB PROCEDURE

1. XNOR layout Lab Flow

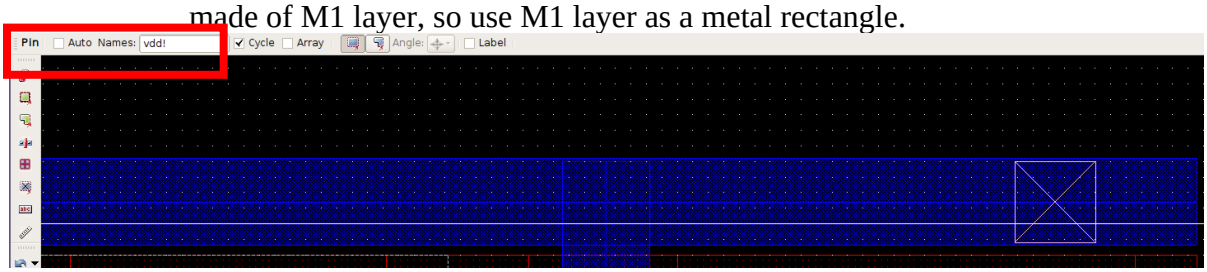
- As a part of Hierarchy design, this lab is divided into two parts.
  - **Part-1:** XNOR Logic (This has four Inputs i.e., A, Abar, B, Bbar)
  - **Part-2:** Four Inputs to Two Inputs using Two Inverters.
- This week ,you will build only XNOR Logic layout.

2. XNOR Logic Layout

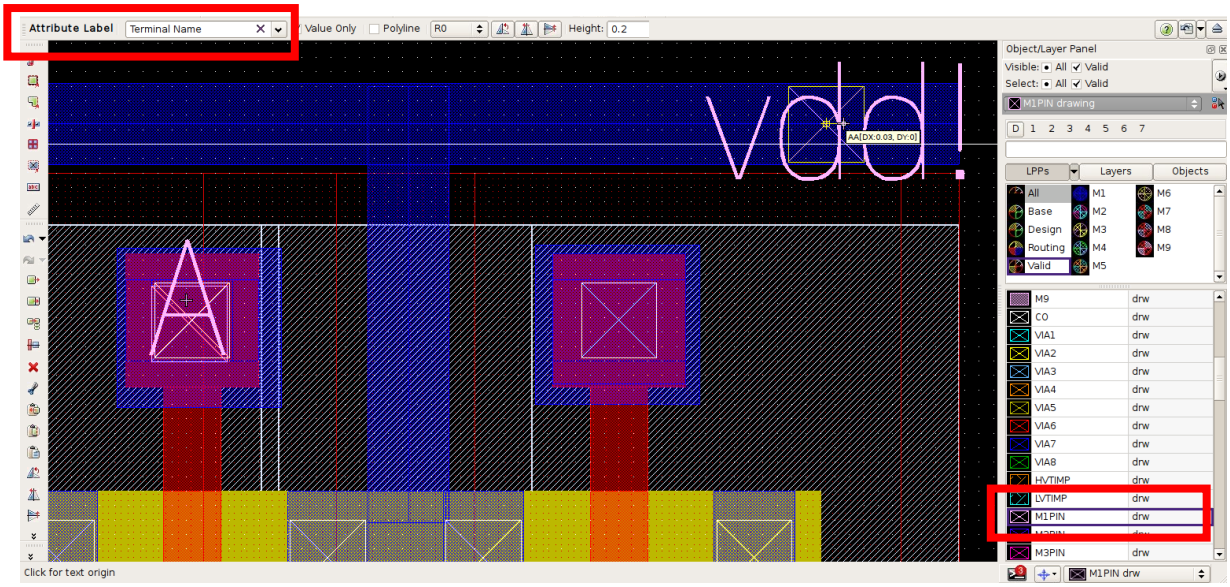
- Open the Library that you created last week for the XNOR Logic gate.
- Create a layout view for your XNOR Logic gate. Remember that your layout view should be within the same XNOR Logic cell that you created the schematic view in.
- Use the tutorial as a reference for different steps. Also, you may refer to the Design rules Excel sheet provided by your T.A.
- Creating Pins is different in hierarchy design.
- **Adding Terminals/Pins**: In order to clearly show input/output terminals when used in the hierarchy to build the next stages, it is important to also add Terminals. Follow this procedure to create them:
  a) It involves two steps. Creating a **Pin** and placing a **Label**
  b) **Pin:** Click Create → Pin → By Shape.



c) Add the name of your pin, in this example we are creating the vdd! Pin. And then use the same M1 or M2 layer to draw a metal rectangle. Since vdd! is made of M1 layer, so use M1 layer as a metal rectangle.



d) **Label:** Select Create → text → attribute label (keyboard shortcut shift+l).
e) From the drop down menu select Terminal Name, and select the metal rectangle you drew in step c.
f) The vdd! Label will show up, but will be in metal layer by default, before placing it, adjust the label to the proper metal pin. (M1pin/M2pin). As this is for vdd! made if M1 layer then use M1 Pin layer as a label.
g) Place the label.



h) Repeat these steps for all your input/output pins.

3. DRC and LVS

- Perform a Design Rules Check (DRC) as well as a Layout vs. Schematic (LVS) test
- Adjust your layout if necessary to fix any errors.
- Refer to your tutorial as a reference for different steps. Also note that the tutorial includes a troubleshooting guide.

Question: What can be done to reduce area and have improved performance?

III. REPORT

Write a short laboratory report that details all the work done. Describe the objective and procedures of this lab with your own words. The lab report should contain the following:

a) All schematics and layouts are used in your lab.
b) Screenshots showing your design passed DRC and LVS
c) Answer any questions in the lab assignment.
d) Conclusions