SANTA CLARA UNIVERSITY	ELEN 153	T.A. Vinay Krishna
Laboratory #7: Hierarchical Design Part 1– Four-Bit Adder		

I. OBJECTIVES

- To learn how to create complex circuits using bottom-up hierarchical design.
- To create a four-bit adder schematic and simulate it.

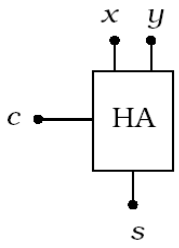
II. LAB PROCEDURE

1. Importing gates

- Download the Adder.zip from Camino
- Move the folder to your home page or directory where you create all your lab work and uncompress it.
- Use the "cd" command to change into that directory and launch Custom Compiler from inside directory. If done correctly, you should be able to see the Adder Library.
- To build you adder, use the given AND, XOR and OR gates given to you. These gates include schematics, symbols and layouts for you to utilize.

2. Half Adder

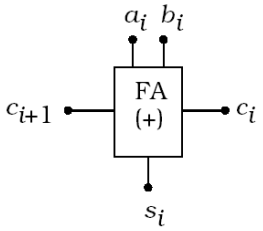
- Create a new library for the four-bit adder.
- Enter the Half-adder schematic, using AND, and XOR primitive cells. Create a symbol for the Half-adder.



x	y	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3. Full Adder

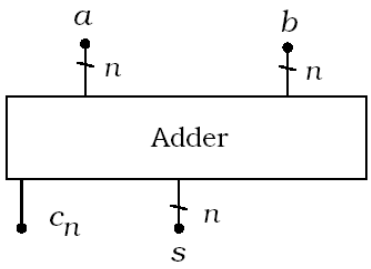
- Enter the hierarchical Full-adder schematic, using the Half-adder symbol, and OR primitive cell. Create a symbol for the Full-adder



a_i	b_i	c_i	s_i	c_{i+1}
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

4. Four-Bit Ripple Carry Adder

- Enter the hierarchical 4-bit Adder schematic, using the Full-adder symbol. Create a symbol for the 4-bit Adder.



5. Simulations

- Test the correctness of the 4-bit Adder schematic entered by using the A and B input vector pairs as suggested by TA. Use pattern source (Vpat) from analoglib.

Question:
How can you make an 8-bit adder using your 4-bit ripple carry adder?

III. REPORT

Write a short laboratory report that details all the work done. Describe the objective and procedures of this lab with your own words. The lab report should contain the following:

a) All schematics used in your lab.
b) SAE simulation setups
c) Simulation waveforms
d) Answer any questions in the lab assignment
e) Conclusions