SANTA CLARA UNIVERSITY	ELEN 153	Prepared by Vinay Krishna Andra
Laboratory #6: Hierarchy Design Part -2 Two-Input XNOR Layout		

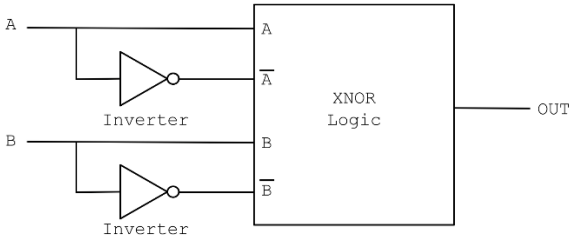
I. OBJECTIVES

- To create a layout for the Two-input XNOR gate
- To perform DRC and LVS.

II. LAB PROCEDURE

1. XNOR layout Lab Flow

- As a part of Hierarchy design, this lab is divided into two parts.
  - **Part-1:** XNOR Logic (This has four Inputs i.e., A, Abar, B, Bbar)
  - **Part-2:** Four Inputs to Two Inputs using Two Inverters.
- Last week ,you completed XNOR Logic layout.
- This week, you will use XNOR Logic Layout and connect two Inverters to create two input XNOR Gate as shown below.



Two - Input XNOR Gate

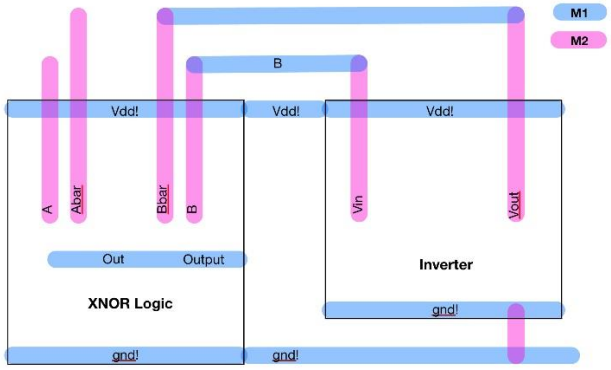
2. Initial Setup (Need to Replace Inverters)

- **Download:** Given Inverter file on Camino.
- Extract (unzip) the Inverter file into the file that contains the entire work of 153L.
- Open **lib.defs** file (this should be the same location as extracted file). A pop-up window prompts up and select “Display”. Now at the end of the code add the following line **DEFINE Inverter ./Inverter** then save the file and close it. Open the Tool or hit F5 key if the tool is already opened. You should be able to access the inverter file.
- This Inverter file contains schematic, symbol and layout compatible to build Two Input XNOR Gate.
- Open the Two Input XNOR schematic that has Inverters and now replace the old Inverters with the given new inverter and say **check & save**.
- You are ready to work on Two – Input XNOR

3. Two – Input XNOR gate Layout

- Open the Library that contains the Schematic of Two Input XNOR gate.
- Create a layout view for your Two Input XNOR gate. Remember that your layout view should be within the same cell that you created the schematic view in.

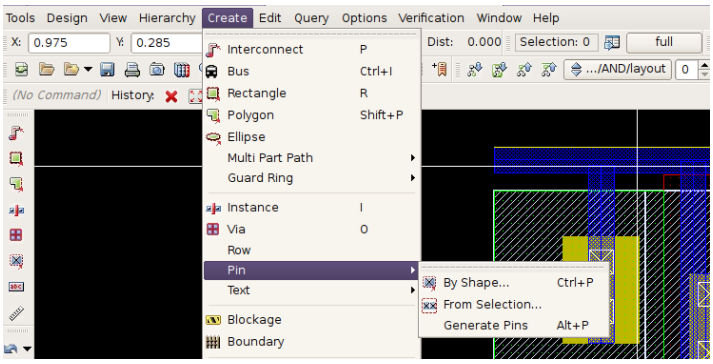
- Create the Two-Input XNOR layout as shown below, using XNOR Logic, and Inverter cells.
- To add the XNOR Logic and Inverter gate layout. Select Create→ instance, or press " i" for its keyboard shortcut. Then select the layout you desire and place it as shown below floor plan.



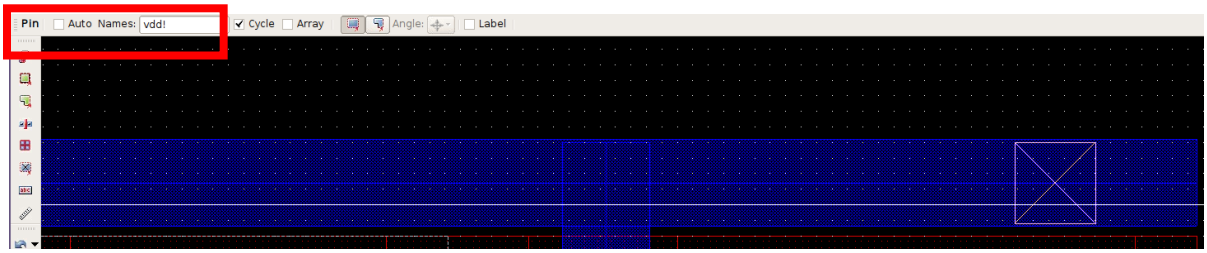
Floor Plan - XNOR Logic and Inverter

NOTE: Above floor plan is incomplete, and it is up to student to figure out the rest with the help of TA.

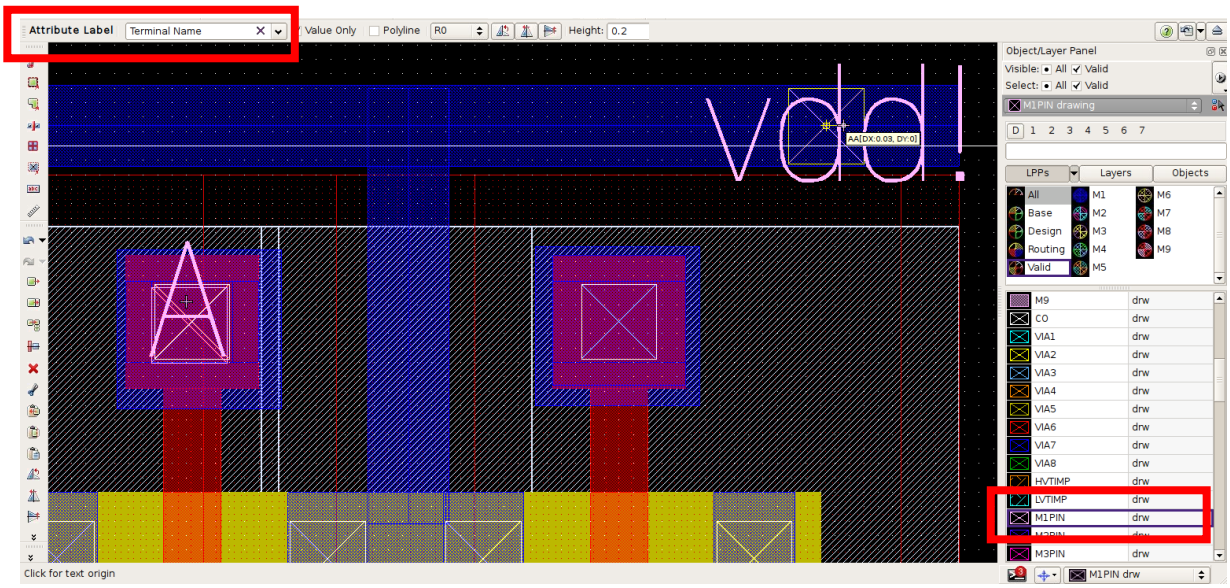
- Creating Pins is similar as in previous lab. If not familiar, then follow the steps below.
- **Adding Terminals/Pins**: In order to clearly show input/output terminals when used in the hierarchy to build the next stages, it is important to also add Terminals. Follow this procedure to create them:
    a) It involves two steps. Creating a **Pin** and placing a **Label**
    b) **Pin:** Click Create → Pin → By Shape.



c) Add the name of your pin, in this example we are creating the vdd! Pin. And then use the same M1 or M2 layer to draw a metal rectangle. Since vdd! is made of M1 layer, so use M1 layer as a metal and draw a rectangle.



d) **Label:** Select Create → text → attribute label (keyboard shortcut shift+l).
e) From the drop down menu select Terminal Name and select the metal rectangle you drew in step c.
f) The vdd! Label will show up, but will be in metal layer by default, before placing it, adjust the label to the proper metal pin. (M1pin/M2pin). As this is for vdd! made of M1 layer then use M1 Pin layer as a label.
g) Place the label.



h) Repeat these steps for all your input/output pins.

4. DRC and LVS

- Perform a Design Rules Check (DRC) as well as a Layout vs. Schematic (LVS) test
- Adjust your layout if necessary to fix any errors.
- Refer to your tutorial as a reference for different steps. Also note that the tutorial includes a troubleshooting guide.

III. REPORT

Write a short laboratory report that details all the work done. Describe the objective and procedures of this lab with your own words. The lab report should contain the following:

a) All schematics and layouts are used in your lab.
b) Screenshots showing your design passed DRC and LVS
c) Answer any questions in the lab assignment.
d) Conclusions