

Homework 4

Chapter 4

③ Given: 00110101 11001010

a) clear odd positions to zero

AND with 01010101 01010101

$$\begin{array}{r} 00110101 \\ 01010101 \\ \hline 00010101 \end{array}$$

b) set rightmost 4 bits to 1
OR with 00000000 1111

so:

$$\begin{array}{r} 00110101 \\ 01010101 \\ \hline 00010101 \end{array}$$

c) complement the most significant 8 bits

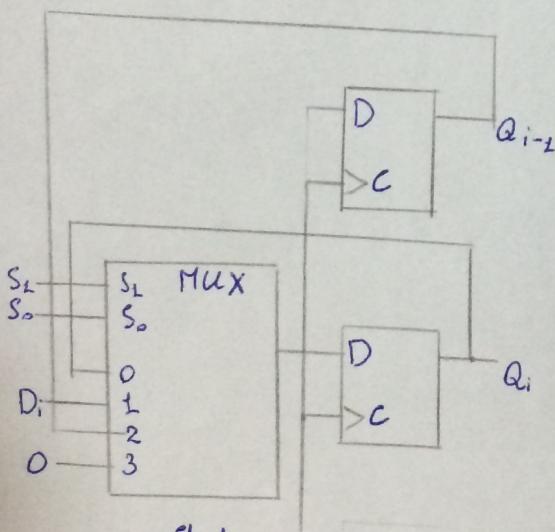
XOR with 11111111 00000000

④ 8 bit operand: 11001010

Shift left: 10010100

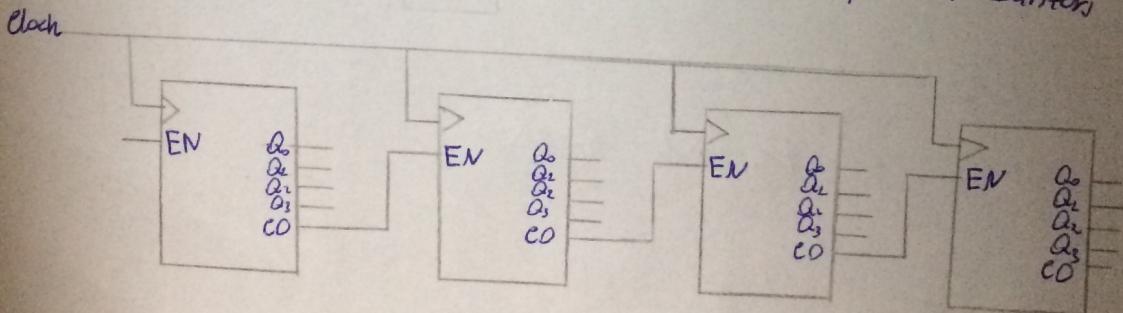
Shift right: 01100101

⑤



S ₁	S ₀	Register Operation
0	0	Load parallel data No change
0	1	Load parallel data
1	0	Shift down
1	1	Clear register to 0

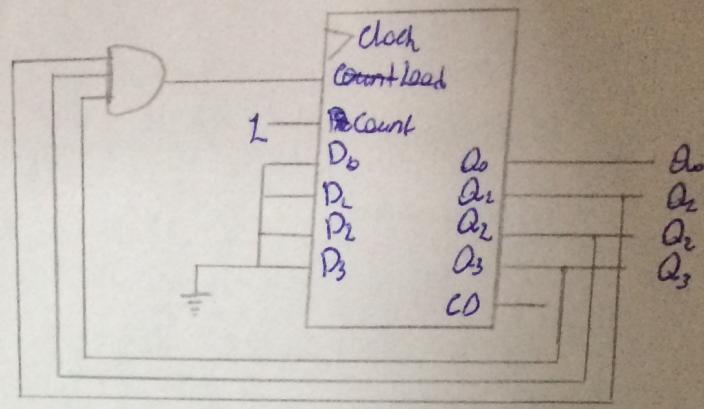
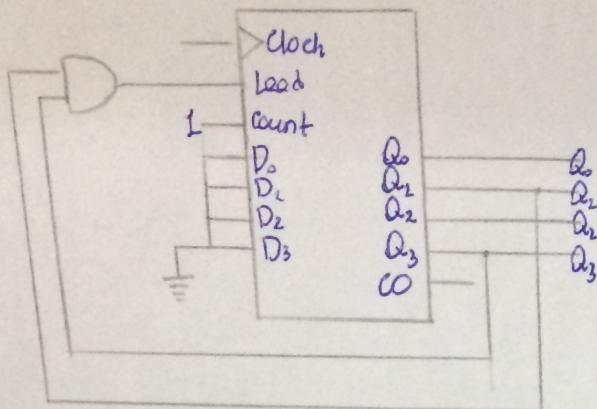
⑩ 16-bit serial-parallel counter using four 4-bit parallel counters



Maximum # of AND gates - 4

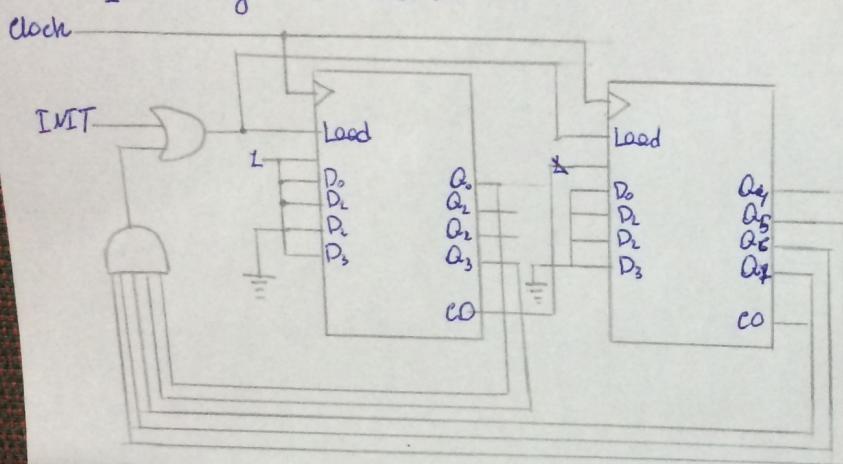
11) Using the synchronous binary counter and AND gate

a) Counter 0000 through 1010 b) Counter 0000 through 1110



12) Binary counter that counts from decimal 11 through 233

In binary: 233: 11101001 where the order is $Q_2Q_6Q_5Q_4Q_3Q_2Q_1Q_0$



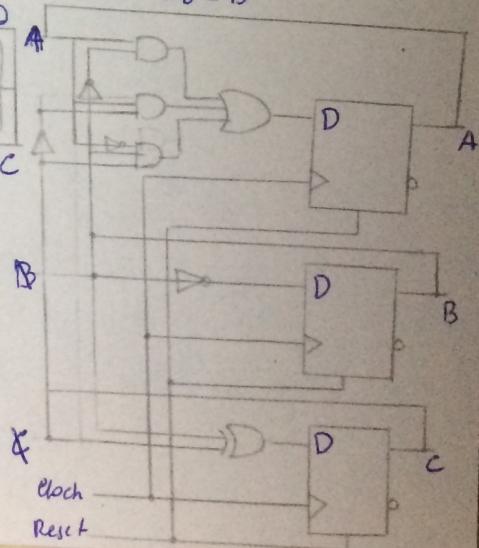
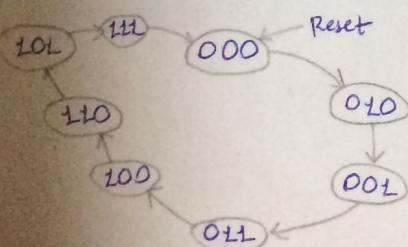
13) Counter with the repeated sequence: 0, 2, 1, 3, 4, 5, 5, 7

Present State			Next State		
A	B	C	D _A	D _B	D _C
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	0	0	0

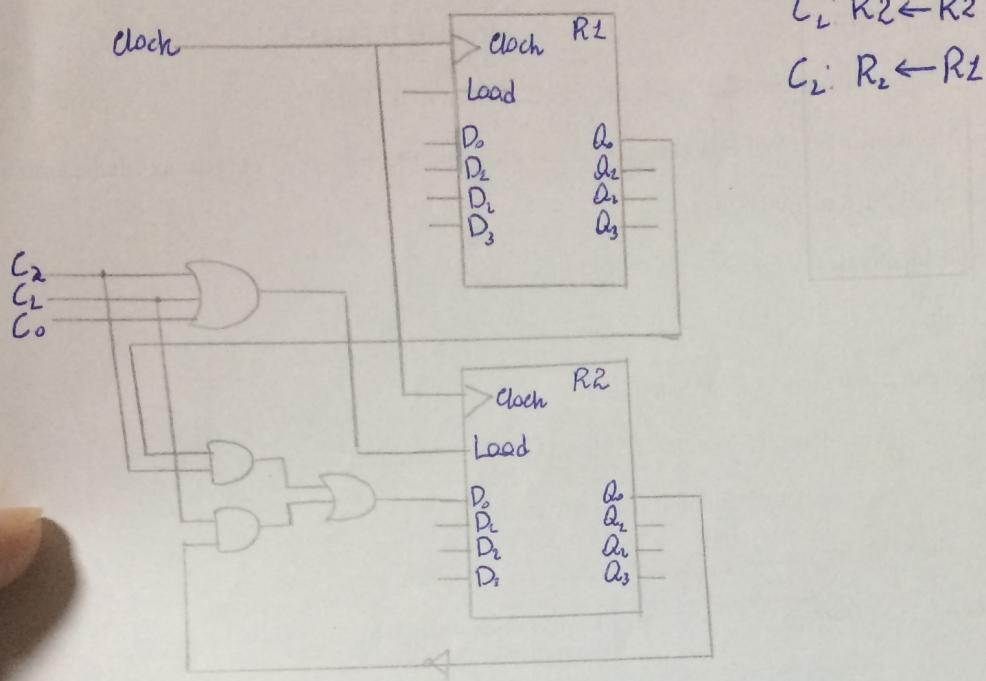
A	BC		00	01	10	11
			0	1	1	*
0	0	0	1	1	*	1
0	0	1	1	1	*	1
0	1	0	1	1	*	1
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	0	1	1
1	1	1	0	0	0	0

$D_A = A\bar{B} + A\bar{C} + \bar{A}\bar{B}\bar{C}$
 $D_B = \bar{B}$
 $D_C = \bar{B}C + B\bar{C} = B \oplus C$

A	BC		00	01	10	11
			0	1	1	*
0	0	0	1	1	1	1
0	0	1	1	1	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	1	1	1	1



⑯ 2 4-bit registers R_1 and R_2



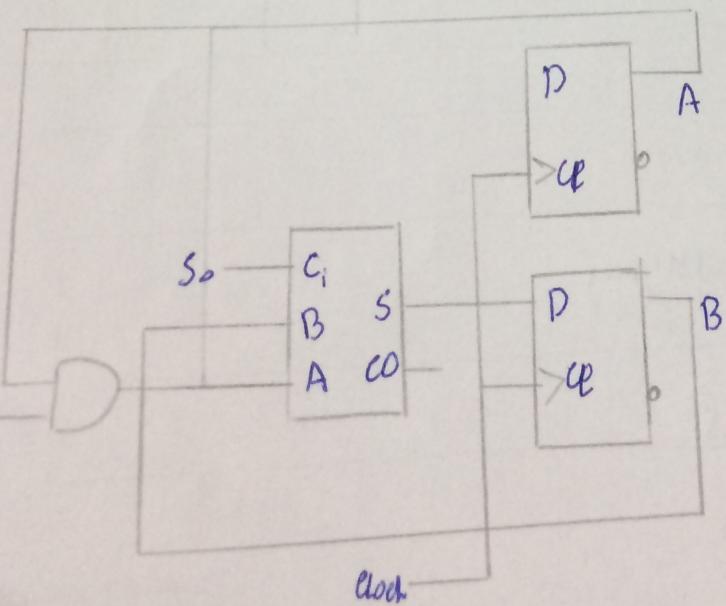
$$C_0: R_2 \leftarrow 0$$

$$C_L: R_2 \leftarrow \overline{R_2}$$

$$C_2: R_2 \leftarrow R_1$$

⑰ A register cell for register B: $S_L: B \leftarrow B+A$
 $S_0: B \leftarrow B+1$

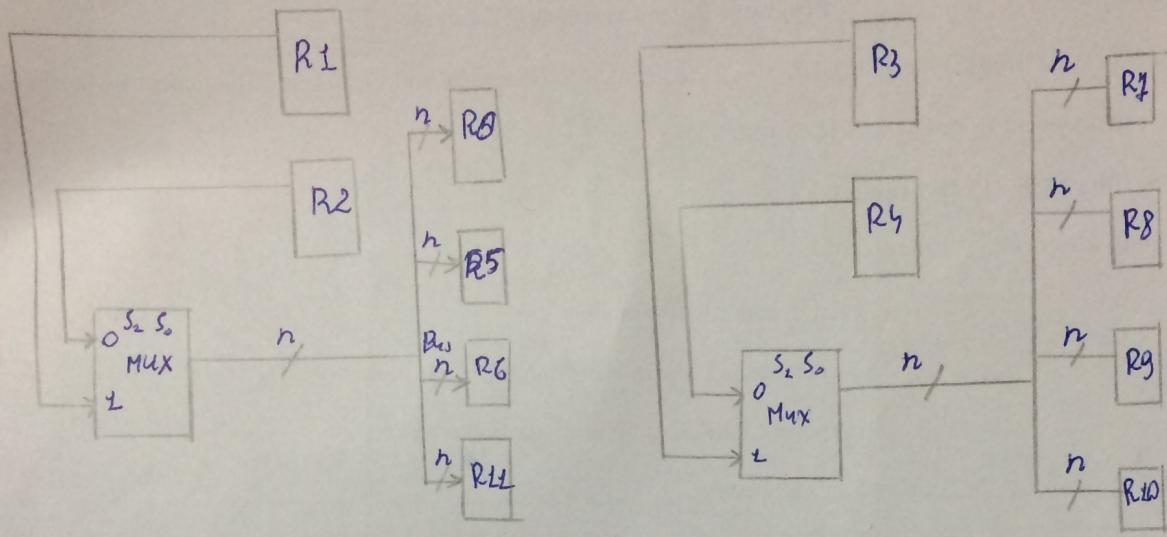
B_i	A_i	C_i	B_{i+1}	C_{i+1}	S_o	B_i	$C(B_{i+1})$	B_{i+1}	C_{i+2}	B_i	B_{i+2}	C_{i+2}
0	0	0	0	0	1	0	D	0	0	0	1	0
0	0	1	1	0	1	0	L	0	0	1	0	1
0	0	1	0	0	1	1	0	L	0	1	0	1
0	1	1	D	L	1	1	L	L	L	1	0	1
1	0	0	L	0	1	1	1	L	L	1	0	1
L	0	1	0	L	1	1	1	0	L	1	0	1
L	1	0	0	L	1	1	0	L	0	1	0	1
L	1	1	L	L	1	1	0	0	L	1	1	1



$$\begin{array}{ll}
 \textcircled{28} \quad R_0 \leftarrow R_2 & R_8 \leftarrow R_3 \\
 R_5 \leftarrow R_1 & R_9 \leftarrow R_5 \\
 R_6 \leftarrow R_2 & R_{10} \leftarrow R_4 \\
 R_7 \leftarrow R_3 & R_{11} \leftarrow R_2
 \end{array}$$

g) At most 2 clock cycles
2 buses

b)



\(\textcircled{34} \) State machine: clock CK

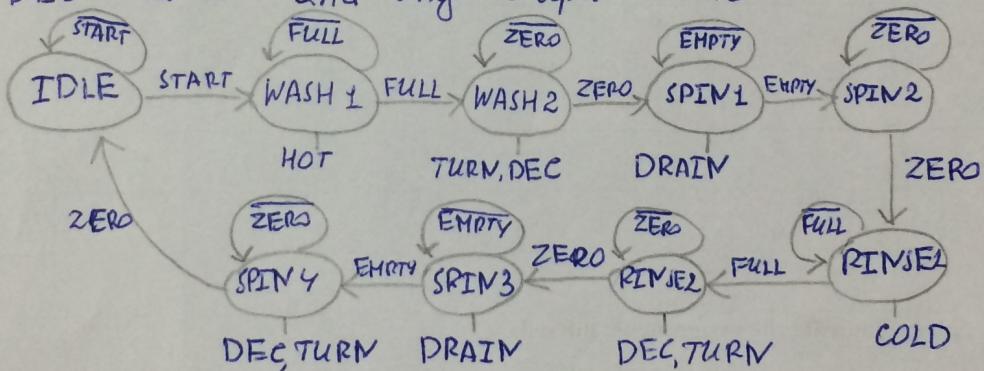
3 external inputs: START, FULL, EMPTY

External outputs: HOT, COLD, DRAIN, TURN

Data path for the control: down counter which has 3 inputs

RESET, DEC and LOAD and single output: ZERO

a)



b) 2 more inputs: PAUSE and STOP

~~Two more states~~ For PAUSE add a FLIP-FLOP set by START and reset by PAUSE. OR flip-flop complemented with each input in the loop and AND it with each input on transition.

For STOP a new state: $\overline{\text{STOP}}$ is ANDED with all input conditions. Each state transitions to state STOP if STOP is 1.

