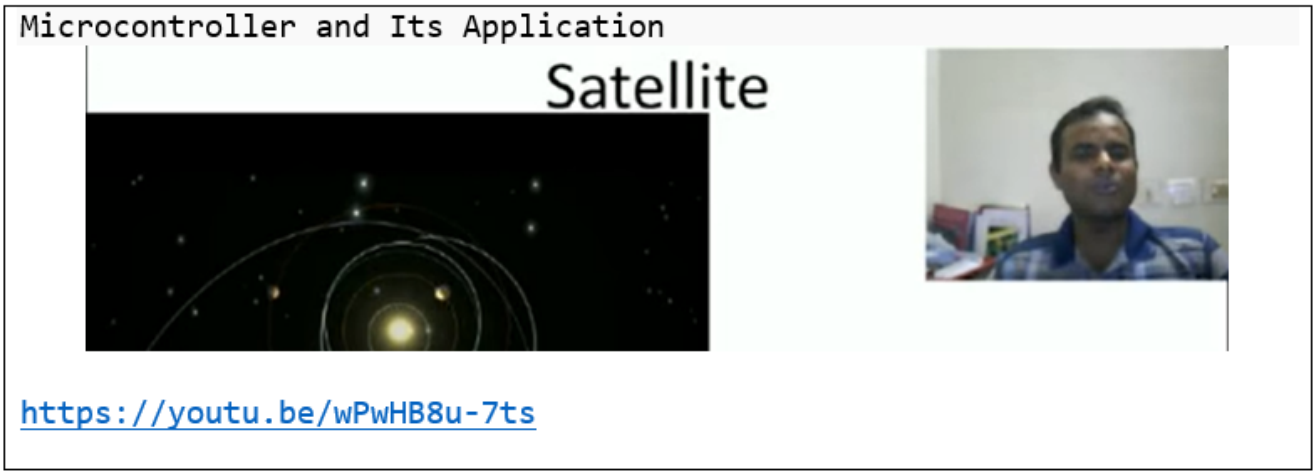
No E-Mail submissions will be accepted.
Submission formats and file naming:
File name : Pts_irstName_lastName_lab_8
File format: pdf or MS Word format
e.g. Pts_Donald_Trump_lab_8.pdf

Reading materials

Use the following link and write a one page summary about the movie.



1) A list of cache replacement algorithms is given below. Choose one of the algorithms and write a summary about that.

1 – Least Recently Used (LRU)
2 – First In First Out (FIFO)
3 – Least Frequently Used (LFU)
4 – Random
5 – Clock algorithm

2) Suppose that a CPU has a level 1 cache, a level 2 cache, and a level 3 cache with access times of 1 nsec, 3 nsec, and 5 nsec, respectively. The main memory access time is 15 nsec. If 35% of the accesses are level 1 cache hits, 25% are level 2 cache hits, 15% are level 3 cache hits, and the main memory access time is 15 nsec. What is the average access time? What is cache hit and miss rate?

average access time = 0.35*1 + 0.25*3 + 0.15*5 + 0.25*15 = 5.6 nsec
cache hit rate = 35% + 25% + 15% = 75%
cache miss rate = 100 - 75% = 25%

3) Direct mapping. A list of memory requests by CPU is given below.

a) Determine cache memory hit or miss for each case.
b) Obtain the updated version of the cache memory.
c) Calculate hit and miss rate.

0	0000	00	01	10	11	M0
1	0001	00	01	10	11	M1
2	0010	00	01	10	11	M2
3	0011	00	01	10	11	M3
4	0100	00	01	10	11	M4
5	0101	00	01	10	11	M5
6	0110	00	01	10	11	M6
7	0111	00	01	10	11	M7
8	1000	00	01	10	11	M8
9	1001	00	01	10	11	M9
10	1010	00	01	10	11	M10
11	1011	00	01	10	11	M11
12	1100	00	01	10	11	M12
13	1101	00	01	10	11	M13
14	1110	00	01	10	11	M14
15	1111	00	01	10	11	M15

	Valid	Tag	Data
00	1	10	M8
01	0	00	M1
10	1	01	M6
11	0	11	M15

Memory requests	Hit(1)/Miss(0)	Data[offset]
000000	0	M0[00]
011001	1	M6[01]
111100	0	M15[00]
000111	0	M1[11]
110000	0	M12[00]
010101	0	M5[01]
011110	0	M7[10]

Updated cache table

	Valid	Tag	Data
00	1	11	M12
01	1	01	M5
10	1	01	M6
11	1	01	M7

Hit rate = 1/7
Miss rate = 6/7

4) What is the difference between data cache and instruction cache?

Instructions are only fetched from memory (read), but data can be read from or written to memory.

5) Assuming that the number of cache lines is equal to 100 and 4 way set-associative mapping is employed:

a) Determine the number of cache sets 100/4 = 25

b) Obtain the cache set numbers for the given memory addresses (complete the following table).

Memory address(MI)	Cache set number
100	0
250	0
131	6
23	23