

Show all your work to get any marks; no work = no marks!

Hand-write with pen and paper, then upload images or a PDF file of the exam before 9:30 PM.

Print and fill out the attached exam, with pen and paper. If you do not have a printer, just hand-write your answers with pen and paper instead. Upload a PDF file of your final exam submission; answer questions in order. Show ALL your work for every question. If you have questions, email Jason_Wilder@bcit.ca

Full Name: Muhammed Asad Mushtaq

Signature: Asad

Student Number: A01066352

Score: 18³/₄ out of 21

1. a) Consider a multilevel computer in which all the levels are different. Each level has instructions that are 4 times as powerful as those of the level below it; that is, one level m instruction can do the work of 4 level $m-1$ instructions. If a level-6 program requires 2 attoseconds to run, how long would equivalent programs take at levels 1 and 19, assuming 3 level m instructions are required to interpret a single $m+1$ instruction? (2 marks)

b) Also, what is wrong in that question? Explain. (1 mark) $C \neq 4, n = 3$

a)

$$\text{level 6} = 2 \text{ attoseconds}$$

$$\text{level 19} = K \times \frac{n^{13}}{C^{13}} \text{ seconds} = \frac{2n^{13}}{C^{13}} = \frac{2(3^{13})}{4^{13}} \text{ attos}$$

$$\text{level 1} = K \times \frac{C^5}{n^5} = \frac{2(4^5)}{3^5} \text{ attos. } (1!)$$

C = number of LLL instructions it takes to replace one HLL instructions
 n = number of interpreter interpretations to one HLL instruction into C LLL instructions

b) N should be greater than C because we want $\frac{n}{C}$ to be higher than 1. (1)

2. Fill in the rows of this table: (1 mark) $\text{Period} = \frac{1}{\text{frequency}}$

| | Frequency | Corresponding period |
|---|---|---|
| a | 25kHz = 25000 Hz | $\frac{1}{25000} = 0.00004s = 0.04ms$ |
| b | $\frac{1}{2 \times 10^{-8}} = 5 \times 10^7 = 50 \text{ MHz}$ | 20 nanoseconds = $2 \times 10^{-8}s$ |
| c | 125Hz | $\frac{1}{125} = 0.008s = 8ms$ |
| d | $\frac{1}{3.33333 \times 10^{-5}} = 3 \times 10^4 = 30 \text{ kHz}$ | 33.3333 microseconds = 3.33333×10^{-5} |

3. Consider a pipeline whose stages take 14 nanoseconds, 16000 femtoseconds, 0.00003 milliseconds, and 0.15 microseconds. What are a) its latency and b) its bandwidth? (2 marks)

a) Latency:

$$\begin{aligned} 14ns &= 14ns & + \\ 16000 \text{ femtoseconds} &= 0.016ns & + \\ 0.00003 \text{ milliseconds} &= 30ns & + \\ 0.15 \text{ microseconds} &= 150ns & \\ \hline &= 194.016ns \end{aligned}$$

Thus, latency is equal to

$$194.016ns / \text{unit}$$

or

$$194.016ns / \text{instruction}$$

b) Bandwidth:

$$1 \text{ unit} / \text{slowest}$$

Thus, bandwidth is equal to

$$1 \text{ unit} / 150ns$$

or

$$1 \text{ instruction} / 150ns$$

4. a) What is the Hamming Distance of a code whose words are 00000011, 10101010, 00001111, and 11110000?

The closest two words include 00000011 and 00001111.

The hamming distance is equal to 2 bits.

- b) How many errors can it correct? c) What are the properties of a good error-correcting code? Why are these good properties? Explain clearly. (2 marks)

b) Error correcting ability is $\leq t/2$. Thus, it can correct 0 bits or not able to correct any bits or errors.

c) Properties of good error-correcting code include having a large hamming distance because a larger amount of errors can be successfully detected and corrected. how!

5. The following Hamming codeword was made using even parity. 1101101. a) Was there an error? b) Where? c) What was the original dataword supposed to have been? d) Explain the limitations of Hamming code in this question. Under what circumstances might Hamming code have failed here? (2 marks)

| | | | | | | |
|-----|-----|---|-----|---|---|---|
| 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 2 | 2 | 4 | 4 | 4 | 4 |
| (P) | (P) | 1 | (P) | 1 | 2 | 2 |
| X | | | X | | | |

a) Yes, there is an error.

b) Error is at the $1 + 4 = 5$ th bit

c) Original dataword was supposed to be 0001

d)

6. Create the odd-parity Hamming codeword for the dataword 010110111. Clearly identify parity bits. (1 mark)

| | | | | | | | | | | | | |
|-----|-----|---|-----|---|---|---|-----|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 2 | 2 | 4 | 4 | 4 | 4 | 8 | 8 | 8 | 8 | 8 | 8 |
| (P) | (P) | 1 | (P) | 1 | 2 | 2 | (P) | 1 | 2 | 4 | 4 | 1 |

Codeword = 0101101110111

_____ { 3 } _____

7. What is the mean memory access time for a system with four levels of cache and a main memory. The access times for these respectively are 2ns, 5ns, 10ns, 20ns, and 1 microsecond. 650 memory accesses were made. 400 hits were in level 1; 100 in level 2; 80 in level 3; 50 in level 4; the rest were in main memory. (2 marks)

Access times [L₁: 2ns, L₂: 5ns, L₃: 10ns, L₄: 20ns, MM: 1000 ns]

$$\begin{aligned} \text{Total Time} &= (650 \times 2\text{ns}) + (250 \times 5\text{ns}) + (150 \times 10\text{ns}) + (70 \times 20\text{ns}) + (20 \times 1000\text{ns}) \\ &= 1300\text{ns} + 1250\text{ns} + 1500\text{ns} + 1400\text{ns} + 20000\text{ns} \\ &= 25450\text{ns} \end{aligned}$$

$$\text{MMAT} = \frac{\text{Total time}}{\text{Total \# of requests}} = \frac{25450\text{ns}}{650} = 39.15\text{ns/request}$$

Thus, MMAT is 39.15 ns/request for this system.

8. How long does it take to read a disk with 4000 cylinders, each containing seven tracks of 256 sectors? First, all the sectors of track 0 are to be read starting at sector 0, then all the sectors of track 1 starting at sector 0, and so on. The rotation rate is 1200 RPM, and a seek takes 4 msec between adjacent cylinders and 40 msec for the worst case. Switching between tracks of a cylinder can be done in 13 msec. (2 marks)

1200 RPM (60sec/min) → 20 RPS → 1/20th sec per revolution → 50 ms per revolution

1) Move A/W head to track 0 = worst case seek time = 40 ms

2) Wait for sector 0 to spin to R/W head = 50 ms / 2 = 25 ms (avg. case)

3) Read the current track = 50 ms

4) switch platter = 13 ms, wait for sector 0 = 37 ms, read platter 2 track = 50 ms

5) switch to platter 3 = 13 ms, wait for sector 0 = 37 ms, read platter 3 track = 50 ms

6) " " 4 " " " " " " 4 " " "

7) " " 5 " " " " " " 5 " " "

8) " " 6 " " " " " " 6 " " "

9) " " 7 " " " " " " 7 " " "

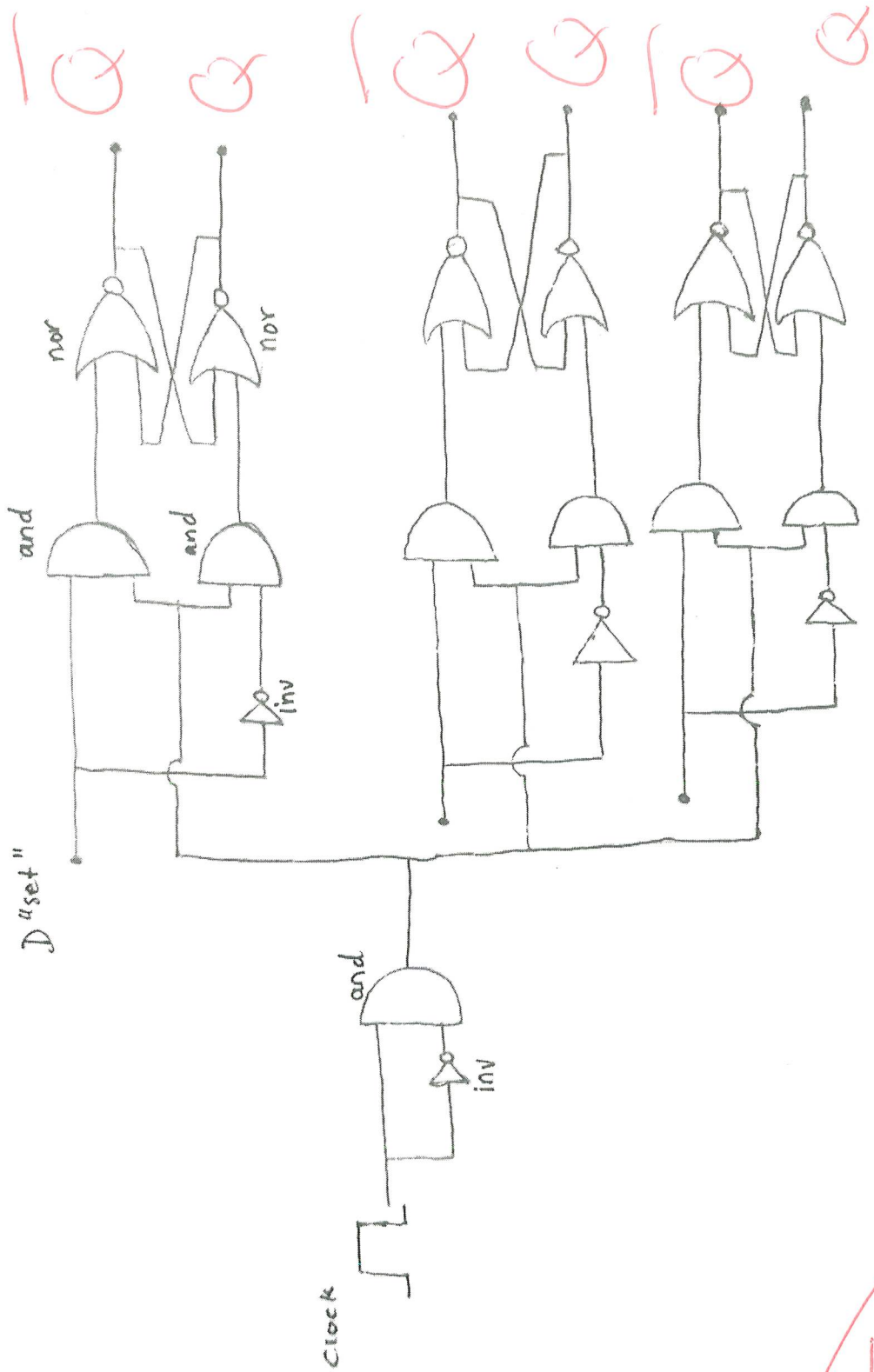
10) switch to platter 1 = 13 msec, move to adjacent cylinder = 4 ms, wait for sector 0 = 37 ms

Repeat steps 3 to 10 3,999 times

$$40 + 25 + 4000(50 + 13 + 100 + 100 + 100 + 100 + 50) = 65 + 4000(700) = 2,800,065\text{ms} = \boxed{2800\text{ seconds}}$$

9. Draw a full 3-bit register (i.e. three D-flip flops together). Label the gates. (2 marks)

See Below



10. Imagine you are tasked with designing a control system for the smart lighting in a home. The system has four lights (L1, L2, L3, L4) and is controlled by three inputs: Time of Day (T), Presence of People (P), and Special Mode (S).

Time of Day (T): This input has two states, Day (0) and Night (1).

Presence of People (P): This input detects if people are present (1) or not (0).

Special Mode (S): This input indicates whether a special mode is activated (1) or not (0). Special mode could be anything like a party mode or an energy-saving mode.

The lights in the home must operate under the following conditions:

During the Day ($T=0$): Only L2 should be on if people are present ($P=1$), regardless of the Special Mode (S).

During the Night ($T=1$) and No Special Mode ($S=0$): L1 and L3 should be on if people are present ($P=1$); otherwise, all lights should be off.

During the Night ($T=1$) and Special Mode ($S=1$): L4 should be on, and L1 should also be on if people are present ($P=1$), regardless of their presence for L4.

Your task is to:

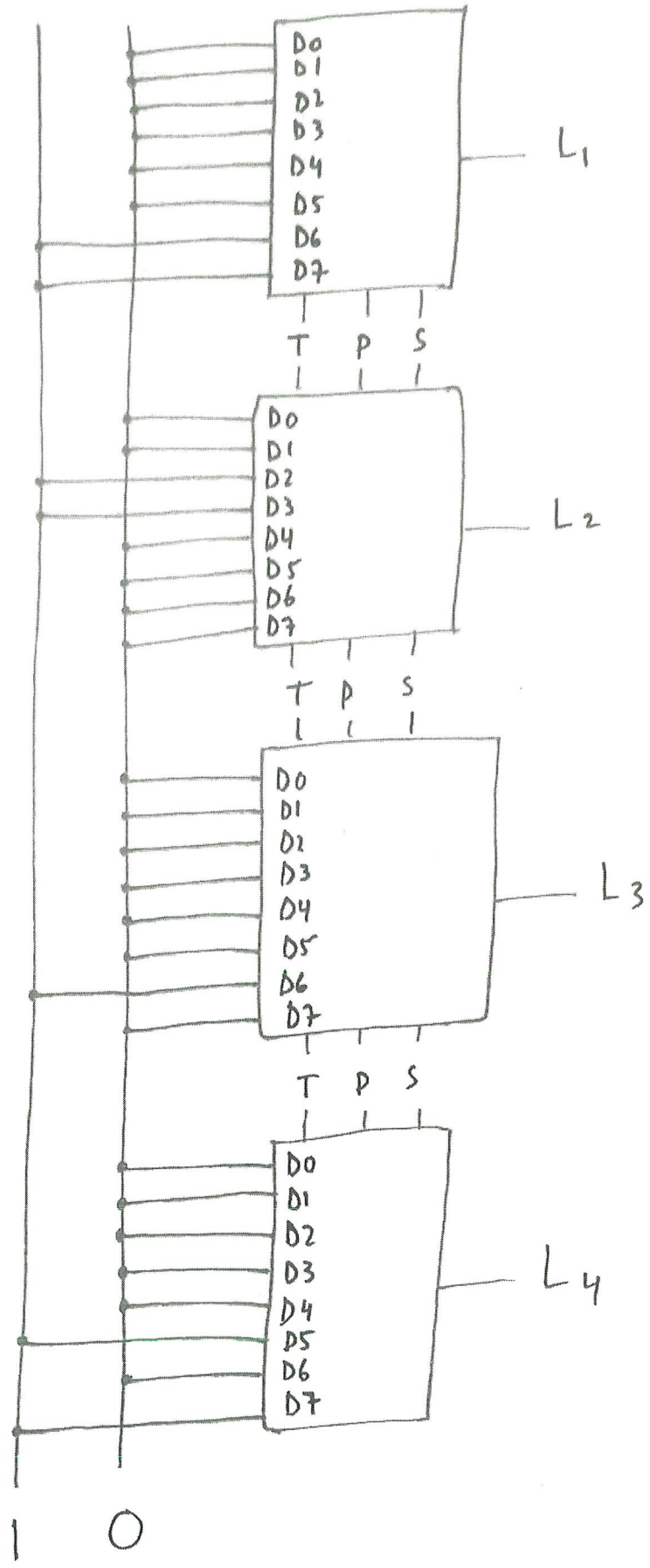
- Develop a truth table that for the logic to turn each light on or off based on the inputs T, P, and S. (1 mark)
- Design a set of multiplexers that implement this logic for controlling the lights. (1 mark)

a)

| | T | P | S | L ₁ | L ₂ | L ₃ | L ₄ |
|----|---|---|---|----------------|----------------|----------------|----------------|
| D0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| D2 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| D3 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| D4 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| D5 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| D6 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| D7 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

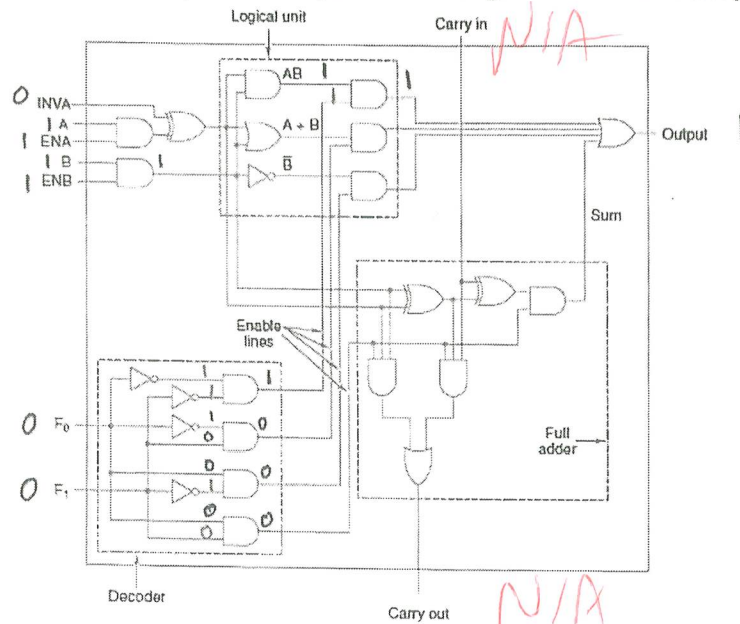
b) See Below

2)



✓

11. Fill in all the inputs and outputs for this diagram. The circuit must perform the operation "1 and 1": (1 mark)



12. Fill in all the inputs and outputs for this diagram to perform the operation "write 000 to word 2": (1 mark)

