# Quiz 5: do it yourself; use the course notes - Res...

## Attempt 1 of 1

Written Jun 21, 2024 8:54 PM - Jun 21, 2024 9:29 PM

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| Attempt Score | 7 / 7 - 100 % |
| Overall Grade (Highest Attempt) | 7 / 7 - 100 % |

### Question 1 — 2 / 2 points

Explain in plain English what the timing diagram we covered last week MEANS. What story is it telling? Tell everything you know, in your own words.

The timing diagram we covered last week involved a synchronous bus diagram.

It was a story of deadlines as the components inside the diagram were dependant on a clock. The components included 3 control lines, 2 buses, and 1 clock. Control lines included memory request, read and wait. Meanwhile the buses included the address bus and data bus.

The whole process started with the CPU sending a memory address fetch request to main memory through the address bus and then after a small delay it sent a read instruction.

The memory instructs the CPU to wait until the memory can catch up. Then once it catches up, it tells the CPU that the requested word from the memory address is ready and available on the data bus.

The CPU then was then able to read the fetched word on the data bus into the register, at falling edge of the next clock cycle.

The timing diagram was dependant on the falling or rising edges of the clock, and illustrated how the CPU fetches the word from the main memory; through a series of well defined deadlines and steps, where each step had corresponding time values for completion. For example, Tad, Tds, Tml, Tm etc.

**The correct answer is not displayed for Written Response type questions.**

## Question 2 — 2 / 2 points

How long does memory have to produce a word from when the address is stable with a 25MHz bus, Tad = 2ns, Tds = 3ns, Tm = 4ns, Tml = 5ns. There are two wait states. Show your work.

25MHz corresponds to 40ns per cycle.

Fastest possible is 1.5 cycles

Total cycles = 1.5 cycles + 2 wait state cycles = 3.5 cycles

Total cycle time = 3.5 cycles * 40ns = 140ns

Max time available to memory = 3.5 cycles - Tad - Tds = 140ns - 2ns - 3ns = 135ns

The memory has 135ns to fetch the word from when the address becomes stable.

**The correct answer is not displayed for Written Response type questions.**

## Question 3 — 3 / 3 points

How long does memory have to produce a word from when the memory request is asserted with a **20MHz** bus, Tad = 2ns, Tds = 3ns, Tm = 4ns, Tml = 5ns. There is one wait state. Show your work.

20 MHz corresponds to 50ns per cycle.

We must solve this problem by using Tm and then Tml, and then pick the worst case as the answer.

Using Tm = 1 cycle (fastest) + 1 wait state – Tds – Tm
= 2 cycles * (50 ns/cycle) – Tds – Tm
= 100ns – 3ns – 4ns = 93ns

Using Tml = 1.5 cycle (fastest) + 1 wait state – Tad – Tds – Tml
= 2.5 cycles * (50 ns/cycle) – Tad – Tds – Tml
= 125ns – 2ns – 3ns – 5ns = 115ns

The answer is worst case -> 93ns

**The correct answer is not displayed for Written Response type questions.**

Done