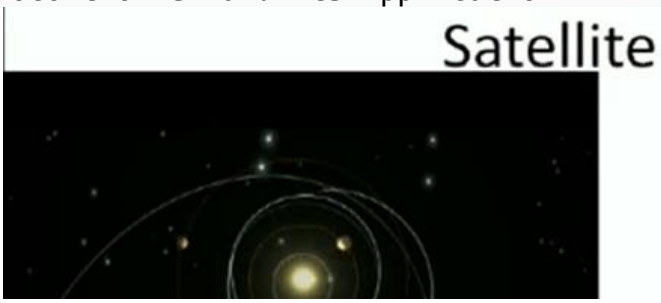
No E-Mail submissions will be accepted.
Submission formats and file naming:
File name : firstName_lastName_lab_8
File format: pdf or MS Word format
e.g. Donald_Trump_lab_8.pdf

Reading materials

Use the following link and write a one page summary about the movie.

Microcontroller and Its Application



https://youtu.be/wPwHB8u-7ts

This video discusses the differences between microcontroller and microprocessors and their implications in day to day life. Both microcontroller and microprocessors are programmable, but processes things in different ways. Microprocessors process a lot filters to support their information. Microcontroller can process things to a degree but unlike microprocessors, microcontrollers can stand alone as an application

Microprocessors contain things like ALU, accumulator, registers etc. But a microcontroller on the other hand has things like internal RAM ROM, I/O ports and more. This gives microcontrollers the advantage in small scale applications.

There's many manufacturers that create microcontrollers. Many of these microcontrollers are used in things like smart devices, remote controllers, sink sensors, home appliances, washing machines, smartphones and many more.

Cars contain many microcontrollers for things like wipers, AC, steering, ABS, windows, etc. And increasing as more and more cars become electric. Even satellites use microcontrollers.

The video then goes on to mention many more examples of microcontrollers like cameras, auxiliary systems, motorcycles etc. Explaining it's harder to find something electric that doesn't have a microcontroller than it is to find one that does.

1) A list of cache replacement algorithms is given below. Choose one of the algorithms and write a summary about that.

1 – Least Recently Used (LRU)

In least recently used, the algorithm removes the least recently used or accessed memory. This happens when the cache is full and memory that needs to be accessed is not found in the cache. It works under the idea that recently used memory is more likely to be used again, so older unused data is replaced/. For example, a cache has 3 slots and loads data in the the order A, B, C, A, D. Here B is removed because the recent order of retrieval was D, A, C.

2 – First In First Out (FIFO)
3 – Least Frequently Used (LFU)
4 – Random
5 – Clock algorithm

2) Suppose that a CPU has a level 1 cache, a level 2 cache, and a level 3 cache with access times of 1 nsec, 3 nsec, and 5 nsec, respectively. The main memory access time is 15 nsec. If 35% of the accesses are level 1 cache hits, 25% are level 2 cache hits, 15% are level 3 cache hits, and the main memory access time is 15 nsec. What is the average access time? What is cache hit and miss rate?

L1 = 1ns, 35%
L2 = 3ns, 25%
L3 = 5ns, 15%
m = 15ns, 25%

main memory
100% − (35 + 25 + 15) = 25

avg time
1 x .35 + 3 x .25 + 5 x .15 + 15 x .25
= 5.6

hit/miss rate
25% → miss
35 + 25 + 15 = 75% → hit

3) Direct mapping. A list of memory requests by CPU is given below.

a) Determine cache memory hit or miss for each case.
b) Obtain the updated version of the cache memory.
c) Calculate hit and miss rate.

0	0000	00	01	10	11	M0
1	0001	00	01	10	11	M1
2	0010	00	01	10	11	M2
3	0011	00	01	10	11	M3
4	0100	00	01	10	11	M4
5	0101	00	01	10	11	M5
6	0110	00	01	10	11	M6
7	0111	00	01	10	11	M7
8	1000	00	01	10	11	M8
9	1001	00	01	10	11	M9
10	1010	00	01	10	11	M10
11	1011	00	01	10	11	M11
12	1100	00	01	10	11	M12
13	1101	00	01	10	11	M13
14	1110	00	01	10	11	M14
15	1111	00	01	10	11	M15

	Valid	Tag	Data
00	1	10	M8
01	0	00	M1
10	1	01	M6
11	0	11	M15

Memory requests	Hit(1)/Miss(0)	Data[offset]
000000	0	M0[00]
011001	1	M6[01]
111100	0	M15[00]
000111	0	M1[11]
110000	0	M12[00]
010101	0	M5[01]
011110	0	M7[10]

Updated cache table

	Valid	Tag	Data
00	1	11	M12
01	1	01	M5
10	1	01	M6
11	1	01	M7

$$hit = \frac{1}{7} = 14.29\%$$

$$miss = \frac{6}{7} = 85.71\%$$

4) What is the difference between data cache and instruction cache?

The instruction cache stores the commands the CPU needs to run programs, making it faster to fetch instructions. Whereas, the data cache, holds the actual information the CPU processes, these are things like numbers or text. Having separate caches helps the CPU work better by handling instructions and data at the same time.

5) Assuming that the number of cache lines is equal to 100 and 4 way set-associative mapping is employed:

a) Determine the number of cache sets

b) Obtain the cache set numbers for the given memory addresses (complete the following table).

Memory Index (MI)	Cache set number
100 % 25 =	0
250 % 25 =	0
131 % 25 =	6
23 % 25 =	23

a) S = lines/way sets = S = 100/4 = 25