Winter_25_Quiz_8 - Results

Attempt 1 of 1

Written Mar 18, 2025 7:54 PM - Mar 18, 2025 8:14 PM

You successfully submitted your quiz.

Attempt Score	**5 / 8 - 62.5 %**
Overall Grade (Highest Attempt)	**5 / 8 - 62.5 %**

Question 1

Obtain the cache set number for the following memory addresses (MI) . The number of cache lines is 64 (consider two way set-associative mapping). Show the details of your calculation.

a) 1123

b) 2047

cache set = # of cache lines / # ways
cache set = 64 / 2
cache set = 32

a)
cache set # = line % cache set
cache set # = 1123 % 32
cache set # = 3

b)
cache set # = line % cache set

cache set # = 2047 % 32
cache set # = 31

The correct answer is not displayed for Written Response type questions.

Question 2

Obtain the cache line number (cache index CI) for the following memory addresses (MI). The number of cache line is 128 and the main memory is directly mapped to the cache memory. Show the details of your calculation.

a) 5874

b) 4095

a) ci = cache line % # number of cache lines
ci = 5874 % 128

ci = cache line // # number of cache lines
a) = 45
b) = 31

The correct answer is not displayed for Written Response type questions.

▼ Hide question 2 feedback

Feedback

5874 % 128 = 114
4095 % 128 = 127

Question 3

Suppose we have a cache with 64 lines (cache blocks) and a block size of 16 bytes. If the memory address is 32 bits, how many bits are needed for the tag, cache index, memory index, and offset fields in the address? The main memory is directly mapped to the cache memory.

- MI = 28, TAG =22, CI = 6 , Offset = 4
- MI = 22, TAG =28, CI = 6 , Offset = 4
- MI = 22, TAG =28, CI = 4 , Offset = 6
- MI = 28, TAG =22, CI = 4 , Offset = 6

Done