Quiz 6: do it yourself; use the course notes - Results

Attempt 1 of 1

Written Jun 28, 2024 9:00 PM - Jun 28, 2024 9:58 PM

Attempt Score	**8 / 8 - 100 %**
Overall Grade (Highest Attempt)	**8 / 8 - 100 %**

Question 1 — 1 / 1 point

What does the following instruction mean in plain English? ADD R4, ((R5)), (R6)?

The instructions is asking to ADD the following data:

- R4: the data value stored in register R4

- ((R5)): the data value stored in the memory address which is stored in another memory address that is stored in register R5.

After adding the data, we store the resulting data in a memory address and that memory address is then stored in register R6.

The correct answer is not displayed for Written Response type questions.

Question 2 — 2 / 2 points

Write the microcode to fetch and decode an instruction for the one-bus datapath we studied last week. **Include lots of very clear, complete, plain-english comments beside each step** explaining what that step is doing, and why.

1. PCout, MARin, READ, Clear Y, Set Cin, ADD, Zin

In this first bus cycle we output the memory address contained in the program counter to internal CPU bus and then input that into the Memory Address Reader. Then CPU sends the READ command to Main Memory. Then we clear register Y to set it 0, and set the carry-in value to 1, and then ADD 1 to value B, which contains the program counter memory address. Then we take the result of that addition and store it in register Z.

2. Zout, PCin, WMFC

In the second bus cycle we output the memory address value contained in register Z to the internal CPU bus and then input it into the Program Counter. This increments the program counter memory address by 1. Then we wait for wait for memory function to complete.

3. MDRout, IRin, DECODE

In the next bus cycle after we receive the data from main memory in the Memory Data Reader (MDR), we output the intruction data to the internal CPU bus and input it into the instruction register. Then we send the data to the Instruction Decoder to decode the instruction in the instruction register.

The correct answer is not displayed for Written Response type questions.

Question 3 **2 / 2 points**

Show the microcode to execute (not fetch or decode) the instruction ADD R1, R2, R2, R1, where the last operand simply denotes the destination of the operation's outcome. Do this in the most efficient way the cpu can.

4. R2out, Yin, ADD, Zin
5. Zout, Yin
6. R1out, ADD, Zin
7. Zout, R1in, END

The correct answer is not displayed for Written Response type questions.

Question 4 **3 / 3 points**

Show the microcode to execute (not fetch or decode) the instruction ADD (R1), (R2), (R3) where the last operand simply denotes the destination of the operation's outcome. Do this in the most efficient way you can. Also, upload a drawing of the datapath showing your tracings of the data moving around the datapath, registers, and memory, etc.

4. R1out, MARin, READ, WMFC
5. MDRout, Yin
6. R2out, MARin, READ, WMFC
7. MDRout, ADD, Zin
8. Zout, MDRin
9. R3out, MARin, WRITE, WMFC, END

*Please see attached image file for full solution.

FDE4.jpg (90.58 KB)

The correct answer is not displayed for Written Response type questions.

Done