

No E-Mail submissions will be accepted.  
Submission formats and file naming:

File name : firstName\_lastName\_lab\_8

File format: pdf or MS Word format

e.g. Donald\_Trump\_lab\_8.pdf

Reading materials

Use the following link and write a one page summary about the movie.

|  |
| --- |
| Microcontroller and Its Application A picture containing text, electronics  Description automatically generated  <https://youtu.be/wPwHB8u-7ts> |

1) A list of cache replacement algorithms is given below. Choose one of the algorithms and write a summary about that.

1 – Least Recently Used (LRU)

In least recently used, the algorithm removes the least recently used or accessed memory. This happens when the cache is full and memory that needs to be accessed is not found in the cache. It works under the idea that recently used memory is more likely to be used again, so older unused data is replaced/. For example, a cache has 3 slots and loads data in the the order A, B, C, A, D. Here B is removed because the recent order of retrieval was D, A, C.

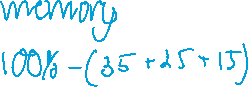
2 – First In First Out (FIFO)

3 – Least Frequently Used (LFU)

4 – Random

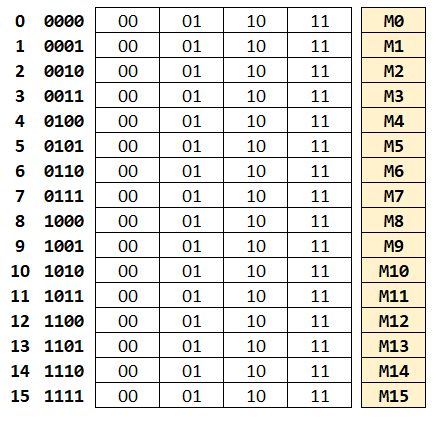
5 – Clock algorithm

2) Suppose that a CPU has a level 1 cache, a level 2 cache, and a level 3 cache with access times of 1 nsec, 3 nsec, and 5 nsec, respectively. The main memory access time is 15 nsec. If 35% of the accesses are level 1 cache hits, 25% are level 2 cache hits, 15% are level 3 cache hits, and the main memory access time is 15 nsec. What is the average access time? What is cache hit and miss rate?



3) Direct mapping. A list of memory requests by CPU is given below.

1. Determine cache memory hit or miss for each case.
2. Obtain the updated version of the cache memory.
3. Calculate hit and miss rate.



|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | | | | | | |
|  |  | Valid |  | Tag |  | Data |
| **00** |  | **1** |  | **10** |  | **M8** |
| **01** |  | **0** |  | **00** |  | **M1** |
| **10** |  | **1** |  | **01** |  | **M6** |
| **11** |  | **0** |  | **11** |  | **M15** |

|  |  |  |
| --- | --- | --- |
| Memory requests | Hit(1)/Miss(0) | Data[offset] |
| 000000 |  |  |
| 011001 |  |  |
| 111100 |  |  |
| 000111 |  |  |
| 110000 |  |  |
| 010101 |  |  |
| 011110 |  |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Updated cache table | | | | | | |
|  |  | Valid |  | Tag |  | Data |
| **00** |  |  |  |  |  |  |
| **01** |  |  |  |  |  |  |
| **10** |  |  |  |  |  |  |
| **11** |  |  |  |  |  |  |



4) What is the difference between data cache and instruction cache?

5) Assuming that the number of cache lines is equal to 100 and 4 way set-associative mapping is employed:

1. Determine the number of cache sets
2. Obtain the cache set numbers for the given memory addresses (complete the following table).

|  |  |
| --- | --- |
| Memory Index (**MI**) | Cache set number |
| 100 |  |
| 250 |  |
| 131 |  |
| 23 |  |

