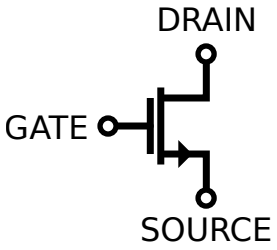
Zero to ASIC: Analogue Design

Thomas Parry

1 Fundamentals of the MOSFET

The MOSFET (Metal-Oxide Semiconductor Field Effect Transistor) is the fundamental building block of modern IC design.



The MOSFET is a *transconductance* device which translates a voltage between it's gate and source terminals to a current between the drain and source - assuming the device is biased correctly.

(a) The Saturation Region

Most devices in a circuit will be operating in saturation where the following description of the current is given for a square-law device:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{1}$$

This can be simplified to:

$$I_D = K_n\frac{W}{L}{V_{OD}}^2 \tag{2}$$

$$given\ that: \quad V_{DS} > V_{OD} \tag{3}$$

The condition is very important, if you want your FET to work as expected you must ensure you have sufficient V_{DS} headroom. The value V_{OD} is also more commonly called $V_{D_{SAT}}$ and is defined as the minimum drain voltage required to keep the device in saturation. Note that in sub-micron processes (like Skywater 130 nm) the statement that $V_{D_{SAT}} = V_{OD}$ is not fully accurate due to second order effects from device scaling.

(b) The Triode Region

When there is insufficient drain-source voltage (by design or error) the device will work in the triode region where it approximates a voltage controlled resistor:

$$I_D = \mu_n C_{ox}\frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{4}$$

(c) The Cutoff Region

When there is insufficient voltage across the gate-source terminals the device is 'off':

$$I_D = 0 \quad given\ that: \quad V_{GS} << V_{TH} \tag{5}$$

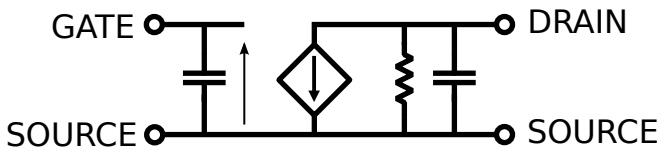
> Always know the region you expect your FET to operate and check that you have it correctly biased or all other assumptions are broken.

2 Basics of Transconductance Efficiency

The transconductance is the amount of current in the drain per gate-source voltage.

$$i_d = g_m \cdot v_{gs} \tag{6}$$

This simple diagram shows the most important concept of the FET: a voltage at the input is converted to an output current. This output current will later be converted by an impedance to another voltage.



The transconductance can be expressed as a function of the bias current, giving the g_m/I_d value. This value is related to how inverted the channel of the FET is - a measure of how 'turned on' the FET is. The measure of channel inversion is how many minority charge carriers have been attracted to the conductive channel between the source and drain.

(a) Transconductance Efficiency and Overdrive Voltage

There is a relation to the overdrive voltage mentioned above, V_{OD}. The higher the V_{OD}, the more the FET is 'turned on', and therefore the more the FET channel is inverted, which leads to a *lower* g_m/I_d. Conversly, a lower V_{OD} turns on the FET less, and therefore the FET channel is less inverted, which leads to a *higher* g_m/I_d.

(b) Realistic Values of Transconductance Efficiency

There is a range of transconductance efficiencies that can be obtained in standard CMOS processes. It is reasonable to assume a maximum transconductance efficiency of 20 in design equations, although in some specific cases values of 25 can be reached. Typically a device will not be used below a transconductance efficiency of 4.

(c) Why Use Transconductance Efficiency?

While transconductance efficiency, g_m/I_d, feels very abstract at first, its use lies in two factors.

1. It gives a strong indication of the channel inversion.
2. It allows quick calculation of circuit currents and other conditions.

For example, if I have determined I will use a FET in weak inversion and I need $1\ mS$ of transconductance, then I very simply know the required current of $50\ \mu A$.

> But how do we know what transconductance we should use for a given FET? We'll discuss this in the next section where I will talk about the relation of matching and noise to transconductance.

Further Reading (clickable)

gm/ID - Based Design
An Introduction to the EKV Model and a comparison of EKV to BSIM