GROUP 3 – STATUS PRESENTATION

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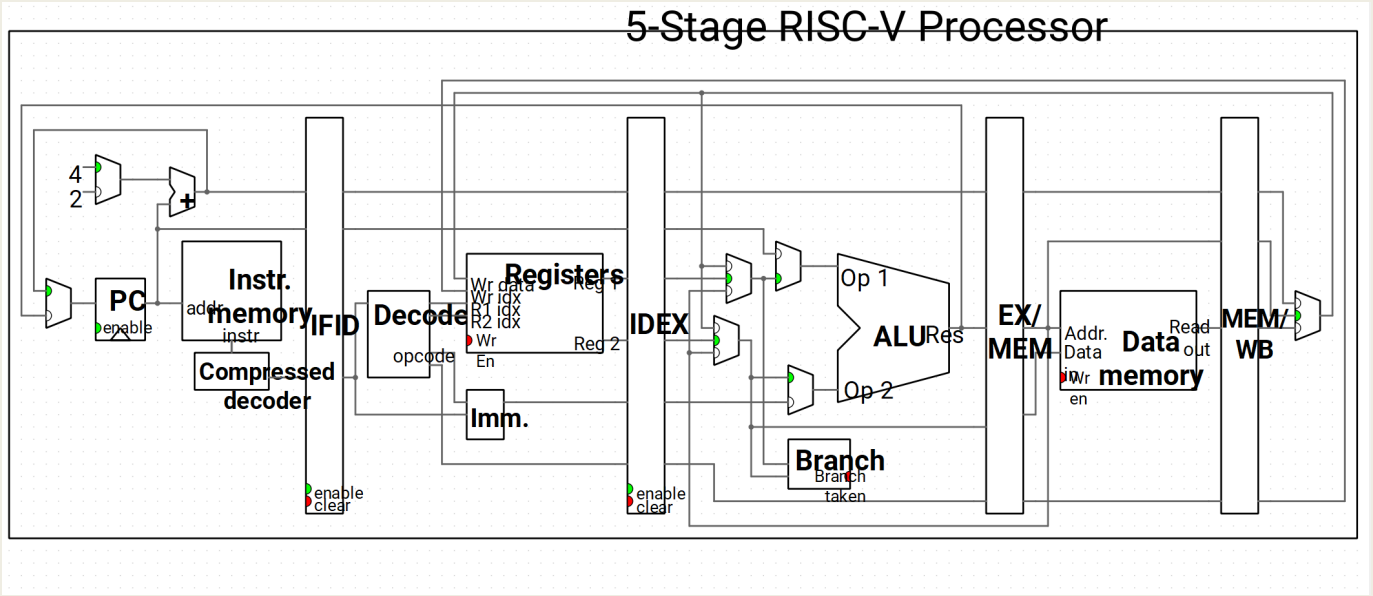
Design Idea

- Implement 5-stage RISC-V processor
- Separate instruction and data memory
- Include forwarding, if possible branch prediction unit
- Test-driven development



So far..

- Two instruction types programmed in decoder
- Addi works
- Implemented basic pipeline
- Functioning registers
- Decoder works in early stages
- Succesful ALU and CPU tests