Inverse Sizing and Exploration Based on Diffusion Models and Structural Knowledge

***Abstract*—Quick and effortless exploration of design spaces is of major importance in the face of rapid development cycles, varying specifications and increasingly complex circuits. It is also well known, that the exploitation of slack in specifications by making adjustments to transistor device sizes can lead to improved yield. We address those challenges by combining two state of the art machine learning approaches to achieve accurate generation of optimal performance points, while also allowing for the possibility to explore nearby sizings that might lead to more robust designs. To this end, a diffusion model is combined with an algorithm, that analyzes the circuit and splits the problem into simpler subproblems. The models are tested on a set of typical operational amplifiers.**

I. Introduction

Since the development of SPICE, the industry accepted method for designing analog circuits has not changed much. While the SPICE models keep becoming more complex [1], the approach of manual device tuning persists [2]. Key challenges of making analog CAD tools useful in practice are robustness, ease of use and applicability to a high range of use cases. All those aspects are not easy to grasp on a fundamental level. On the other hand, machine learning approaches excel in modeling nonlinear black box phenomena. Their combination with already existing conventional techniques has a high potential to bridge remaining gaps, that prevent the adoption of tools in industry.

Analog design is inherently an inverse problem. While the calculation of performances, yield etc., is satisfactorily possible via simulation, the inverse, i.e. getting a circuit with optimal parametrization requires experience, trial and error and complex numerical routines. As shown in previous works [4], [5], machine learning (ML) methods can be used to accurately reproduce sizings on (pareto) optimal fronts. Furthermore, it has been shown [3] that diffusion models are well adaptable to the inverse sizing problem. Other ML based works attempted to solve this same problem. In [16], artificial neural networks (ANNs) are used to guess circuit sizings, utilizing only one ANN for modeling an entire netlist, leading to a higher learning task complexity and thus large sample sizes (in [16] 16600 or roughly $16 - 160\,x$ sample sizes used in this work) are required to learn the inverse problem within a smaller performance range. In [19], the problem is broken down into smaller tasks, and one ANN is trained to sequentially size a single device, in the same vein as [4], feeding the outputs of the previous ANNs to the input of the next, producing a cascade of networks that can be sorted in different ways, until an optimal order is found. The drawback is that for more complex circuits of e.g. 15 devices, optimally ordering the ANNs for sizing leads to a complexity of 15!.

Other works follow the traditional approach of tackling the direct sizing problem, treating it as an optimization problem [20]–[23]. Reinforcement learning was also studied, with [**?**], [17], [18] replacing the optimizer with an artificial neural network (ANN), leading to improvements in prediction speed, accuracy, and scalability. However, to the best of our knowledge, none of them show strengths in all four categories, speed, accuracy, sample efficiency and exploration.

In this work, we aim for a combination of all those virtues by applying denoising diffusion probabilistic models (DDPM) to the sizing of OpAmps, utilizing the approach in [4] of subdividing the circuits into simpler structures, which has shown high accuracy for low sample sizes. DDPMs have proven their potential for generating strongly varied, but realistic results in other fields, OpenAi's DALL-E and Stable Diffusion being among the most prominent examples. [3] proved these model's efficacy in the inverse sizing problem.

Unlike most machine learning models, DDPMs can suggest different sizings for the same problem by repeatedly sampling them. As shown in Section IV, this approach to the inverse problem can produce a more varied set of possible sizings, which is very helpful when exploring sizing options in the vicinity of performance optima. This work contributes a machine learning approach that:

- can suggest valid sizings with resulting performance in the vicinity of the required metrics, allowing for exploration of sizings while still fulfilling specifications
- is highly data efficient
- has an accurate expectation of the generated sizings
- generates sizing solutions at push-button speed

In section II, we provide an overview of the proposed method and its connection to structural analysis. In sec. **??**, we describe the sizing process in detail. We conclude with a presentation of results for two OpAmps.

II. From Structural Analysis to Circuit Sizing via Machine Learning

A. Basics of Structural and Functional Blocks

Our method heavily relies on decomposing circuits into subcircuits, which we call structural building blocks. Most building blocks are known to the analog designer by names such as *current mirror* or *differential pair*.

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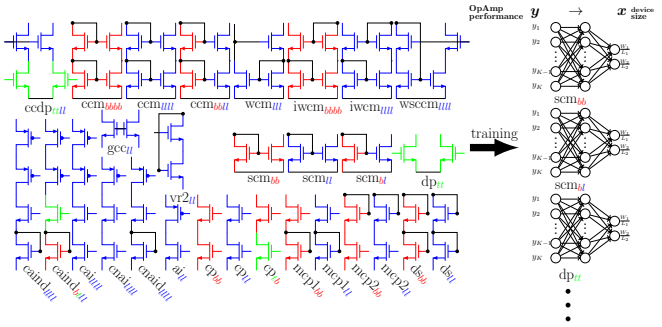

Fig. 1: Splitting various OpAmps into canonical building blocks with different functional characteristics and accumulating intrinsic design know-how by training each building block with random optimal samples from all available OpAmps. Indices b, l and t represent *bias*, *load* and *transconductance* functionality of devices. Every building block maps the overall OpAmp performance to its sizing.

We further distinguish different functional variants of one and the same structural block. To this end, we assign to every transistor in a circuit its functional property, out of three different possibilities: *bias, load* or *transconductance*. For example, a *simple current mirror* (scm) can act as *load*, but in other parts of a circuit, the same building block can act as *bias*. And sometimes, some part of a current mirror can act as *load*, while another part acts as *bias*. Figure 1 shows all structural blocks and their functional variants from our dataset. An example of decomposing a Folded-Cascode OpAmp into blocks can be seen in figure 2a. Its structural building blocks are shaded, the names annotated close by. Structural and functional block recognition is fully automated. The time required for this is much less than one second.

B. Overview of the Method

III. Conclusion

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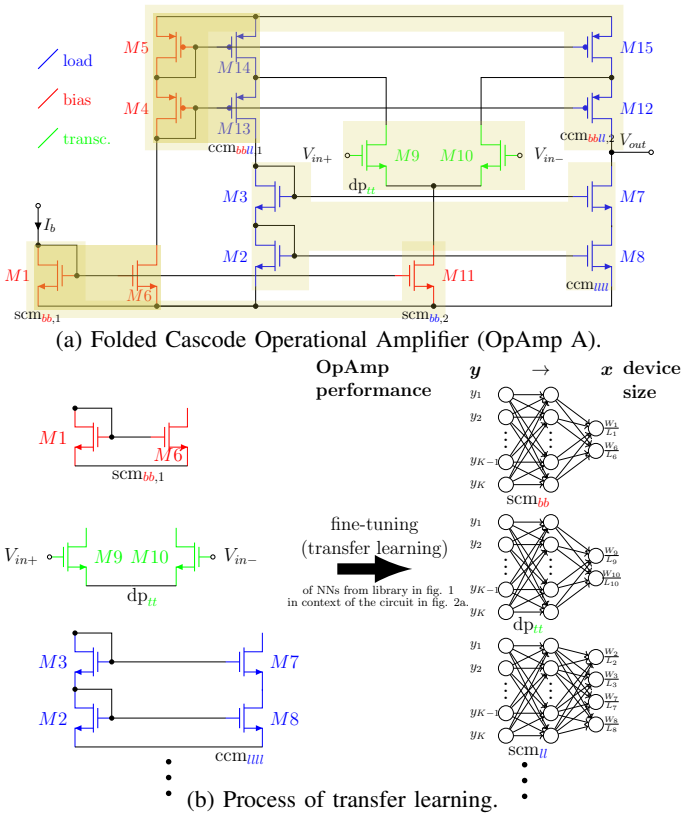
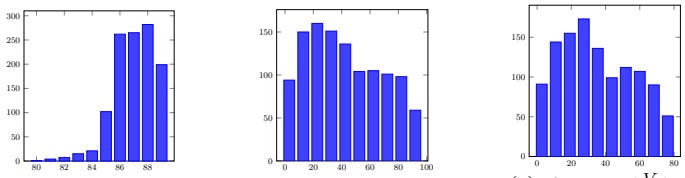


(a) Folded Cascode Operational Amplifier (OpAmp A).

(b) Process of transfer learning.

Fig. 2: Instead of training one huge network per OpAmp, we can split an Opamp, e.g. OpAmp A, into blocks (shading and coloring in fig. 2a) and use weights from our network-database as initial training points to merely fine-tune our networks (2b).



(a) gain (dB) (b) trns. fr. (Mhz) (c) slew rate ($\frac{V}{\mu s}$)

(d) power (mW) (e) phase margin (f) CMRR

Fig. 3: Histograms of some performance features for the Folded-Cascode OpAmp in Fig. 2a.

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