Inverse Sizing and Exploration Based on Diffusion Models and Structural Knowledge

***Abstract*—Quick and effortless exploration of design spaces is of major importance in the face of rapid development cycles, varying specifications and increasingly complex circuits. It is also well known, that the exploitation of slack in specifications by making adjustments to transistor device sizes can lead to improved yield. We address those challenges by combining two state of the art machine learning approaches to achieve accurate generation of optimal performance points, while also allowing for the possibility to explore nearby sizings that might lead to more robust designs. To this end, a diffusion model is combined with an algorithm, that analyzes the circuit and splits the problem into simpler subproblems. The models are tested on a set of typical operational amplifiers.**

I. Introduction

Since the development of SPICE, the industry accepted method for designing analog circuits has not changed much. While the SPICE models keep becoming more complex [1], the approach of manual device tuning persists [2]. Key challenges of making analog CAD tools useful in practice are robustness, ease of use and applicability to a high range of use cases. All those aspects are not easy to grasp on a fundamental level. On the other hand, machine learning approaches excel in modeling nonlinear black box phenomena. Their combination with already existing conventional techniques has a high potential to bridge remaining gaps, that prevent the adoption of tools in industry.

Analog design is inherently an inverse problem. While the calculation of performances yield etc., is satisfactorily possible via simulation, the inverse, i.e. getting a circuit with optimal parameterization requires experience, trial and error and complex numerical routines. As shown in previous works [3]–[5]

With increasing MOSFET model complexity [1], analog design, particularly OpAmp design, remains manual in industrial practice [2], despite the existence of automatic tools. Various procedural methods for automated design have been discussed in [6]–[8]. The idea of using smaller building blocks and hierarchical strategies is successfully demonstrated, e.g., in [9]–[13]. Early on, modeling performance characteristics of circuits has been popular, e.g. by symbolic analysis [14], [15]. Some prior works in the machine learning realm follow the idea of skipping or replacing the optimization algorithm by other means such as neural networks (NNs). In [16], artificial neural networks (ANNs) are used to guess circuit sizings; due to modeling the entire netlist with one ANN and including non-optimal results in the former case, the complexity of the learning task is higher and thus large sample sizes (in [16] 16600 or roughly $16 - 160\,x$ our sample sizes) are required to learn the inverse problem within a smaller performance range. Similarly to our work, [5] uses optimal samples for training but without exploiting structural knowledge. In [17], [18], reinforcement algorithms are presented, substituting the optimizer with an NN. Here, the simulation effort is increased as multiple rounds are required for every sizing, similar to traditional optimization. In [19], the complexity of the NNs is reduced by having small networks represent single device parameters and cascading them in different ways, feeding outputs of earlier networks to the input of later networks in the tree. Unfortunately, with a circuit of e.g. 15 devices/networks, optimally ordering them in a chain can lead to a complexity of 15! in the worst case. Other works, such as [20]–[23], follow the traditional approach of treating sizing as an optimization problem or concentrate on performance modeling. While achieving good accuracy in their findings, they contend with the costly iteration process inherent in optimization.

In this paper, utilizing sampled sizings from the open-source tool FUBOCO [24], we introduce a machine learning algorithm for sizing operational amplifiers **without the need for optimization and simulation** during the deployment phase. Our approach stands out by **capitalizing on automatically extracted structural** and **functional information**, a departure from related works. This brings about benefits in terms of speed, flexibility, and accuracy. The required sample size, setup- and evaluation-time, as well as necessary expert knowledge are kept at a minimum. Additional contributions include the creation of a comprehensive database of netlists, the development of a custom loss function, and the utilization of a quasi-Newton optimizer for training purposes.

In section II, we provide an overview of the proposed method and its connection to structural analysis. In sec. **??**, we describe the sizing process in detail. We conclude with a presentation of results for two OpAmps.

II. From Structural Analysis to Circuit Sizing via Machine Learning

A. Basics of Structural and Functional Blocks

Our method heavily relies on decomposing circuits into subcircuits, which we call structural building blocks. Most building blocks are known to the analog designer by names such as *current mirror* or *differential pair*.

We further distinguish different functional variants of one and the same structural block. To this end, we assign to

Parts of this work have been done within the collaborative project HoLoDEC funded by the Federal Ministry of Education and Research Germany (BMBF) under the funding code 16ME0705.

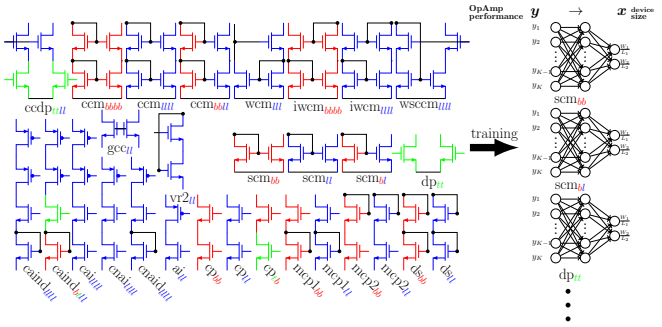

Fig. 1: Splitting various OpAmps into canonical building blocks with different functional characteristics and accumulating intrinsic design know-how by training each building block with random optimal samples from all available OpAmps. Indices b, l and t represent *bias*, *load* and *transconductance* functionality of devices. Every building block maps the overall OpAmp performance to its sizing.

every transistor in a circuit its functional property, out of three different possibilities: *bias, load* or *transconductance*. For example, a *simple current mirror* (scm) can act as *load*, but in other parts of a circuit, the same building block can act as *bias*. And sometimes, some part of a current mirror can act as *load*, while another part acts as *bias*. Figure 1 shows all structural blocks and their functional variants from our dataset. An example of decomposing a Folded-Cascode OpAmp into blocks can be seen in figure 2a. Its structural building blocks are shaded, the names annotated close by. Structural and functional block recognition is fully automated. The time required for this is much less than one second.

B. Overview of the Method

III. Conclusion

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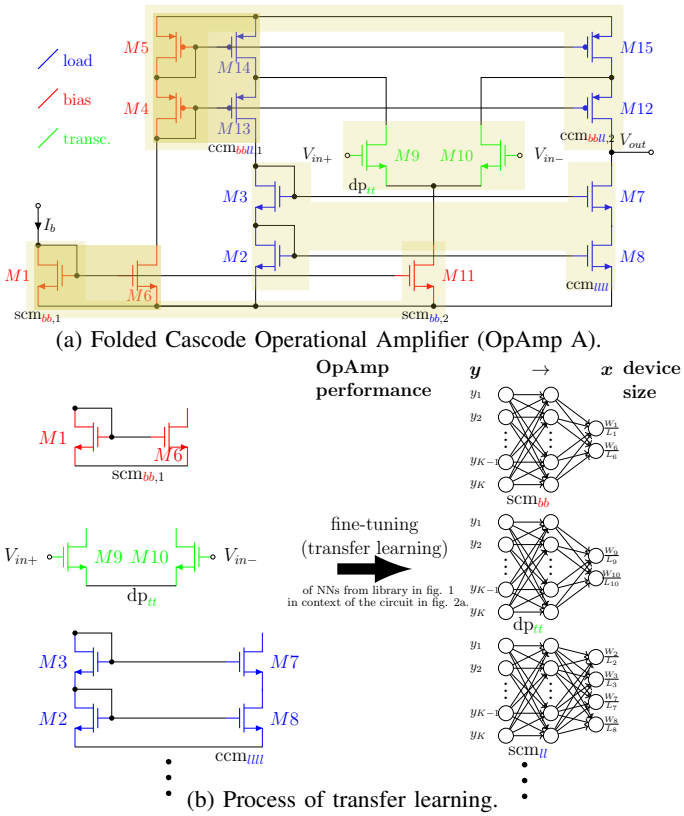
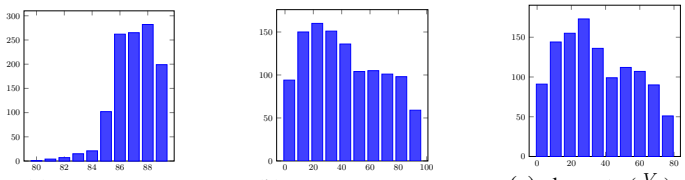


(a) Folded Cascode Operational Amplifier (OpAmp A).

(b) Process of transfer learning.

Fig. 2: Instead of training one huge network per OpAmp, we can split an Opamp, e.g. OpAmp A, into blocks (shading and coloring in fig. 2a) and use weights from our network-database as initial training points to merely fine-tune our networks (2b).



(a) gain (dB) (b) trns. fr. (Mhz) (c) slew rate ($\frac{V}{\mu s}$)

(d) power (mW) (e) phase margin (f) CMRR

Fig. 3: Histograms of some performance features for the Folded-Cascode OpAmp in Fig. 2a.

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