EE2026: DIGITAL DESIGN
Academic Year 2020-2021, Semester 1

FPGA Design Project:
Sight and Sound Entertainment System

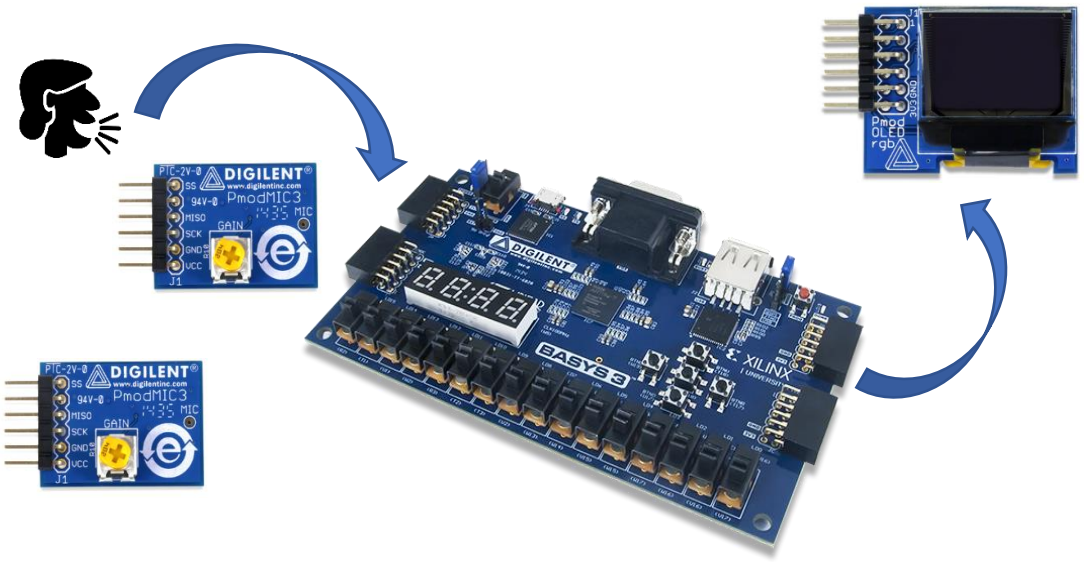
ABSTRACT

Using the fundamental technical skills obtained from the previous lab sessions, you will be creating a Sight and Sound Entertainment (SSE) system. Two types of additional devices will be provided to you for the system:

- **MEMs microphone:** This analog-to-digital device will capture audio signals from the surroundings, and provides the data to you in a digital format.
- **OLED RGB Display Screen:** Information can be displayed on this 96 x 64 bit display screen with 16-bit colour resolution.

(You will need to replace the devices at your own cost if damaged. Extensions are not given for damaged components. Use them with upmost care!)

This manual introduces to you some concepts involved, and guides (NOT handhold!) you through getting a basic SSE up and running. You will need to use your own logic, creativity and resourcefulness to enhance the SSE system.



1. PROJECT OVERVIEW

This SSE system is a pair work project that includes both **individual** and **teamwork** components.

Some milestones that you are requested to achieve for the SSE system will be detailed in **Section 4** of this lab manual. To make your system more functional, user-friendly and unique, your team will also need to work on features of your own choosing!

2. SCHEDULE AND COMPONENT WEIGHTAGE

This project constitutes 35% of the overall grade for EE2026. The breakdown in weight is tabulated below:

<table>
<tr><th>Week</th><th>Tasks</th><th colspan="2">Student A</th><th>Student B</th><th>Tasks' Evaluation</th></tr>
<tr><td>8</td><td>Teamwork (Task 1A and Task 1B):
Basic display of audio signal on OLED
(Microphone – Basys 3 – OLED Interfacing)</td><td colspan="2">4%
Team</td><td></td><td>Evaluated at the start of week 9 lab session.
This will not be evaluated again in week 12 / 13</td></tr>
<tr><td>9</td><td>Student A (Task 2A):
Real-time audio volume indicator
(Microphone – Basys 3 interfacing)

Student B (Task 2B):
Graphical visualizations and configurations
(OLED – Basys 3 interfacing)</td><td>8%
Individual</td><td></td><td>8%
Individual</td><td>Evaluated in week 12 / 13 as a complete project</td></tr>
<tr><td rowspan="2">10</td><td>Teamwork:
• System Integration: User-Friendly Sound Display and Entertainment system
• Improvement feature(s) (open-ended)</td><td colspan="2">10%
Team</td><td></td><td rowspan="2">Evaluated in week 12 / 13 as a complete project</td></tr>
<tr><td>Student A:
Improvement feature(s) (open-ended)

Student B:
Improvement feature(s) (open-ended)</td><td>8%
Individual</td><td></td><td>8%
Individual</td></tr>
<tr><td>11</td><td>No lab session</td><td>-</td><td></td><td>-</td><td>Project archive and Report submission at the end of week 11</td></tr>
<tr><td>12 / 13</td><td>Project Assessment</td><td>5%
Individual: Q&A (execution and understanding)</td><td></td><td>5%
Individual: Q&A (execution and understanding)</td><td>The complete project (ONE bitstream only), supported by the report, is evaluated</td></tr>
</table>

PLAGIARISM WARNING

This is a teamwork project. Discussions are encouraged. However, 'discussion' is not a valid excuse if your codes turn out to be uncomfortably similar. NUS and the EE2026 teaching team take plagiarism very seriously.

- Warning from the NUS Code of Student Conduct:
  "Any student found to have committed or aided and abetted the offence of plagiarism may be subject to disciplinary action" http://www.nus.edu.sg/registrar/adminpolicy/acceptance.html
- Both the source and recipient of the project solutions (codes) or reports will be **unconditionally penalised** in such cases. Marks will also be adjusted and withheld from release if the codes are similar beyond a certain empirical threshold.
- Students will also be reported to BoD (Board of Discipline).

3. HARDWARE AND SOFTWARE RESOURCES

HARDWARE COMPONENTS:

- Each team can only sign out **1 PmodMIC3** and **1 Pmod OLEDrgb** from the Digital Electronics Lab from week 8 onwards
- Each student has already been assigned **1 Basys 3** Development Board at the beginning of the semester

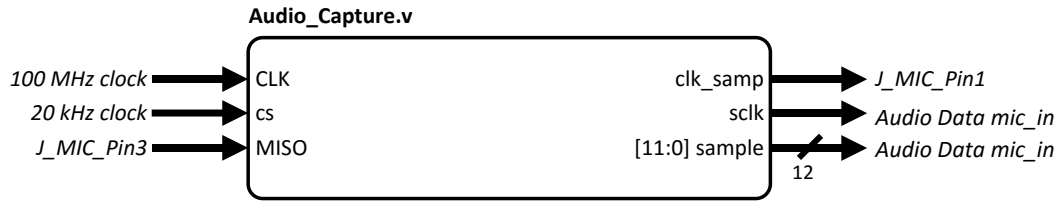
SOFTWARE FILES:

A project template (**SoundDisplay.xpr.zip**) can be downloaded from LumiNUS. The template consists of the following:

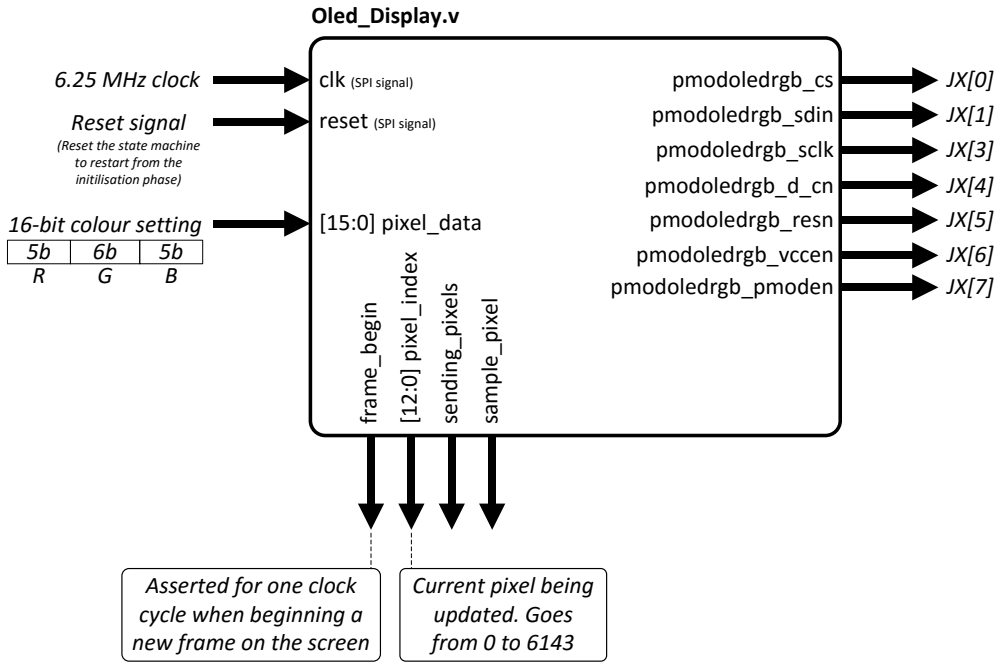
Design Sources:

Top_Student.v: The top-module of the design. This will be your main module, or typically called the Top Level module, where you instantiate the sub-modules and make the necessary links between these sub modules. **You will need to modify this module, as well as create other design sources for use in this module.**

Audio_Capture.v: An interface module between the microphone pmod device and your design on the FPGA. This module works with the *PmodMIC3* to convert the serial data input into a 12-bit parallel `mic_in` sample data. The conversion needs a sampling clock and a serial clock. **You are NOT required to make changes to this module.**



Oled_Display.v: An interface module between your design on the FPGA and the OLED display. This module works to send serial SPI data into the OLED display for initialization and drawing. **You are NOT required to make changes to this module.**



Constraint Sources:

Basys3_Master.xdc: A master constraints file that defines the I/O constraints for the Basys 3 Development Board

MODULE WIKI:

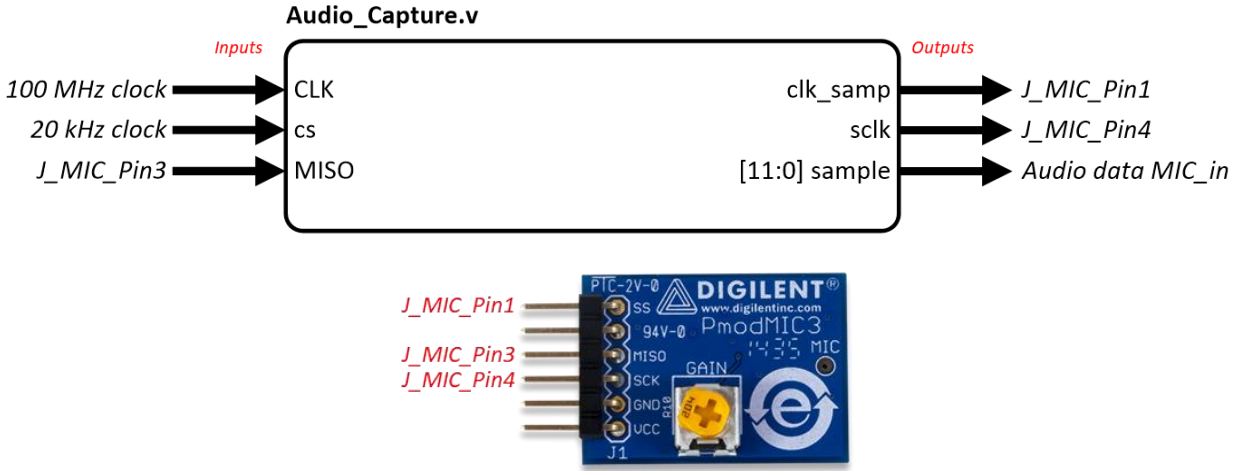
tiny.cc/ee2026wiki : The project wiki includes a Verilog error troubleshooting guide, VHDL vs verilog code comparison and useful resources when you are working on additional features.

4. TASKS AND REQUIREMENTS

4.1 BASIC DISPLAY OF AUDIO SIGNAL ON OLED

OBJECTIVE: To set up the SSE system, by interfacing the Basys 3 Development Board with the PmodMIC3 and the PmodOLED. Your system will capture and digitize the audio signal input from the microphone on the PmodMIC3. The data will then be processed by the FPGA, for display on the PmodOLED

STUDENT A: Setting up the Microphone



A1. **Instantiate the `Audio_Capture.v` module in `Top_Student.v`**

A2. **Create and provide the 100MHz and 20kHz (`clk20k`) clock signals to `Audio_Capture.v`**
The 20kHz clock is used as the sampling clock for capturing the audio signal. At every rising edge of this 20kHz clock signal, the audio signal from the microphone is read and stored in a 12-bit register named `sample`. This means that a 1s audio signal will need to be represented by 20,000 discrete samples.

A3. **Name the microphone data you receive from Audio_Capture.v, `mic_in`, and display this on 12 LEDs.**
`mic_in` is the 12-bit data that is being read by the microphone. By displaying the microphone input on the LEDs, a quick visual observation can indicate if the microphone is properly connected.

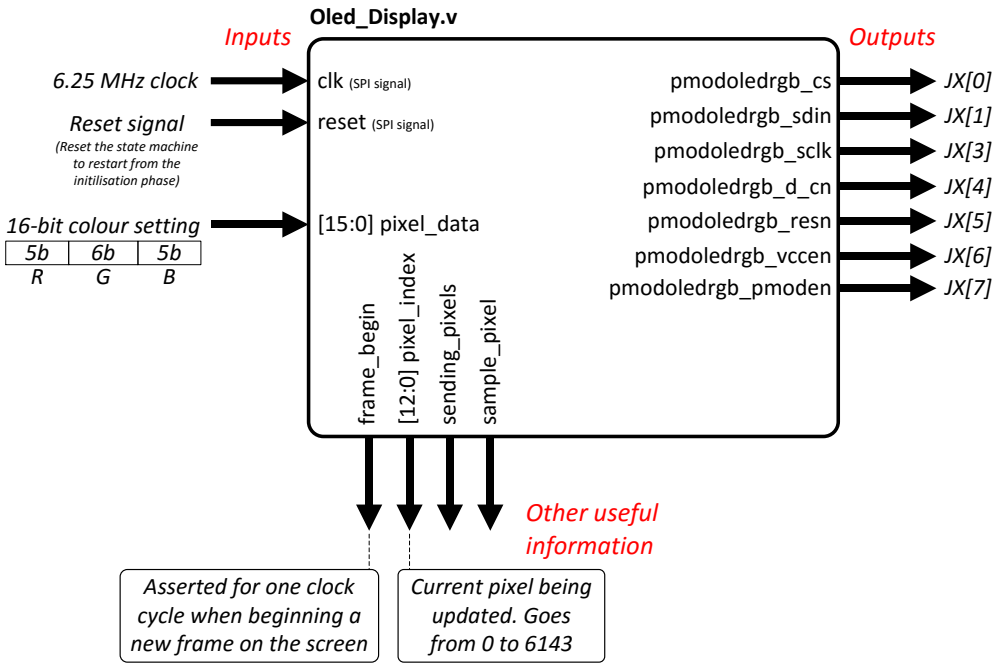
A4. **Now, create a 1-bit-two-to-one multiplexer that switches the LEDs between the following signals when sw[0] is toggled:**
- The 12-bit `mic_in`
- A zero signal

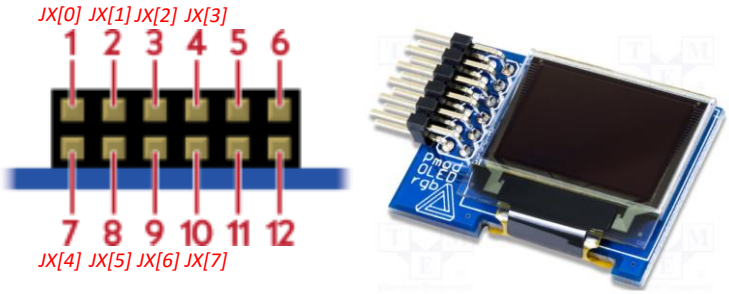
A5. **Connect the rest of the signals (`J_MIC_Pin1/2/3/4`) to the PmodMIC3 device accordingly.**
These are necessary input and output signals required for the microphone to function correctly.

A6. **Attach the PmodMIC3 with FPGA. Update the constraints file according to the chosen Pmod Ports**
Very Important: To avoid damaging the boards, make sure the GND and VCC pins on the Pmod and Basys3 are connected correspondingly

A7. **Generate the bitstream and download to the FPGA. If the above is executed correctly, you would observe :**
- All LEDs light up or flicker when displaying `mic_in`.
- All the LEDs switch off when the control signal of the multiplexer (created in step A4) is toggled

STUDENT B: Setting up the OLED





B1. **Instantiate the `Oled_Display.v` module in `Top_Student.v`**

B2. **Create and provide a 6.25MHz clock signal named `clk6p25m`, to `Oled_Display.v`**

B3. **Create a debounced single pulse signal named `reset`**
This `reset` signal should be asserted for one clock cycle when the center pushbutton on the Basys 3 is pressed once. Connect it as the Reset signal as labelled in the block diagram.

B4. **Create a 16-bit signal named `oled_data` and initialize it with a value of `16'h07E0`.**
The `oled_data` defines the colour of each pixel. Since the RGB OLED screen has 16-bit color resolution, this is represented through 5 bits for the red colour component, 6 bits for the green colour component, and 5 bits for the blue color component. Connect it to the `pixel_data` input of Oled_Display.v.

B5. **Connect the `JX[0:7]` signals to the PmodOLED device accordingly.**

B6. **Attach the OLED display to the Basys 3 and update the constraints file accordingly.**

B7. **Generate the bitstream and download to the FPGA**
Verify that the background colour of the screen is green. Why is it green?
Verify that the screen resets when you press the center pushbutton.

TEAMWORK: System Integration

C1. **Combine the codes from both members.**

C2. **Connect the MSBs of `mic_in` to part of the 16-bit colour setting given to the OLED through `oled_data`**
The 16-bit colour setting consists of 5 bits for the red colour component, 6 bits for the green colour component, and 5 bits for the blue component. According to the **first rightmost numerical digit** of the matriculation card of **student B**, the 5 (or 6 for green) most significant bits of `mic_in` must be connected to the RGB components as tabulated below:

Rightmost numerical digital of student B	R	G	B
0	✓		
1		✓	
2			✓
3	✓		✓
4	✓		
5		✓	
6			✓
7	✓		✓
8		✓	
9			✓

A tick (✓) indicates that the 5 (or 6 for green) most significant bits of `mic_in` are connected to that respective colour component

C3. **Generate the bitstream and download to the FPGA**

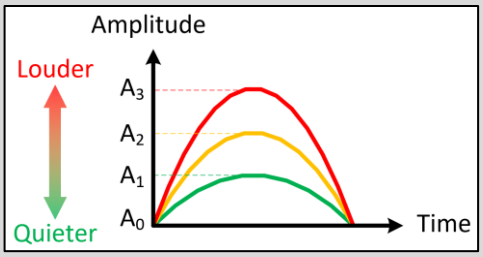
- Observe a single colour with varying intensities, depending on the audio signal
- Using a tone generator application, supply a sine wave to the microphone. You will observe a cyclic repetitive pattern on the OLED screen

C4. **Demonstrate the above to the lab instructors at the <u>beginning</u> of your lab session in Week 9**

Note: *After this section 4.1. has been evaluated in week 9, it will not be evaluated again during the complete project assessment in week 12 / 13. You may remove components you no longer need after the evaluation in week 9*

4.2A [STUDENT A] REAL-TIME AUDIO VOLUME INDICATOR

DESCRIPTION: An audio volume indicator displays a representation of the audio intensity in audio equipment. It helps people to observe the changes in the audio signal visually, such as by extracting the amplitude data from a waveform:



In this task, we use the 7-segment displays and LED array on the Basys 3 as audio volume indicators. Each numerical value on the 7-segment displays, and each LED, would represent an amplitude range from the audio signal.

X1. **Use the LED array and 7-segment displays to show the peak intensity (volume) of the audio signal (`mic_in`)**

X2. **Replace the "zero signal" in task A4 with the peak intensity (volume) signal of task X1**

X3. **The LED array of task X1 should display intensity linearly and refresh at an observable rate**

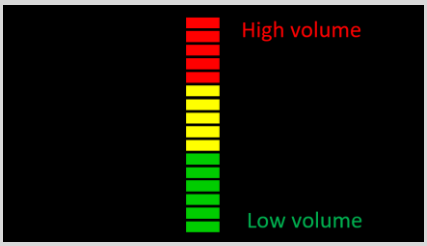
X4. **The 7-segment display indicates volume an observable rate, using decimal digits from 0 to 15**

GUIDELINES:

- The peak volume mapped to the LEDs must remain for a reasonable period of time to be observable by human eyes. You may need to record the peak value of a set of sampled data within this period of time
- A linear display means the LEDs should light up as a bar, instead of individual bits. That is, once the volume reaches a certain level, all LEDs below the level should light up
- **To test if your peak intensity (volume) algorithm works well, the following must be observed:**
  If a sinusoidal test signal of constant amplitude is used as an input audio signal, an approximately constant volume reading should be produced. If your volume reading is not quite stable, you may need to improve upon your peak intensity algorithm

4.2B [STUDENT B] GRAPHICAL VISUALIZATIONS AND CONFIGURATIONS

DESCRIPTION: To improve the user-friendliness of the SSE system, the volume can be graphically represented as a basic volume bar on the OLED screen:



In this task, you need to design a linear volume bar with 0 to 15 levels. On a black background, the bars should be colour-coded in green, yellow and red to indicate when volume is low or high. Text is not required.

Y1. **Create a white border near the four corners of the OLED screen**
The user must be able to choose between two borders: One with a thickness of 1 pixel, the other 3 pixels

Y2. **Design two other complementary colour themes which are easy to visualize**
A colour theme affects the OLED background colour AND the border colour AND the volume bar AND other components' colour on the OLED screen. The colours must all be easy on the user's eyes

Y3. **Implement a function to turn on / off specific parts of the display independently. This includes:**
- Turning on / off the border
- Showing / hiding the volume bar
- Showing / hiding other components on the OLED screen

Y4. **Implement a function to freeze the volume bar being shown on the screen at any time instant**

GUIDELINES:

- Work on creating an **x** and **y** coordinate system derived from `pixel_index` to make the pixel drawings on the OLED screen less cumbersome (*Hint: You may employ the modulus % and / operators*)

4.3 SYSTEM INTEGRATION AND IMPROVEMENT FEATURE(S)

Working together with your partner, integrate the tasks from **Section 4.1**, **Section 4.2A** and **Section 4.2B** to graphically display the volume on the OLED screen. Ensure that your SSE system is easy to use and user-friendly.

As part of the project requirements, you are furthermore required to implement improvement feature(s) to add value to the Sound Display and Entertainment system, in order to distinguish your unique system from the rest. The system should be made more interactive, interesting, functional and user-friendly.

The additional improvement(s) are open-ended and will be evaluated equally amongst the metrics of
(1) Functionality : Feature(s) should provide useful function in the context of a SIGHT AND SOUND entertainment system. Features that satisfy this only partially (SIGHT or SOUND) are nonetheless still accepted.
(2) Complexity : Describes complexity in implementation of feature.
(3) Quality : Describes how feature(s) or user experience(s) is designed well or thorough.
(4) Creativity : Describes creativity or uniqueness in feature(s) or implementation.

Before you connect other external devices to the Basys 3 development board, you need the approval of your lab assistant.

5. PROJECT SUBMISSION

There are two items (ITEM A, and ITEM B) to submit to LumiNUS. Penalties apply for late submissions.

Official Lab Session	ITEM A Project Archive	ITEM B Report
Monday	**Deadline:** End of Week 11 Saturday, 31st October 2020, 12:00 P.M.	**Deadline:** End of Week 11 Monday, 02nd November 2020, 12:00 P.M.
Tuesday		
Wednesday		
Thursday		
Thursday		

Improvements are evaluated based on your own original **Verilog** program codes. The grading metrics consist of quality, complexity, functionality and creativity.

5.1 ITEM A: PROJECT ARCHIVE SUBMISSION

- Only **ONE** Vivado project archive (.zip) per team. **The archive should not exceed 50 MB in size.** (Excess of 50 MB in size is only allowed with prior approval from the lab assistant, and only if Xilinx IP cores have been used)
- Ensure that your bitstream has been successfully generated and tested on your Basys 3 development board **BEFORE** archiving your Vivado workspace for LumiNUS upload. Download your LumiNUS archive after uploading. Unzip it / Extract all, and check if you can run your bitstream correctly
- Name your project archive in the format indicated below to avoid losing marks:
  Official lab session_Name of any one team member as indicated exactly on the matriculation card_Matriculation number of Student A_ Matriculation number of Student B_Archive
  Example: Wednesday_AM_BELLE MONTEBELLO_A0053100B_ A0131026R_Archive.*xpr.zip*

5.2 ITEM B: REPORT SUBMISSION

- Include the following in your report (**One A4 size double-sided sheet at most for the report**):
  - ❖ Name and matriculation number of both students
    - Indicate who is Student A (Real-Time Audio Volume Indicator), and who is Student B (Graphical Visualisations and configurations)
  - ❖ Official lab session (Examples: Monday P.M., Wednesday P.M., Thursday A.M.) and group I.D.
    - Your group I.D. will be present in the document "*EE2026 Project Assessment Schedule.pdf*", and which will be uploaded at the end of week 11
  - ❖ Quick start / User guide which consists of:
    - Description of the features that you have designed and successfully implemented
    - Instructions on how these features can be operated by the user
      (Use the template provided on the next page)
    - Instructions may alternatively be described through flowcharts
  - ❖ Images must be in colour
  - ❖ Feedbacks. Possible topics include:
    - What did you like most / least about the project?
    - How would you suggest the overall project assignment be improved?
    - Any other constructive feedbacks / suggestions are welcome

    Note that feedbacks, whether positive or negative, **DO NOT** have any effects on your grades 😊
  - ❖ References:
    - Include references to open sources codes
    - Plagiarism penalties apply for open source codes that are not properly referenced

- Name your report submission in the format indicated below to avoid losing marks (The one team member name MUST be the same as that indicated for the Project Archive):
  Official lab session_Name of any one team member as indicated exactly on the matriculation card_Matriculation number of Student A_ Matriculation number of Student B_Report
  Example: Wednesday_AM_BELLE MONTEBELLO_A0053100B_ A0131026R_Report.*pdf*

TEMPLATE FOR THE QUICK START / USER GUIDE

Ensure that your quick start / user guide has the following 5 columns (There is no need to include the instructions found on the second row):

Feature	Feature Marks For	Input Devices	Feature Description	Images / Photos
Brief feature name. Features not indicated here will not be evaluated	Claim the feature marks for: - Student A **OR** - Student B **OR** - Team marks Improvement marks consist of 5% individual marks, and 10% team marks. **Your team** is responsible in **deciding** who will claim the marks	Indicate the input devices related to the feature. For examples: - SW0 - PBC - Character "X' on keyboard - Left mouse button	Indicate how to use the feature, and the expected effect that would be observed. The instructions should be clear	Take pictures of your Basys 3 / OLED screen to support your features. Images that properly support your feature description will help you explain better
Real-time audio volume indicator	Remy	SW0 …	**SW0 is 0:** mic_in shown on 12 LEDs **SW0 is 1:** Peak intensity shown on 16 LEDs …	
Graphical visualisations and configurations	Belle	SW3, SW4, SW5, SW6 …	**SW3, SW4:** 1 pixel thick border if 2'b01, 3 pixels thick border if 2'b10 **SW5, SW6:** Colour theme …	
"Name of improvement 1"	Remy	PBL	…	…
"Name of improvement 2"	Belle	SW7	…	
"Name of improvement 3"	Belle	SW8	…	…
"Name of improvement 4"	Team	PBU, PBD	…	…
"Name of improvement 5"	Team	SW9, SW10	…	
"Name of improvement 6"	Team	PBC, SW11	…	

- HIGHLIGHT THE BACKGROUND COLOUR OF TASKS WHOSE MARKS ARE CLAIMED BY **STUDENT A IN PASTEL BLUE**
- HIGHLIGHT THE BACKGROUND COLOUR OF TASKS WHOSE MARKS ARE CLAIMED BY **STUDENT B IN PASTEL GREEN**
- HIGHLIGHT THE BACKGROUND COLOUR OF TASKS WHOSE MARKS ARE CLAIMED BY **THE TEAM IN PASTEL PINK**

Each distinct improvement can only be claimed once, either for the individual component, OR for the team component

Bring **TWO printed copies** of your report in **COLOUR**, when you come for your assessment