## EE2026 Lab 3 pg 12

case hint example explanation

```
always @ (posedge clk 25 mhz)
begin
   case (counter value)
      2'd0:
         begin
                my value a \leq 20;
                                    This begin and end
                my value b <= 40;
         end
                                     defines the start and
      2'd1:
         begin
                                     end of the always block.
                my value a \leq 100;
                my value b \le 200;
         end
      2'd2: my value c <= 5;
      default: my value d <= 9;
   endcase 🐇
end
```

always block

```
always @ (posedge clk 25 mhz)
begin
   case (counter value)
      2'd0:
          begin
                 my value a \leq 20;
                 my_value_b <= 40;
          end
       2'd1:
          begin
                 my value a \leq 100;
                 my value b \le 200;
          end
       2'd2: my_value c <= 5;
       default: my_value_d <= 9;
   endcase
end
```



At each rising edge of this signal (clk\_25\_mhz), this block of code is executed once.

```
always @ (posedge clk 25 mhz)
begin
   case (counter value)
      2'd0:
          begin
                 my value a \leq 20;
                 my value b <= 40;
          end
       2'd1:
          begin
                 my_value a <= 100;
                 my value b \le 200;
          end
       2'd2: my_value_c <= 5;
       default: my value d <= 9;
   endcase
end
```

This is the case statement.

It starts with case and ends
with endcase.

```
always @ (posedge clk 25 mhz)
begin
   case (counter value)
        d0:
          begin
                  my value a \leq 20;
                  my value b \leq 40;
           end
       2'd1:
           begin
                  my value a \leq 100;
                  my value b \le 200;
           end
       2'd2: my value c <= 5;
       default: my value d <= 9;
   endcase
```

counter\_value is a 2-bit register with 4 possible decimal values 0, 1, 2, 3.

```
(posedge clk 25 mhz)
always @
begin
   case (counter value)
           begin
                  my_value_a <= 20;
my_value_b <= 40;</pre>
           end 📛
       2'd1:
           begin
                  my value a \leq 100;
                  my value b \le 200;
           end
       2'd2: my value c <= 5;
       default: my value d <= 9;
   endcase
```

If counter\_value is 0, these two lines of code in 1 will run.

After the codes are executed, we will skip the rest of the lines of code and go to endcase.

```
always @ (posedge clk 25 mhz)
begin
    case (counter value)
       2'd0:
            begin
                    my_value_a <= 20;
my_value_b <= 40;</pre>
            end
            begin —
                    my_value_a <= 100;
my_value_b <= 200;</pre>
        2'd2: my value c <= 5;
        default: my_value_d <= 9;
    endcase
```

If counter\_value is 1, the two
lines of code in 2 will run.

The rest of the code is skipped.

```
always @ (posedge clk 25 mhz)
begin
    case (counter value)
       2'd0:
            begin
                    my_value_a <= 20;
my_value_b <= 40;</pre>
            end
        2'd1:
            begin
                    my_value_a <= 100;
my_value_b <= 200;</pre>
            end
        2'd2: my value c <=
        default: my value d <= 9;
    endcase
```

If counter\_value is 1, the two
lines of code in 2 will run.

The rest of the code is skipped.

If counter\_value is 2, 3 will
run.

```
(posedge clk 25 mhz)
begin
    case (counter value)
             begin
                     my_value_a <= 20;
my_value_b <= 40;</pre>
             end
        2'd1:
             begin
                     my_value_a <= 100;
my_value_b <= 200;</pre>
        2'd2: my value c <=
        default: my_value_d <= 9;
    endcase
```

If counter\_value is 3, as it is not specified as one of the cases, the default case is executed and 4 is run.

The default case catches all undefined values. (eg. don't cares, X, and Z)