[Figures]

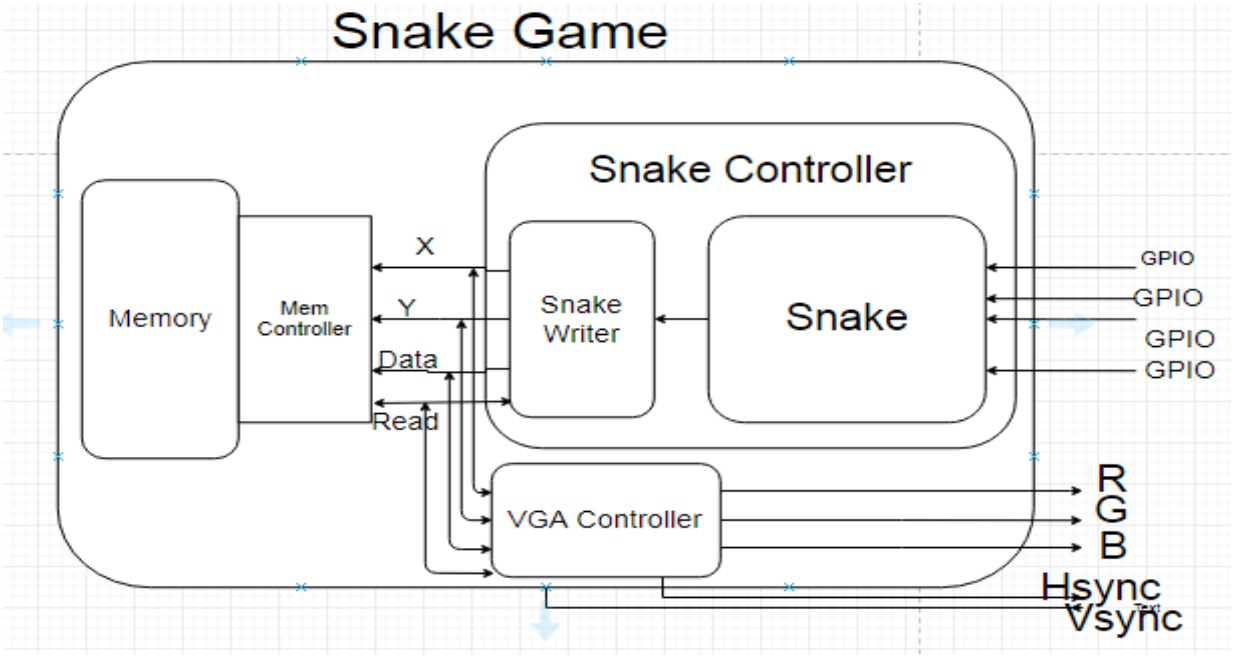

Figure 1: Block Diagram of Snake components complete with memory, four GPIO inputs and VGA output.

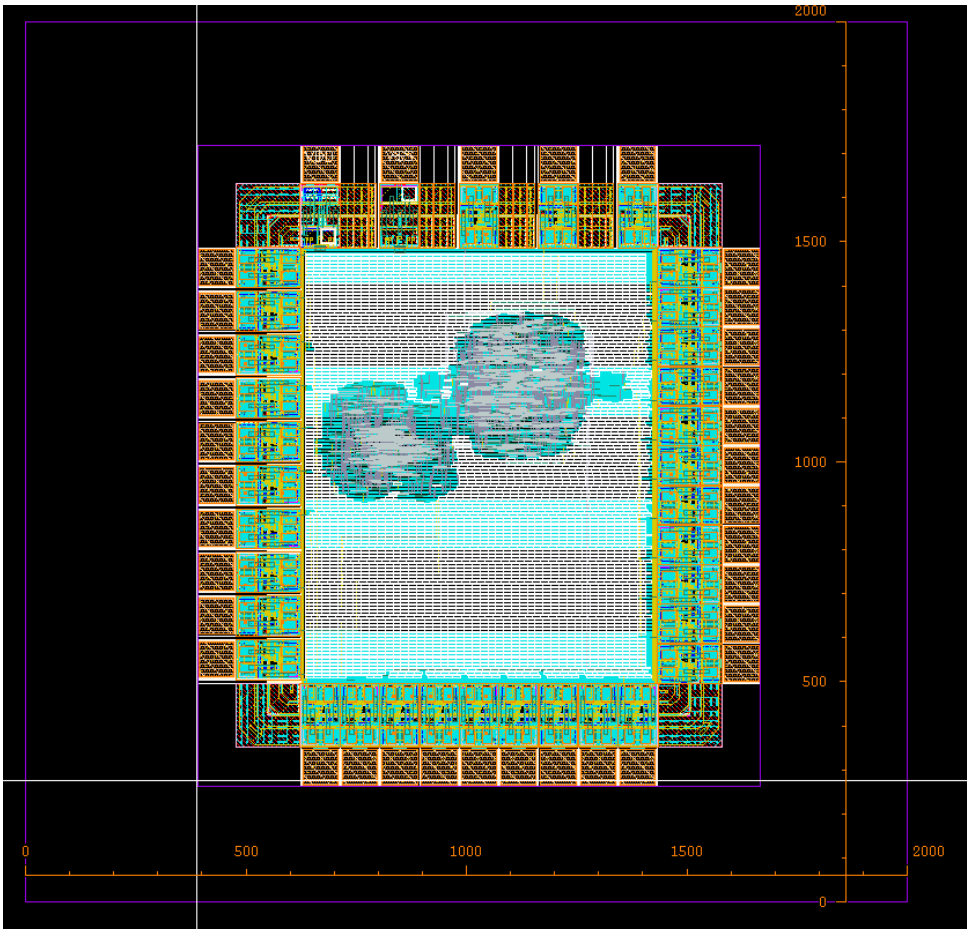

Fig. 2: Final Integrated Circuit Layout including measurements to show area constraints.

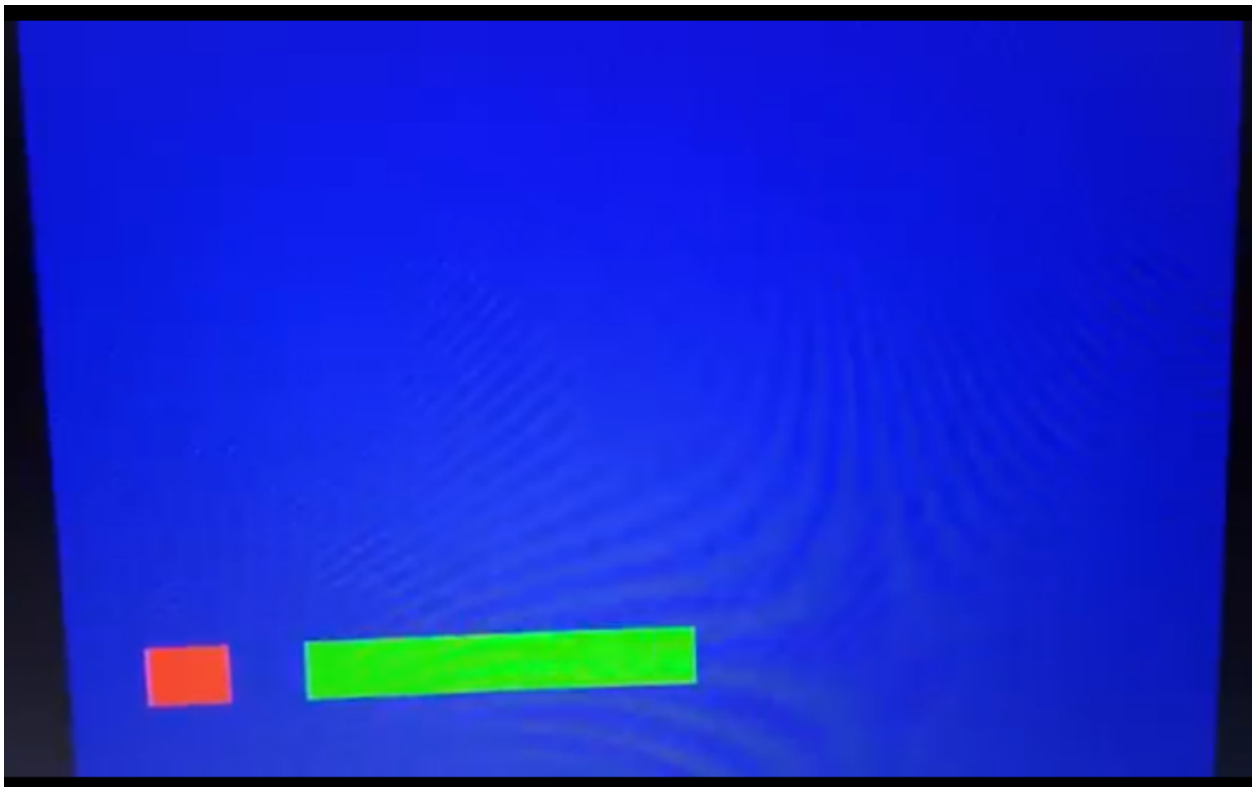

Fig 3: This is an example of the actual Snake Game VGA output from an FPGA.

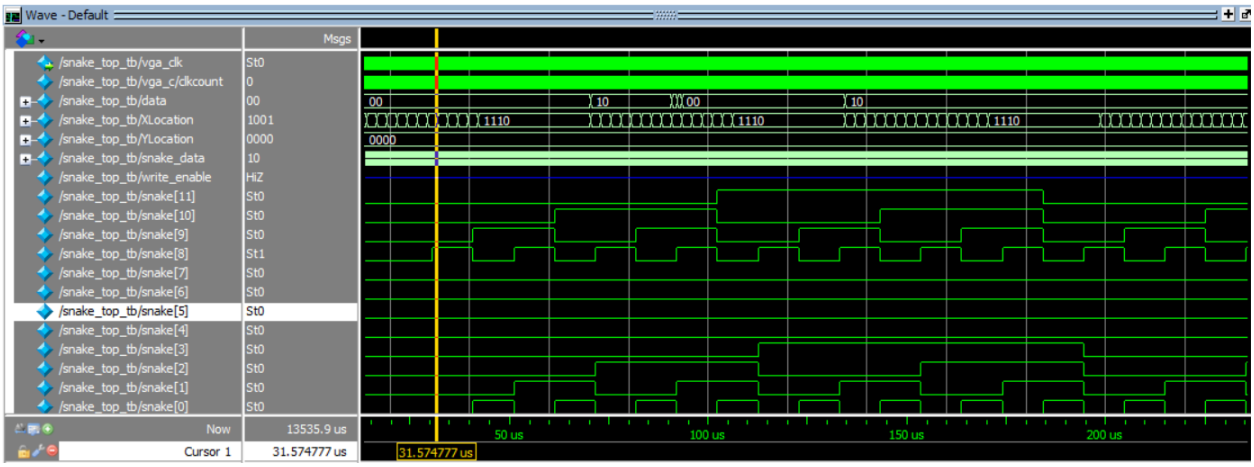

Fig 4: Modelsim simulation of top verilog module

```
****************************************
Report : area
Design : snake_top
Version: K-2015.06-SP5-6
Date   : Thu Nov 29 18:44:42 2018
****************************************

Library(s) Used:

    sclib_tsmc180_tt (File: /research/ece/lnis-teaching/Designkit

Number of ports:                         3911
Number of nets:                         70054
Number of cells:                        66210
Number of combinational cells:          63743
Number of sequential cells:              2457
Number of macros/black boxes:               0
Number of buf/inv:                       5039
Number of references:                      13

Combinational area:            838393.873064
Buf/Inv area:                   42343.723297
Noncombinational area:         131040.975578
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:               969434.848642
Total area:                 undefined
```

Figure 5: Area Report for synthesized design

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : snake_top
Version: K-2015.06-SP5-6
Date   : Sat Dec  1 15:27:50 2018
****************************************
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  sw/y_loc_reg[0]/CLK (DFFQX1)                            0.00       0.00 r
  sw/y_loc_reg[0]/Q (DFFQX1)                              0.21       0.21 f
  sw/y_loc[0] (snakeWriter)                               0.00       0.21 f
  mem/y_loc_sw[0] (memory)                                0.00       0.21 f
  mem/mult_102_S2/B[0] (memory_DW02_mult_0)               0.00       0.21 f
  mem/mult_102_S2/U31/Z (XOR2X1)                          0.25       0.46 r
  mem/mult_102_S2/U2/Z (INVX2)                            0.06       0.52 f
  mem/mult_102_S2/U28/Z (AND2X1)                          0.10       0.62 f
  mem/mult_102_S2/U27/Z (MUX2X1)                          0.20       0.82 f
  mem/mult_102_S2/PRODUCT[2] (memory_DW02_mult_0)         0.00       0.82 f
  mem/add_102_S2/A[2] (memory_DW01_add_0)                 0.00       0.82 f
  mem/add_102_S2/U20/Z (OR2X1)                            0.09       0.91 f
  mem/add_102_S2/U19/Z (NAND2X1)                          0.06       0.97 r
  mem/add_102_S2/U18/Z (NAND2X1)                          0.05       1.02 f
  mem/add_102_S2/U6/Z (INVX2)                             0.07       1.09 r
  mem/add_102_S2/U11/Z (NAND3X1)                          0.17       1.43 r
  mem/add_102_S2/U5/Z (NOR2X1)                            0.06       1.50 f
  mem/add_102_S2/U4/Z (AND2X1)                            0.12       1.61 f
  mem/add_102_S2/SUM[8] (memory_DW01_add_0)               0.00       1.61 f
  mem/U3/Z (INVX4)                                        0.06       1.67 r
  mem/U2170/Z (AND2X1)                                    0.30       1.97 r
  mem/U79/Z (NAND2X1)                                     0.10       2.70 r
  mem/world_memory_reg[7][1]/D (DFFQX1)                   0.00       2.70 r
  data arrival time                                                  2.70

  clock clk (rise edge)                                  20.00      20.00
  clock network delay (ideal)                             0.00      20.00
  mem/world_memory_reg[7][1]/CLK (DFFQX1)                 0.00      20.00 r
  library setup time                                     -0.09      19.91
  data required time                                                19.91
  -----------------------------------------------------------------------------
  data required time                                                19.91
  data arrival time                                                 -2.70
  -----------------------------------------------------------------------------
  slack (MET)                                                       17.21
```

Figure 6 :Timing Report for synthesized design

```
****************************************
Report : power
        -analysis_effort low
Design : snake_top
Version: K-2015.06-SP5-6
Date   : Sat Dec  1 15:27:50 2018
****************************************

Global Operating Voltage = 1.8
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 362.1260 uW   (90%)
  Net Switching Power  =  42.2092 uW   (10%)
                         ---------
Total Dynamic Power    = 404.3352 uW  (100%)

Cell Leakage Power     = 254.1322 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000           0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000           0.0000  (   0.00%)
register           0.2809        5.4357e-04           73.5050           0.2815  (  69.58%)
sequential     4.5076e-02           0.0000           25.1144       4.5101e-02  (  11.15%)
combinational  3.6145e-02        4.1666e-02         155.5129       7.7966e-02  (  19.27%)
--------------------------------------------------------------------------------------------------
Total              0.3621 mW     4.2209e-02 mW       254.1322 nW        0.4046 mW
1
```

Figure 7: Power report synthesized design