Computer Organization Lab 5

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1. Memory Stall Cycles

Operation	abbreviation	Delay(cycle)
Send the address	t_{sa}	1
Access single cache content	t_{asc}	2
Access L1 cache content	t_{a1c}	1
Access L2 cache content	t_{a2c}	10
Access memory content	t_{am}	100
Send a word of data	t_{sw}	1

1.1 One-word-wide memory organization

$t_{\text{hit penalty}} = t_{sa} + t_{asc} + t_{sw} = 4_{\text{cycles}}$

$t_{\text{miss penalty}} = t_{sa} + 8 * (t_{sa} + t_{am} + t_{sw} + t_{asc}) + t_{asc} + t_{sw} = 836_{\text{cycles}}$

1.2 Wider memory organization

$t_{\text{hit penalty}} = t_{sa} + t_{asc} + t_{sw} = 4_{\text{cycles}}$

$t_{\text{miss penalty}} = t_{sa} + 8 * (t_{sa} + t_{am} + t_{sw} + t_{asc}) / 8 + t_{asc} + t_{sw} = 108_{\text{cycles}}$

bandwidth = 8表示一次可以搬移8 words, 多一個 / 8 。

1.3 Two-level memory organization

$t_{\text{hit penalty}} = t_{sa} + t_{a1c} + t_{sw} = 3_{\text{cycles}}$

$t_{\text{L1 cache miss penalty}} = t_{sa} + 4 * (t_{sa} + t_{a2c} + t_{sw} + t_{a1c}) + t_{asc} + t_{sw} = 55_{\text{cycles}}$

$t_{\text{L2 cache miss penalty}} = t_{sa} + 4 * (t_{sa} + t_{a2c} + t_{sw} + t_{a1c}) + 32 * (t_{sa} + t_{am} + t_{sw} + t_{a2c}) + t_{asc} + t_{sw} = 3639_{\text{cycles}}$