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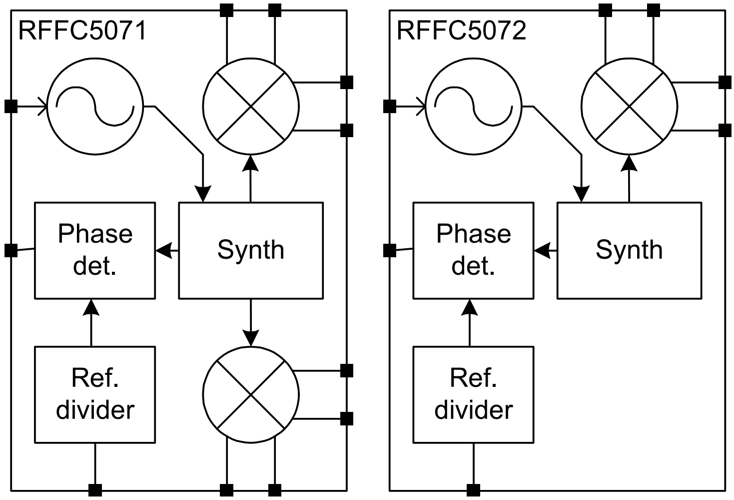
RFFC5071/5072

WIDEBAND SYNTHESIZER/VCO WITH INTEGRATED 6GHz MIXER

Package: QFN, 32-Pin, 5mmx5mm



Functional Block Diagram

Features

- 85MHz to 4200MHz LO Frequency Range
- Fractional-N Synthesizer with Very Low Spurious Levels
- Typical Step Size 1.5Hz
- Fully Integrated Low Phase Noise VCO and LO Buffers
- Integrated Phase Noise
  - 0.18° rms at 1 GHz
  - 0.50° rms at 3GHz
- High Linearity RF Mixer(s)
- 30MHz to 6000MHz Mixer Frequency Range
- Input IP3 +23dBm
- Mixer Bias Adjustable for Low Power Operation
- Full Duplex Mode (RFFC5071)
- 2.7V to 3.3V Power Supply
- Low Current Consumption
- 3- or 4-Wire Serial Interface

Applications

- Wideband Radios
- Distributed Antenna Systems
- Diversity Receivers
- Software Defined Radios
- Frequency Band Shifters
- Point-to-Point Radios
- WiMax/LTE Infrastructure
- Satellite Communications
- Wideband Jammers

Product Description

The RFFC5071 and RFFC5072 are re-configurable frequency conversion devices with integrated fractional-N phased locked loop (PLL) synthesizer, voltage controlled oscillator (VCO) and either one or two high linearity mixers. The fractional-N synthesizer takes advantage of an advanced sigma-delta modulator that delivers ultra-fine step sizes and low spurious products. The PLL/VCO engine combined with an external loop filter allows the user to generate local oscillator (LO) signals from 85MHz to 4200MHz. The LO signal is buffered and routed to the integrated RF mixers which are used to up/down-convert frequencies ranging from 30MHz to 6000MHz. The mixer bias current is programmable and can be reduced for applications requiring lower power consumption. Both devices can be configured to work as signal sources by bypassing the integrated mixers. Device programming is achieved via a simple 3-wire serial interface. In addition, a unique programming mode allows up to four devices to be controlled from a common serial bus. This eliminates the need for separate chip-select control lines between each device and the host controller. Up to six general purpose outputs are provided, which can be used to access internal signals (e.g. the LOCK signal) or to control front end components. Both devices operate with a 2.7V to 3.3V power supply.

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ BiFET HBT
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{DD})	-0.5 to +3.6	V
Input Voltage (V_{IN}) any pin	-0.3 to V_{DD}+0.3	V
RF/IF mixer input power	+15	dBm
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-40 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
ESD Requirements					
Human Body Model	2000			V	DC Pins
	1500			V	All Pins
Charge Device Model	500			V	All Pins
Operating Conditions					
Supply voltage (V_{DD})	2.7	3.0	3.3	V	
Temperature (T_{OP})	-40		+85	°C	
Logic Inputs/Outputs (V_{DD}**=Supply to DIG_VDD pin)**					
Input low voltage	-0.3		+0.5	V	
Input high voltage	1.5		V_{DD}	V	
Input low current	-10		+10	μA	Input=0V
Input high current	-10		+10	μA	Input=V_{DD}
Output low voltage	0		0.2*V_{DD}	V	
Output high voltage	0.8*V_{DD}		V_{DD}	V	
Load resistance	10			kΩ	
Load capacitance			20	pF	
GPO Drive Capability					
Sink Current		20		mA	At V_{OL} = +0.6V
Source Current		20		mA	At V_{OL} = +2.4V
Output Impedance		25		Ω	
Static					
Supply Current (I_{DD}) with 1GHz LO		100		mA	Low current, MIX_IDD=1, one mixer enabled.
		125		mA	High linearity, MIX_IDD=6, one mixer enabled.
Standby			2	mA	Reference oscillator and bandgap only.
Power Down Current			300	μA	ENBL=0 and REF_STBY=0
Mixer 1/2 (Mixer output driving 4:1 balun)					
Gain		-2		dB	Not including balun losses
Noise Figure <3000MHz		10		dB	Low current setting
		13		dB	High linearity setting
Noise Figure <4000MHz		11		dB	Low current setting
		15		dB	High linearity setting

Mixer 1/2 (Mixer output driving 4:1 balun) (continued)					
IIP3		+10		dBm	Low current setting
		+23		dBm	High linearity setting
Input Port Frequency range	30		6000	MHz	
Mixer input return loss		10		dB	100Ω differential
Output port frequency range	30		4500	MHz	
Mixer 1/2 (Mixer output driving 1:1 balun)					
Output Port Frequency Range	30		6000	MHz	
Gain		-7		dB	Not including balun losses
Reference Oscillator					
External reference frequency	10		104	MHz	
Reference divider ratio	1		7		
External reference input level	500	800	1500	mVp-p	AC-coupled
Synthesizer (PLL Closed Loop, 52MHz)					
Synthesizer Output Frequency	85		4200	MHz	
Phase detector frequency			52	MHz	
Phase noise (LO=1GHz)		-108		dBc/Hz	10kHz offset
		-108		dBc/Hz	100kHz offset
		-135		dBc/Hz	1MHz offset
		0.19		°	RMS integrated from 1kHz to 40MHz
Phase noise (LO=2GHz)		-102		dBc/Hz	10kHz offset
		-102		dBc/Hz	100kHz offset
		-130		dBc/Hz	1MHz offset
		0.32		°	RMS integrated from 1kHz to 40MHz
Phase noise (LO=3GHz)		-97		dBc/Hz	10kHz offset
		-97		dBc/Hz	100kHz offset
		-124		dBc/Hz	1MHz offset
		0.50		°	RMS integrated from 1kHz to 40MHz
Phase noise (LO=4GHz)		-95		dBc/Hz	10kHz offset
		-96		dBc/Hz	100kHz offset
		-124		dBc/Hz	1MHz offset
		0.61		°	RMS integrated from 1kHz to 40MHz
Normalized phase noise floor		-214		dBc/Hz	Measured at 20kHz to 30kHz offset
Voltage Controlled Oscillator					
Open loop phase noise at 1MHz offset					
2.5GHz LO frequency		-134		dBc/Hz	VCO3, LO Divide by 2
2.0GHz LO frequency		-135		dBc/Hz	VCO2, LO Divide by 2
1.5GHz LO frequency		-136		dBc/Hz	VCO1, LO Divide by 2
Open loop phase noise at 10MHz offset					
2.5GHz LO frequency		-149		dBc/Hz	VCO3, LO Divide by 2
2.0GHz LO frequency		-150		dBc/Hz	VCO2, LO Divide by 2
1.5GHz LO frequency		-151		dBc/Hz	VCO1, LO Divide by 2
External LO Input					
LO Input Frequency Range	85		4200	MHz	LO Divide by 1
LO Input Frequency Range	85		5400	MHz	LO Divide by 2
External LO Input Level		0		dBm	Driven from 50Ω Source Via a 1:1 Balun

Pin	Function	Description
1	ENBL/GPO5	Device Enable pin (see note 1 and 2).
2	EXT_LO	External local oscillator input (See note 4).
3	EXT_LO_DEC	Decoupling pin for external local oscillator (See note 4).
4	REXT	External bandgap bias resistor (See note 3).
5	ANA_VDD1	Analog supply. Use good RF decoupling.
6	LFILT1	Phase detector output. Low-frequency noise-sensitive node.
7	LFILT2	Loop filter op-amp output. Low-frequency noise-sensitive node.
8	LFILT3	VCO control input. Low-frequency noise-sensitive node.
9	MODE/GPO6	Mode select pin (See note 1 and 2).
10	REF_IN	Reference input. Use AC coupling capacitor.
11	NC	
12	TM	Connect to ground.
13	MIX1_IPN	Differential input 1 (see note 4). On RFFC5072 this pin is NC.
14	MIX1_IPP	Differential input 1 (see note 4). On RFFC5072 this pin is NC.
15	GPO1/ADD1	General purpose output / MultiSlice address bit.
16	GPO2/ADD2	General purpose output / MultiSlice address bit.
17	MIX1_OPN	Differential output 1 (see note 5). On RFFC5072 this pin is NC.
18	MIX1_OPP	Differential output 1 (see note 5). On RFFC5072 this pin is NC.
19	DIG_VDD	Digital supply. Should be decoupled as close to the pin as possible.
20	NC	
21	NC	
22	ANA_VDD2	Analog supply. Use good RF decoupling.
23	MIX2_IPP	Differential input 2 (see note 4).
24	MIX2_IPN	Differential input 2 (see note 4).
25	GPO3/FM	General purpose output / frequency control input.
26	GPO4/LD/DO	General purpose output / Lock detect output / serial data out.
27	MIX2_OPN	Differential output 2. (see note 5).
28	MIX2_OPP	Differential output 2. (see note 5).
29	RESETX	Chip reset (active low). Connect to DIG_VDD if asynchronous reset is not required.
30	ENX	Serial interface select (active low) (See note 1).
31	SCLK	Serial interface clock (see note 1).
32	SDATA	Serial interface data (see note 1).
Exposed paddle		Ground reference, should be connected to PCB ground through a low impedance path.

Note 1: An RC low-pass filter could be used on this line to reduce digital noise.

Note 2: If the device is under software control this input can be configured as a general purpose output (GPO).

Note 3: Connect a 51KΩ resistor from this pin to ground. This pin is sensitive to low frequency noise injection.

Note 4: DC voltage should not be applied to this pin. Use either an AC coupling capacitor as part of lumped element matching network or a transformer (see application schematic).

Note 5: This pin must be connected to ANA_VDD2 using an RF choke or transformer (see application schematic).

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Theory of Operation

The RFFC5071 and RFFC5072 are wideband RF frequency converter chips which include a fractional-N synthesizer and a low noise VCO core. The RFFC5071 has an LO signal multiplexer, two LO buffer circuits, and two RF mixers. The RFFC5072 has a single LO buffer circuit and one RF mixer. Both devices have an integrated voltage reference and low drop out regulators supplying critical circuit blocks such as the VCOs and synthesizer. Synthesizer programming, device configuration and control are achieved through a mixture of hardware and software controls. All on-chip registers are programmed through a simple 3-wire serial interface.

VCO

The VCO core in the RFFC5071 and RFFC5072 consists of three VCOs which, in conjunction with the integrated LO dividers of /2 to /32, cover the LO range of 85MHz to 4200MHz. Each VCO has 128 overlapping bands which are used to achieve low VCO gain and optimal phase noise performance across the whole tuning range. The chip automatically selects the correct VCO (VCO auto-select) and VCO band (VCO coarse tuning) to generate the desired LO frequency based on the values programmed into the PLL1 and PLL2 registers banks.

The VCO auto-select and VCO coarse tuning are triggered every time ENBL is taken high, or if the PLL re-lock self clearing bit is programmed high. Once the correct VCO and band have been selected the PLL will lock onto the correct frequency. During the band selection process, fixed capacitance elements are progressively connected to the VCO resonant circuit until the VCO is oscillating approximately at the correct frequency. The output of this band selection, CT_CAL, is made available in the read-back register. A value of 127 or 0 in this register indicates that the coarse tuning was unsuccessful, and this will also be indicated by the CT_FAILED flag also available in the read-back register. A CT_CAL value between 1 and 126 indicates a successful calibration, the actual value being dependent on the desired frequency as well as process variation for a particular device.

The band select process will center the VCO tuning voltage at about 1.0V, compensating for manufacturing tolerances and process variation as well as environmental factors including temperature. In applications where the device is left enabled at the same LO frequency for some time, it is recommended that automatic band selection be performed for every 30°C change in temperature. This assumes an active loop filter.

The RFFC5071 and RFFC5072 feature a differential LO input to allow the mixer to be driven from an external LO source. The fractional-N PLL can be used with an external VCO driven into this LO input, which may be useful to reduce phase noise in some applications. This may also require an external op-amp, dependant on the tuning voltage required by the external VCO.

In the RFFC5071 the LO signal is routed to mixer 1, mixer 2, or both mixers depending on the state of the MODE pin (or MODE bit if under software control) and the value of the FULLD bit. Setting FULLD high puts the device into Full Duplex mode and both mixers are enabled.

Fractional-N PLL

The RFFC5071 and RFFC5072 contain a charge pump-based fractional-N phase locked loop (PLL) for controlling the three VCOs. The PLL includes automatic calibration systems to counteract the effects of process and environmental variations, ensuring repeatable loop response and phase noise performance. As well as the VCO auto-select and coarse tuning, there is a loop filter calibration mechanism which can be enabled if required. This operates by adjusting the charge pump current to maintain loop bandwidth. This can be useful for applications where the LO is tuned over a wide frequency range.

The PLL has been designed to use a reference frequency of between 10MHz and 104MHz from an external source, which is typically a temperature controlled crystal oscillator (TCXO). A reference divider (divide by 1 to divide by 7) is supplied and should be programmed to limit the frequency at the phase detector to a maximum of 52MHz.

Two PLL programming banks are provided, the first bank is preceded by the label PLL1 and the second bank is preceded by the label PLL2. For the RFFC5071 these banks are used to program mixer 1 and mixer 2 respectively, and are selected automatically as the mixer is selected using MODE. For the RFFC5072 mixer 2 and register bank PLL2 are normally used.

The VCO outputs are first divided down in a high frequency prescalar. The output of this high frequency prescalar then enters the N divider, which is a fractional divider containing a dual-modulus prescaler and a digitally spur-compensated fractional sequence generator. This allows very fine frequency steps and minimizes fractional spurs. The fractional energy is randomized and appears as fractional noise at frequency offsets above 100kHz which will be attenuated by the loop filter. An external loop filter is used, giving flexibility in setting loop bandwidth for optimizing phase noise and lock time, for example.

The synthesizer step size is typically 1.5Hz when using a 26MHz reference frequency. The exact step size for any reference and LO frequency can be calculated using the following formula:

$(F_{REF} * P) / (R * 2^{24} * LO\_DIV)$

Where F_{REF} is the reference frequency, R is the reference division ratio, P is the prescalar division ratio, and LO_DIV is the LO divider value.

Pin 26 (GPO4) can be configured as a lock detect pin. The lock status is also available in the read-back register. The lock detect function is a window detector on the VCO tuning voltage. The lock flag will be high to show PLL lock which corresponds to the VCO tuning voltage being within the specified range, typically 0.30V to 1.25V.

The lock time of the PLL will depend on a number of factors; including the loop bandwidth and the reference frequency at the phase detector. This clock frequency determines the speed at which the state machine and internal calibrations run. A 52MHz phase detector frequency will give fastest lock times, of typically <50usecs when using the PLL re-lock bit.

Phase Detector and Charge Pump

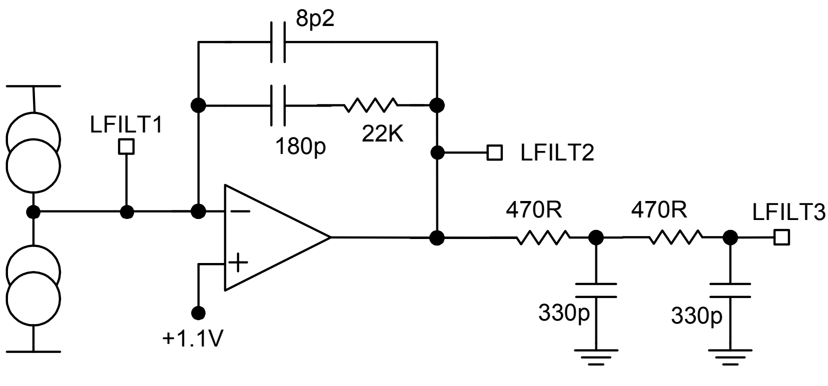
The phase detector provides a current output to drive an active loop filter. The charge pump output current is set by the value contained in the P1_CP_DEF and P2_CP_DEF fields in the loop filter configuration register. The charge pump current is given by approximately 3uA/bit, and the fields are 6 bits long. This gives default value (31) of 93uA and maximum value (63) of 189uA.

If the automatic loop bandwidth calibration is enabled the charge pump current is set by the calibration algorithm based upon the VCO gain.

The phase detector will operate with a maximum input frequency of 52MHz.

Loop Filter

The active loop filter is implemented using the on-chip low noise op-amp with external resistors and capacitors. The internal configuration of the chip is shown below with the recommended active loop filter. The op-amp gives a tuning voltage range of typically +0.1V to +2.4V. The recommended loop filter shown is designed to give the lowest integrated phase noise for reference frequencies of 26MHz and 52MHz. The external loop filter gives the flexibility to optimize the loop response for any particular application and combination of reference and VCO frequencies.



External Reference

The RFFC5071 and RFFC5072 have been designed to use an external reference such as a TCXO. The typical input will be a 0.8Vp-p clipped sine wave, which should be AC-coupled into the reference input. When the PLL is not in use, it may be desirable to turn off the internal reference circuits, by setting the REFSTBY bit low, to minimize current draw while in standby mode.

On cold start, or if REFSTBY is programmed low, the reference circuits will need a warm-up period. This is set by the SU_WAIT bits. This will allow the clock to be stable and immediately available when the ENBL bit is asserted high, allowing the PLL to assume normal operation.

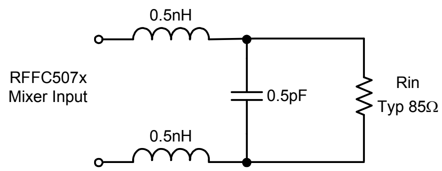
If the current consumption of the reference circuits in standby mode, typically 2mA, is not critical, then the REFSTBY bit can be set high. This allows the fastest startup and lock time after ENBL is taken high.

Wideband Mixer

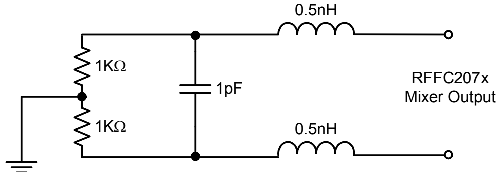
The mixers are wideband, double-balanced Gilbert cells. They support RF/IF frequencies from 30MHz up to 6000MHz. Each mixer has an input port and an output port that can be used for either IF or RF (in other words, for up- or down-conversion). The mixer current can be programmed to between about 15mA and 45mA depending on linearity requirements. The majority of the mixer current is sourced through the output pins via either a center-tapped balun or an RF choke in the external matching circuitry to the supply.

The RF mixer input and output ports are differential and require baluns and simple matching circuits optimized to the specific application frequencies. A conversion gain of approximately -2dB (not including balun losses) is achieved with 100Ω differential input impedance, and the outputs driving 200Ω differential load impedance. Increasing the mixer output load increases the conversion gain.

The mixer has a broadband common gate input. The input impedance is dominated by the resistance set by the mixer 1/gm term, which is inversely proportional to the mixer current setting. The resistance will be approximately 85Ω at the default mixer current setting (100). There is also some shunt capacitance at the mixer input, and the inductance of the bond wires (about 0.5nH on each pin) to consider at higher frequencies. The following diagram is a simple model of the mixer input impedance:



The mixer output is high impedance, consisting of approximately 2kΩ resistance in parallel with some capacitance, approximately 1pF dependent on PCB layout. The mixer output does not require a conjugate matching network. It is a constant current output which will drive a real differential load of between 50Ω and 500Ω, typically 200Ω. Since the mixer output is a constant current source, a higher resistance load will give higher output voltage and gain. A shunt inductor can be used to resonate with the mixer output capacitance at the frequency of interest. This inductor may not be required at lower frequencies where the impedance of the output capacitance is less significant. At higher output frequencies the inductance of the bond wires (about 0.5nH on each pin) becomes more significant. Above about 4500MHz, it is beneficial to lower the output load to 50Ω to minimize the effect of the ouput capacitance. The following diagram is a simple model of the mixer output:



The RFFC5071 mixer layout and pin placement has been optimized for high mixer-to-mixer isolation of greater than 60dB. The mixers can be set up to operate in half duplex mode (1 mixer active) or full duplex mode (both mixers active). This selection is done via control of MODE and by setting the FULLD bit. When in full duplex mode, either PLL register bank can be used, the LO signal is routed to both mixers.

Mode	FULLD	Active PLL Register Bank	Active Mixer
LOW	0	1	1
HIGH	0	2	2
LOW	1	1	1 and 2
HIGH	1	2	1 and 2

Serial Interface

All on-chip registers in the RFFC5071 and RFFC5072 are programmed using a proprietary 3-wire serial bus which supports both write and read operations. Synthesizer programming, device configuration, and control are achieved through a mixture of hardware and software controls. Certain functions and operations require the use of hardware controls via the ENBL, MODE, and RESETB pins in addition to programming via the serial bus. Alternatively there is the option to control the chip completely via the serial bus.

The serial data interface can be configured for 4-wire operation by setting the 4wire bit in the SDI_CTRL register high. Then pin 26 is used as the data out pin, and pin 32 is the serial data in pin.

Hardware Control

Three hardware control pins are provided: ENBL, MODE, and RESETB.

The ENBL pin has two functions: to enable the analog circuits in the chip and to trigger the VCO auto-selection and coarse tuning mechanisms. The VCO auto-selection and coarse tuning is initiated when the ENBL pin is taken high. Every time the frequency of the synthesizer is reprogrammed, ENBL has to be asserted high to initiate these mechanisms and then to initiate the PLL locking. Alternatively following the programming of a new frequency the PLL re-lock self clearing bit could be used.

If the device is left in the enabled state for long periods, it is recommended that VCO auto-selection and coarse tuning (band selection) is performed for every 30°C change in temperature. The lock detect flag can be used to indicate when to perform the VCO calibration, it shows that the VCO tuning voltage has drifted significantly with changing temperature.

The RESETB pin is a hardware reset control that will reset all digital circuits to their startup state when asserted low. The device includes a power-on-reset function, so this pin should not normally be required, in which case it should be connected to the positive supply.

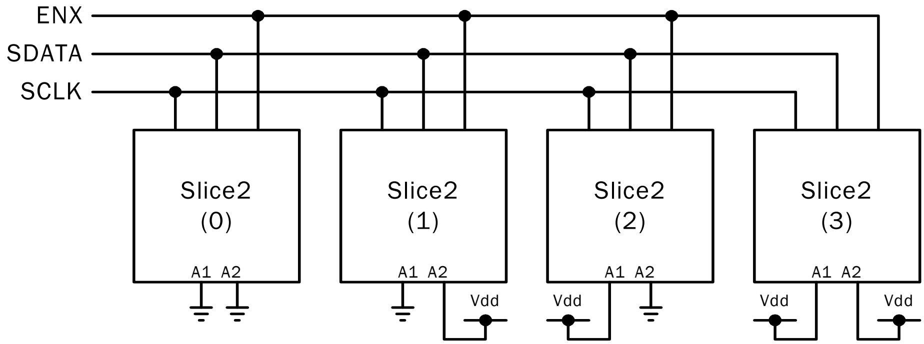
The MODE pin controls which mixer(s) and PLL programming register bank is active.

Serial Data Interface Control

The normal mode of operation uses the 3-wire serial data interface to program the device registers, and three extra hardware control lines: MODE, ENBL and RESETB.

When the device is under software control, achieved by setting the SIPIN bit in the SDI_CTRL register high, then the hardware can be controlled via the SDI_CTRL register. When this is the case, the three hardware control lines are not required. If the device is under software control, pins 1 and 9 can be configured as general purpose outputs (GPO).

Multi-Slice Mode



The Multi-Slice mode of operation allows up to four chips to be controlled from a common serial bus. The device address pins A0 and A1 are used to set the address of each part.

On power up, and after a reset, the devices ignore the address pins (A1 and A2, pins 15 and 16) and any data presented to the serial bus will be programmed into all the devices. However, once the sipin bit in the SDI_CTRL register is set, each device then adopts an address according to the state of the address pins on the device.

General Purpose Outputs

The general purpose outputs (GPOs) can be controlled via the GPO register and will depend on the state of MODE since they can be set in different states corresponding to either mixer path 1 or 2. For example, the GPOs can be used to drive LEDs or to control external circuitry such as switches or low power LNAs.

Each GPO pin can supply approximately 20mA load current. The output voltage of the GPO high state will drop with increased current drive by approximately 25mV/mA. Similarly the output voltage of the GPO low state will rise with increased current, again by approximately 25mV/mA.

External Modulation

The RFFC5071 and RFFC5072 fractional-N synthesizer can be used to modulate the frequency of the VCO. There are two dedicated registers, EXT_MOD and FMOD, which can be used to configure the device as a modulator. It is possible to modulate the VCO in two ways:

1.Binary FSK

The MODSETUP bits in the EXT_MOD register are set to 11. GPO3 is then configured as an input and used to control the signal frequency. The frequency deviation is set by the MODSTEP and MODULATION bits in the EXT_MOD and FMOD registers respectively.

The modulation frequency is calculated according to the following formula:

$$F_{MOD} = 2^{MODSTEP} \cdot F_{PD} \cdot (MODULATION)/2^{16}$$

Where MODULATION is a 2's complement number and F_{PD} is the phase detector frequency.

2.Continuous Modulation

The MODSETUP bits in the EXT_MOD register are set to 01. The frequency deviation is set by the MODSTEP and MODULATION bits in the EXT_MOD and FMOD registers respectively. The VCO frequency is then changed by writing a new value into the MOD-

ULATION bits, the VCO frequency is instantly updated. An arbitrary frequency modulation can then be performed dependant only on the rate at which values are written into the FMOD register.

The modulation frequency is calculated according to the following formula:

$$F_{MOD} = 2^{MODSTEP} \cdot F_{PD} \cdot (MODULATION)/2^{16}$$

Where MODULATION is a 2's complement number and F_{PD} is the phase detector frequency.

Programming Information

The RFFC5071 and RFFC5072 share a common serial interface and control block. Please refer to the Register Maps and Programming Guide which are available for download from http://rfmd.com/products/IntSynthMixer/.

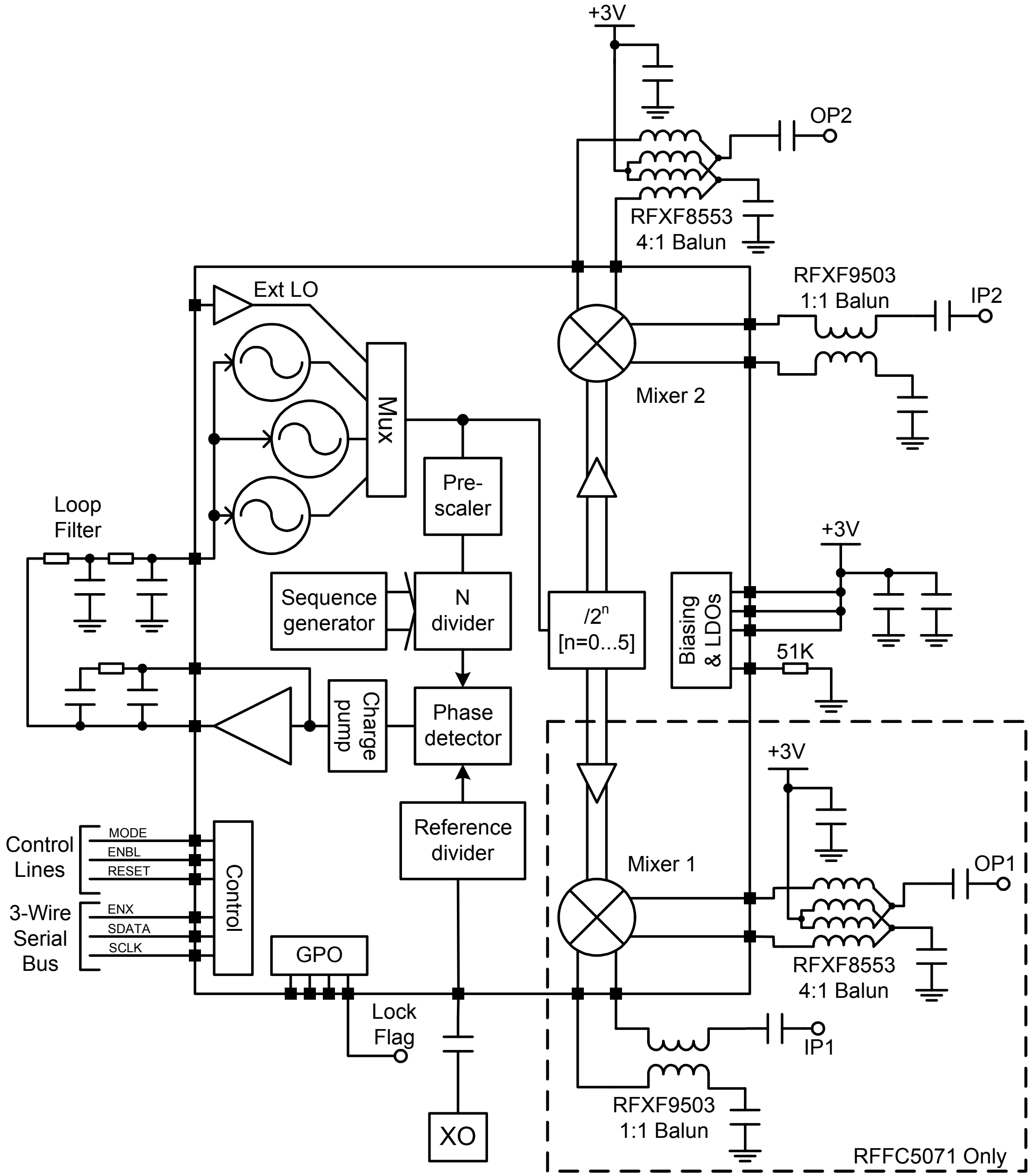
Evaluation Boards

Evaluation boards for RFFC5071 and RFFC5072 are provided as part of a design kit, along with the necessary cables and programming software tool to enable full evaluation of the device. Design kits can be ordered from www.rfmd.com or from local RFMD sales offices and authorized sales channels. For ordering codes please see “Ordering Information” on page 26.

For further details on how to set up the design kits go to http://rfmd.com/products/IntSynthMixer/.

The standard evaluation boards are configured with 3.7GHz ceramic baluns on the RF ports and wideband transformers on the IF ports. On the RFFC5071 evaluation board, mixer 1 is configured for down-conversion and mixer 2 is configured for up-conversion. On the RFFC5072 evaluation board, mixer 2 is configured for down conversion.

Detailed Functional Block Diagram



Note: Wideband transmission line transformer baluns shown above for operation to ~2.5GHz. Substitute baluns for higher frequency applications as required.

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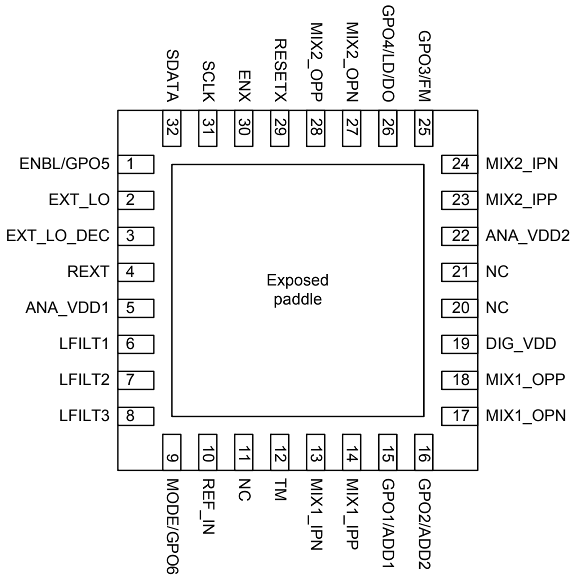
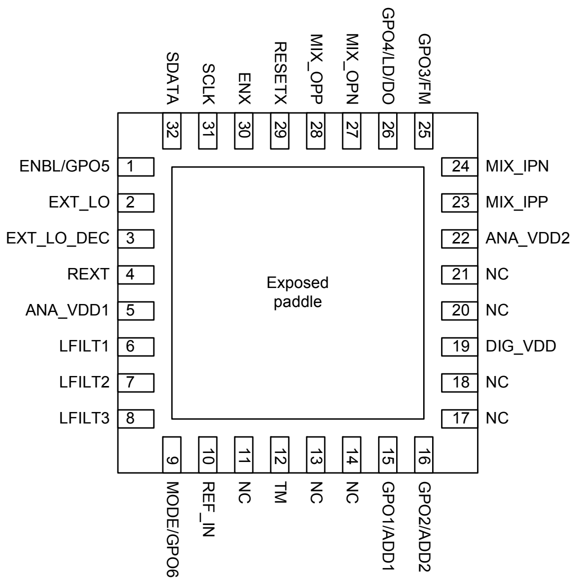
RFFC5071 Pin Out



RFFC5072 Pin Out



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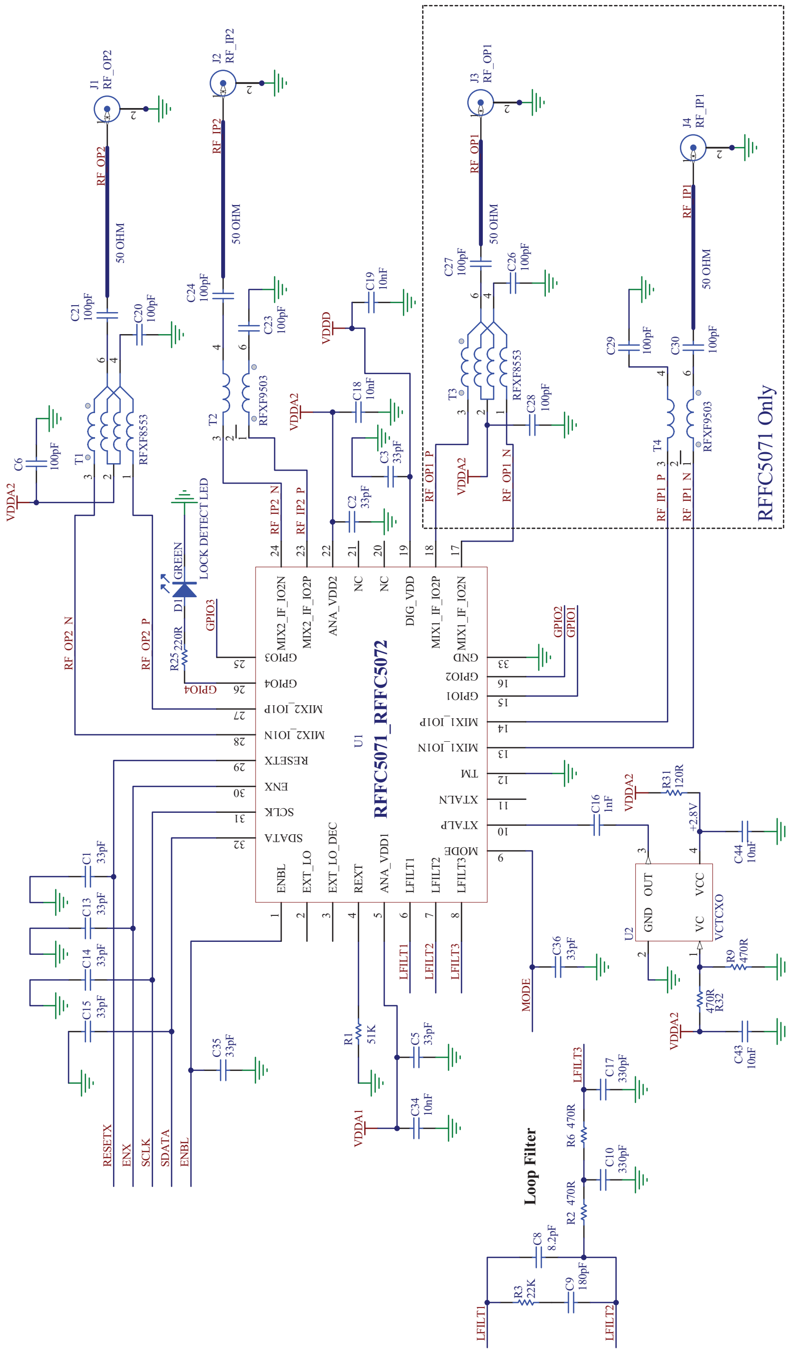
Wideband Application Schematic (<2.5GHz)



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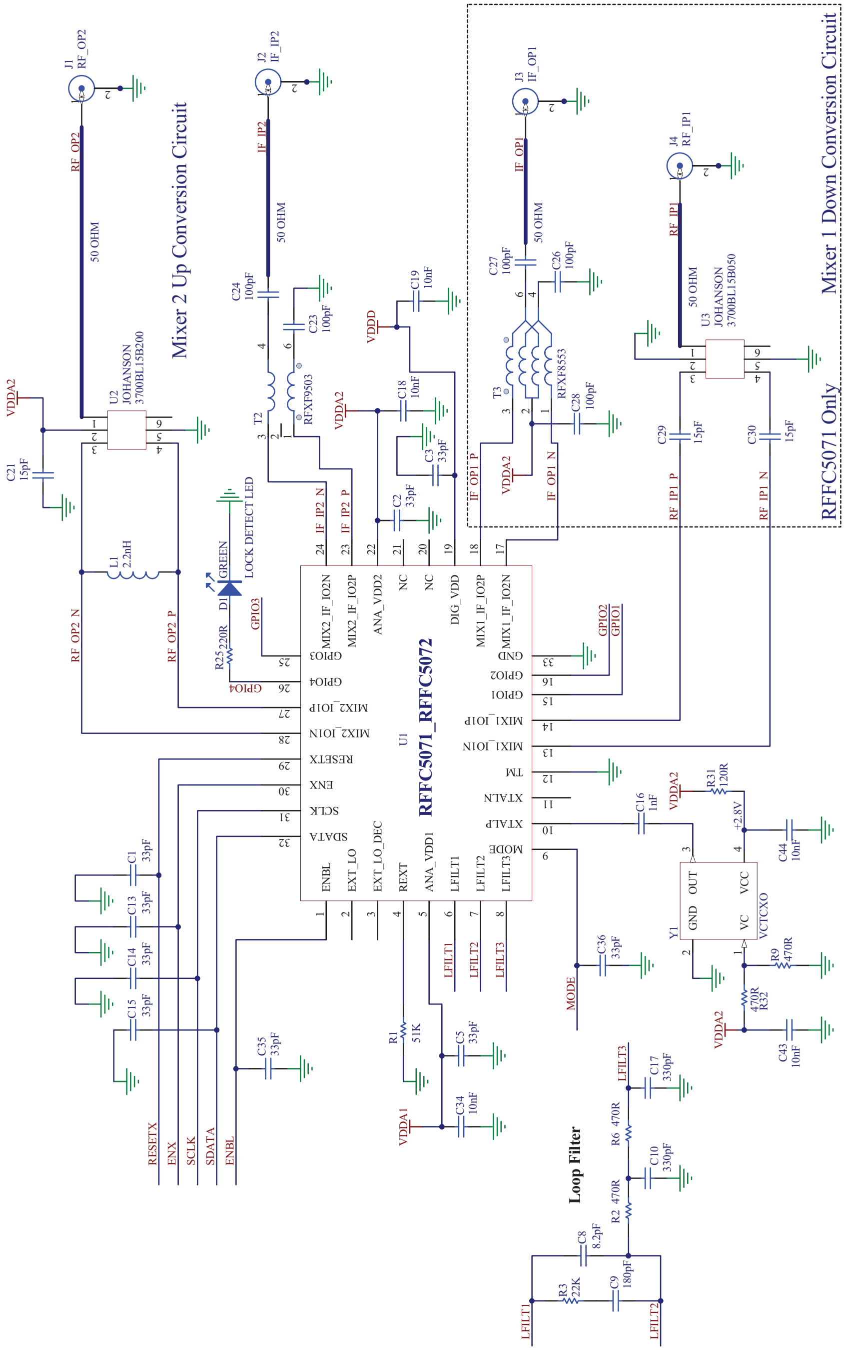
Narrowband 3.7 GHz Application Schematic



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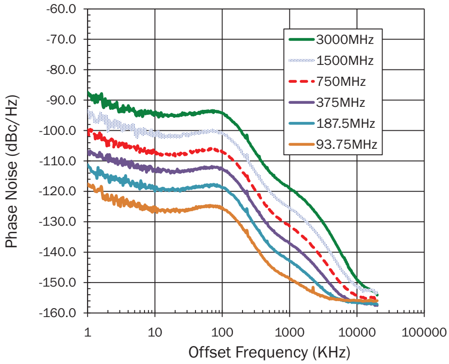
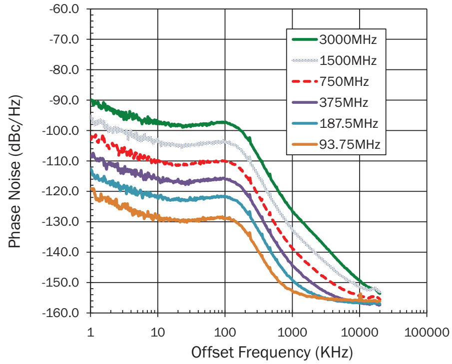
Typical Performance Characteristics: Synthesizer

V_{DD}=+3V and T_A=+27°C unless stated.

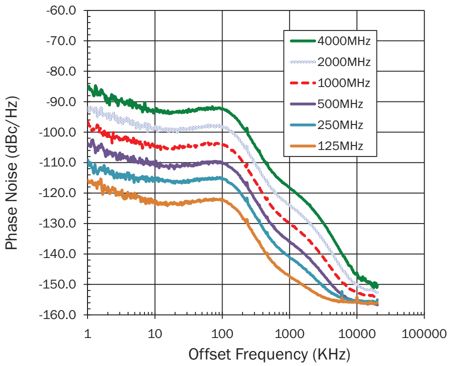
Synthesizer Phase Noise
3000MHz VCO Frequency, 26MHz Crystal Oscillator



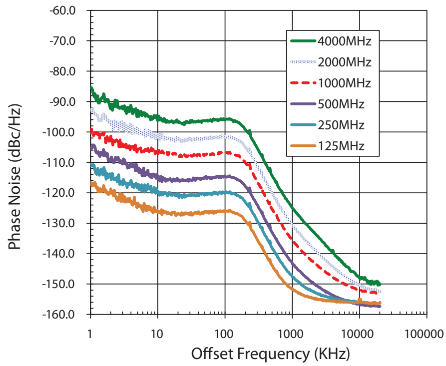
Synthesizer Phase Noise
3000MHz VCO Frequency, 52MHz Crystal Oscillator



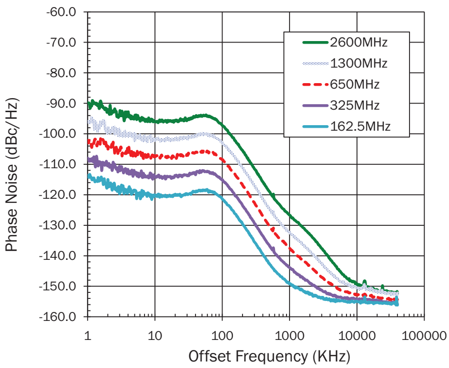
Synthesizer Phase Noise
4000MHz VCO Frequency, 26MHz Crystal Oscillator



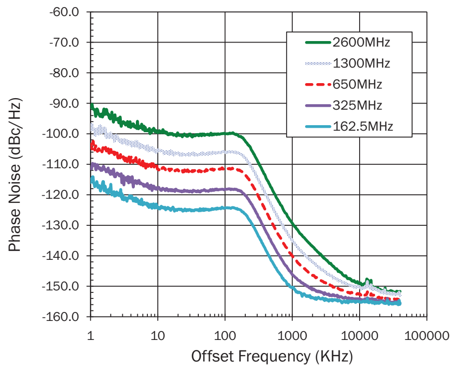
Synthesizer Phase Noise
4000MHz VCO Frequency, 52MHz Crystal Oscillator



Synthesizer Phase Noise
5200MHz VCO Frequency, 26MHz Crystal Oscillator

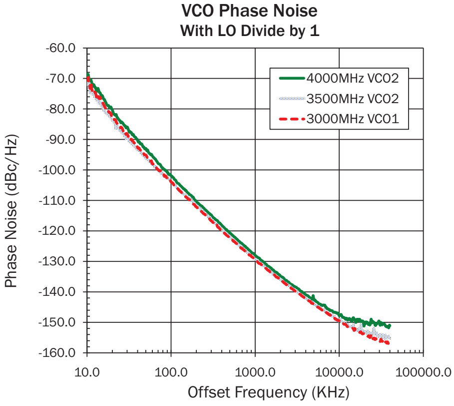


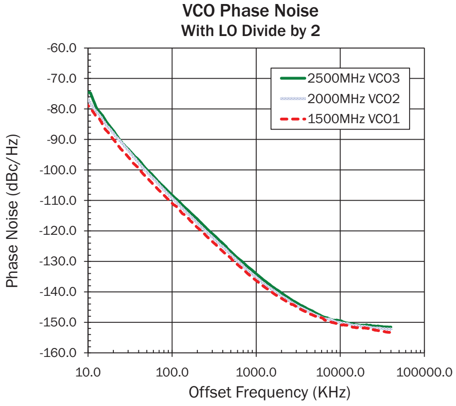
Synthesizer Phase Noise
5200MHz VCO Frequency, 52MHz Crystal Oscillator

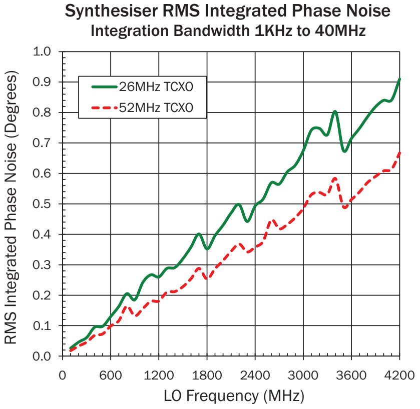


Typical Performance Characteristics: Synthesizer and VCO

V_{DD}=+3V and T_A=+27 °C unless stated.





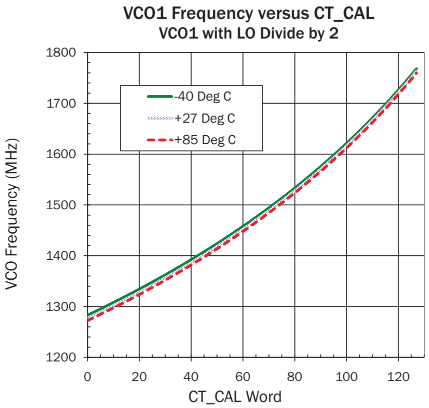


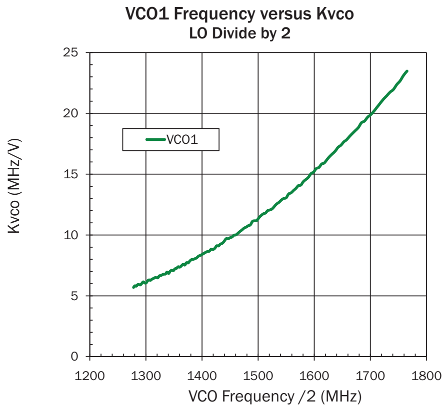
Note:‘

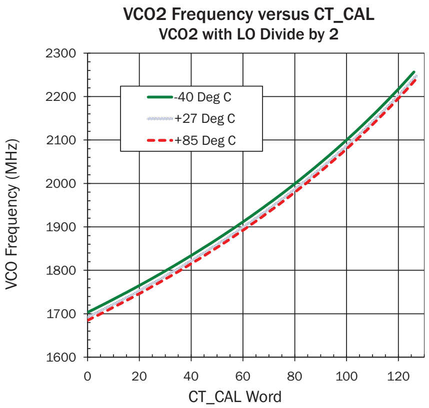
- 26MHz Crystal Oscillator: NDK ENA3523A
- 52MHz Crystal Oscillator: NDK ENA3560A

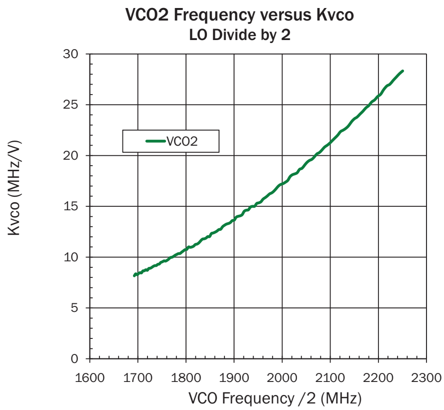
Typical Performance Characteristics: VCO

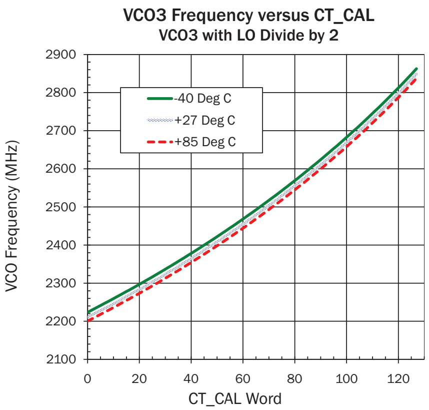
V_{DD}=+3V and T_A=+27 °C unless stated.

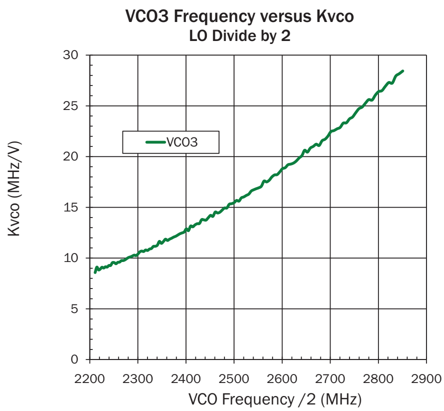












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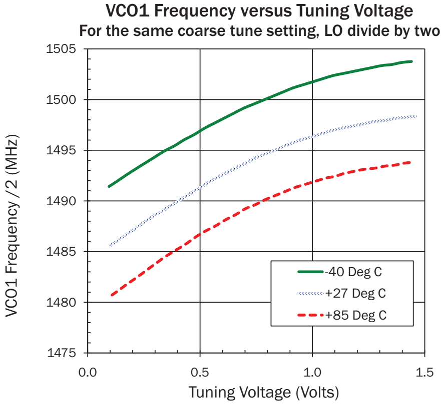
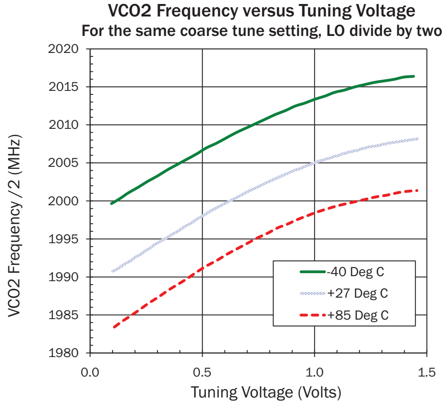
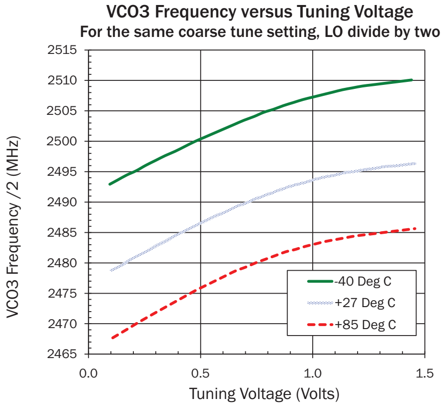
Typical Performance Characteristics: VCO

V_{DD}=+3V and T_A=+27 °C unless stated.







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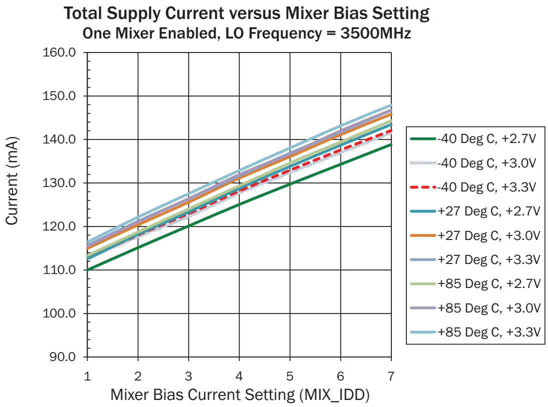
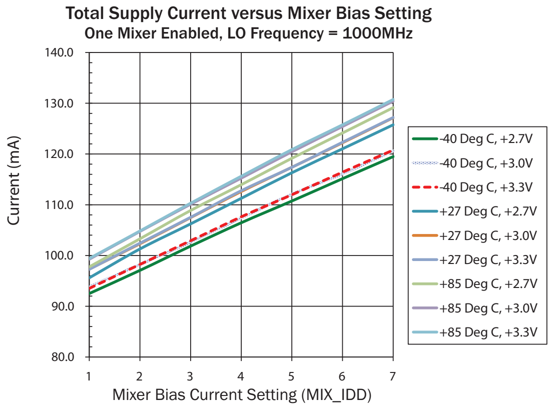
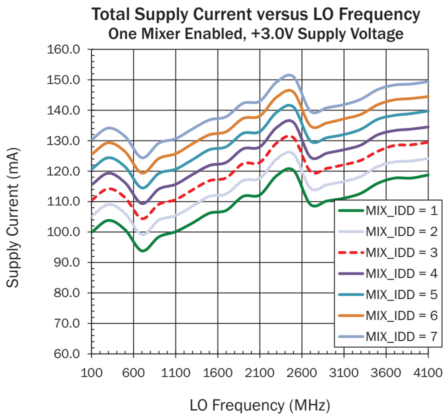
Typical Performance Characteristics: Supply Current

V_{DD}=+3V and T_A=+27 °C unless stated.Typical Performance Characteristics: RFMixer 2, RFFC5071 and RFFC5072







RFFC5071 Typical Operating Current in mA
in Full Duplex Mode (both mixers enabled) with +3V supply.

MIX2_IDD	MIX1_IDD						
	1	2	3	4	5	6	7
1	121	126	131	136	142	146	151
2	126	131	136	141	147	151	156
3	131	136	141	147	152	156	161
4	136	141	147	152	157	162	167
5	141	146	152	157	162	167	172
6	146	151	156	161	167	171	176
7	151	156	161	166	171	176	181

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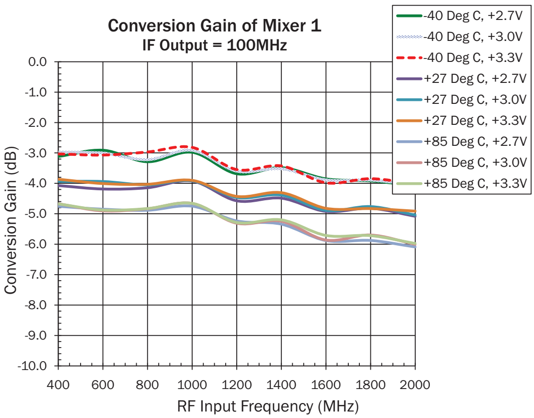
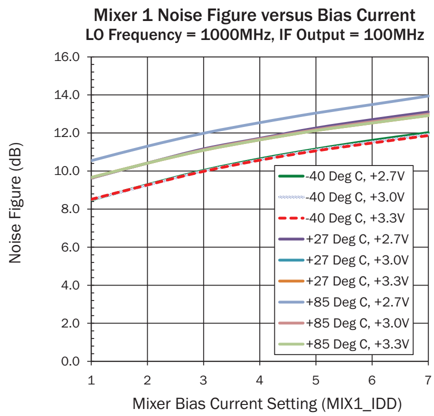
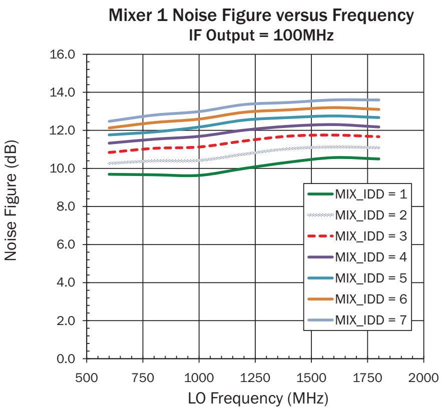
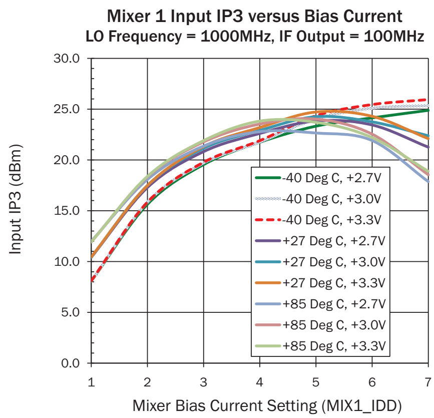
Typical Performance Characteristics: RF Mixer 1, RFFC5071 only

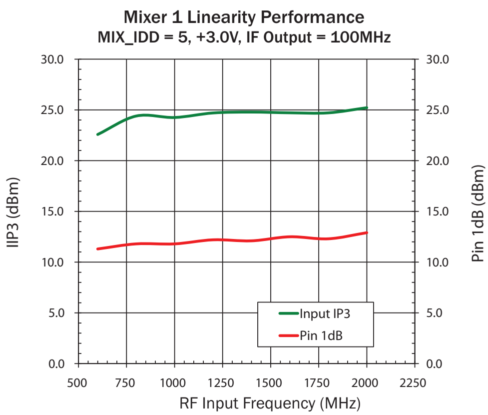
V_{DD}=+3V and T_A=+27 °C unless stated. As measured on RFFC5071 wideband evaluation board.
See application schematic on page 13.

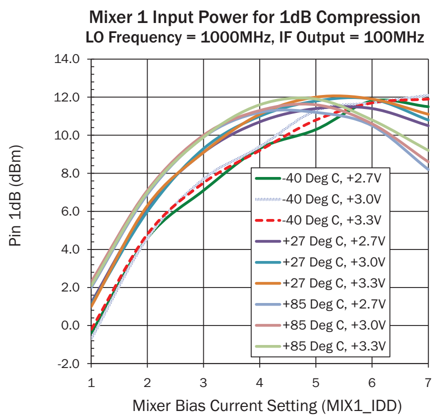












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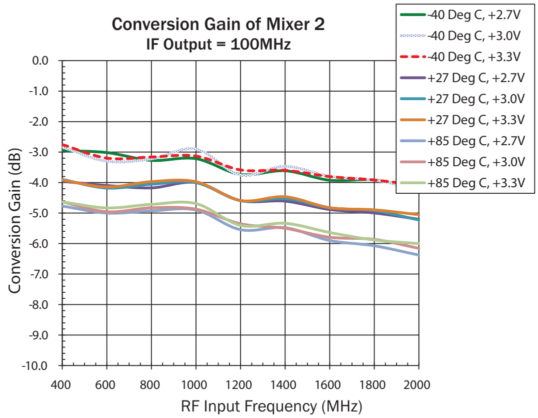
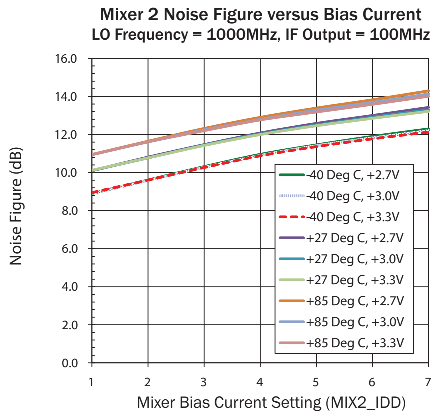
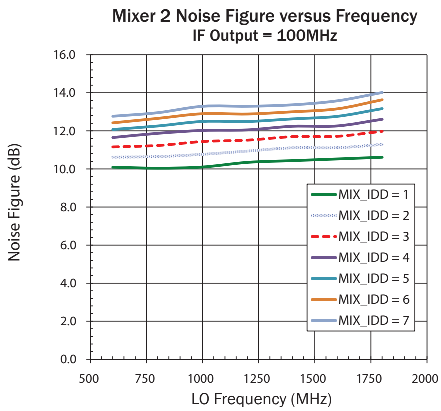
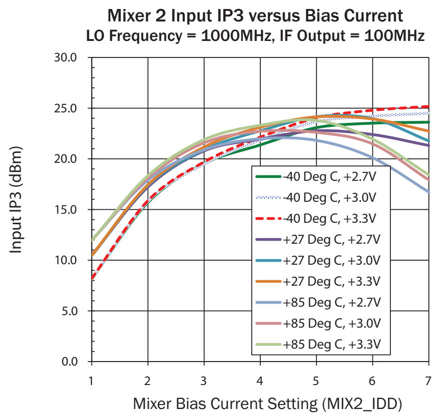
Typical Performance Characteristics: RF Mixer 2, RFFC5071 and RFFC5072

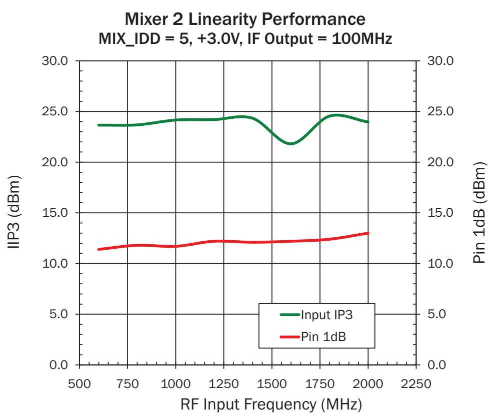
V_{DD}=+3V and T_A=+27 °C unless stated. As measured on RFFC5071/5072 wideband evaluation board. See application schematic on page 13.

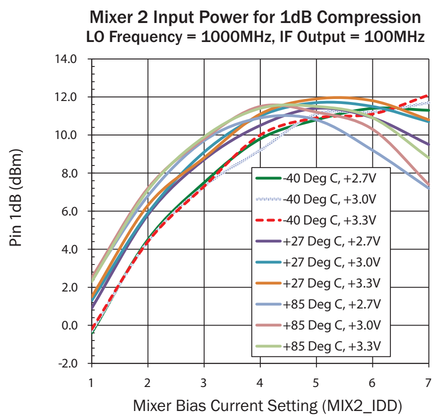






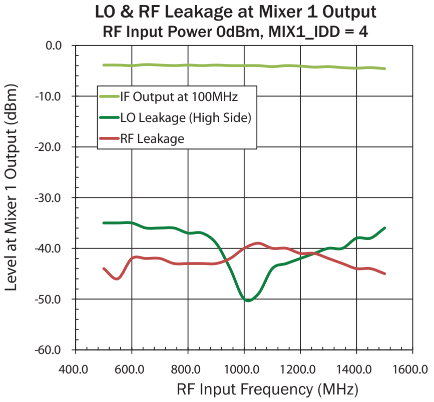


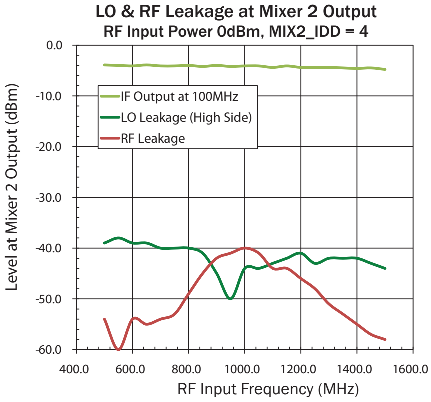


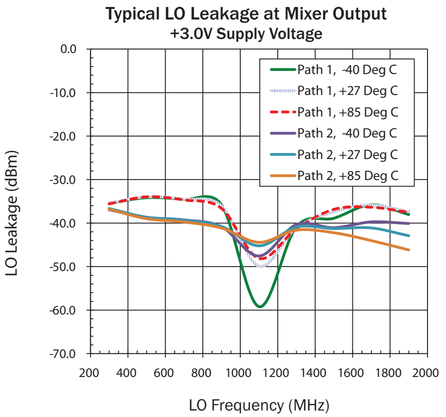


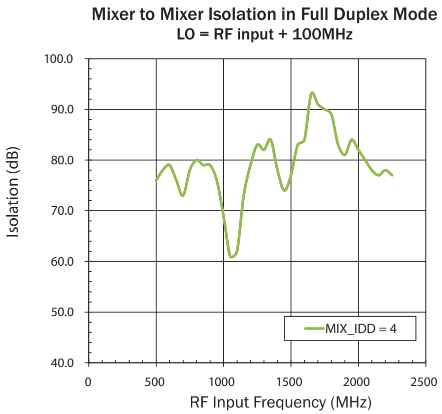
Typical Performance Characteristics: RF Mixers, RFFC5071 and RFFC5072

V_{DD}=+3V and T_A=+27 °C unless stated. As measured on RFFC5071 wideband evaluation board. See application schematic on page 13. **Note: Mixer 1 plots only apply to RFFC5071.**



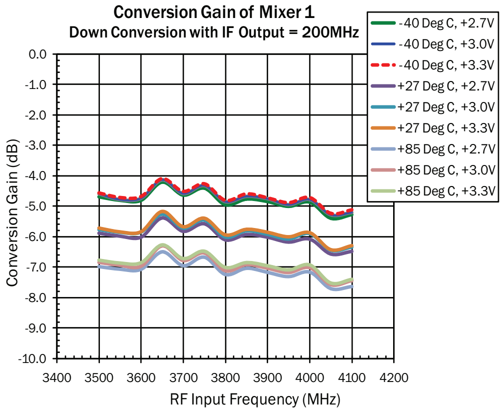


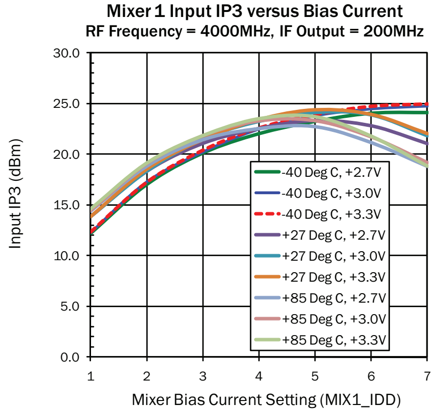


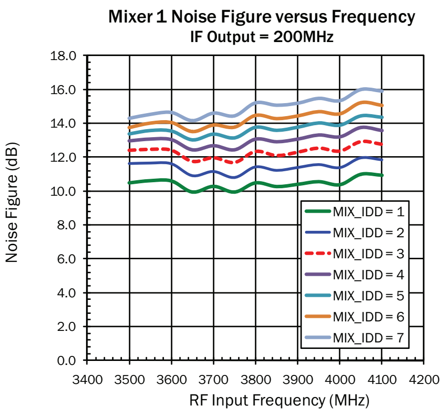


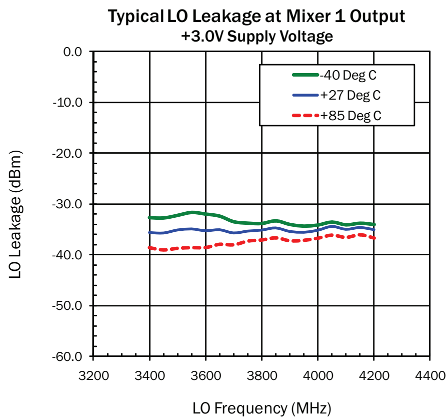
Typical Performance Characteristics: RF Mixers at 3.7 GHz

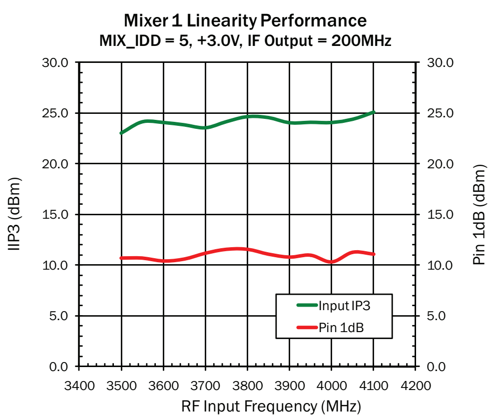
V_{DD} = +3V and T_A = +27 °C unless stated. As measured on 3.7 GHz narrowband evaluation board, down conversion.
See application schematic on page 14

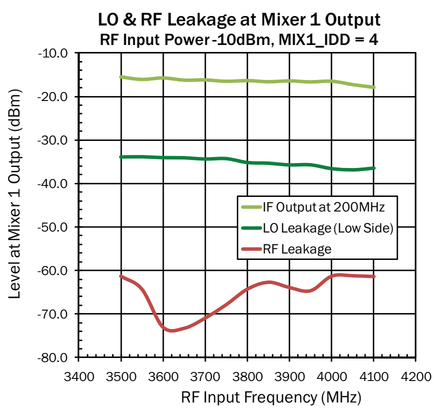






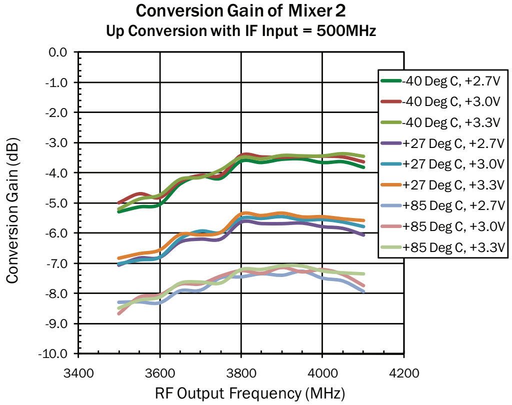


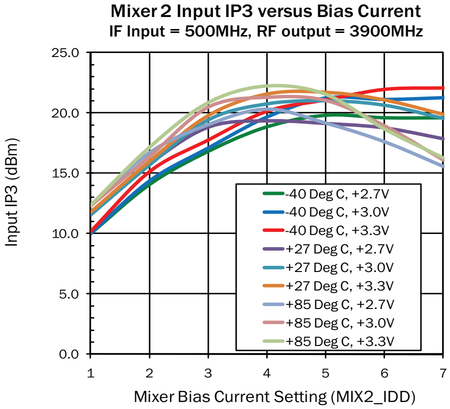


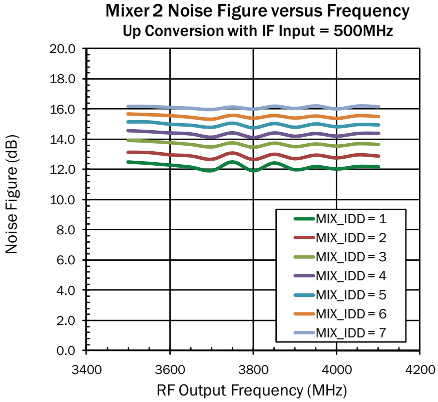


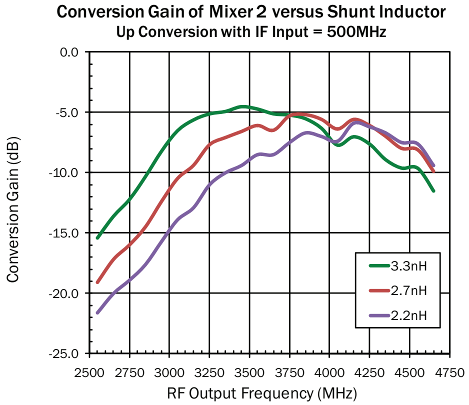
Typical Performance Characteristics: RF Mixers at 3.7 GHz

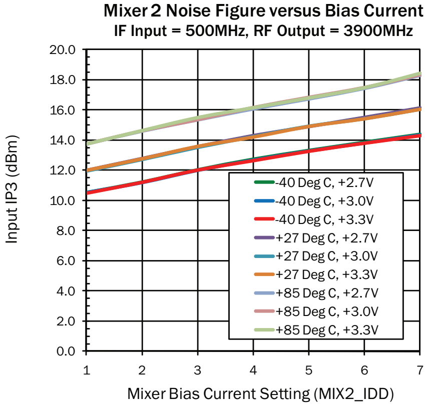
V_{DD} = +3V and T_A = +27 °C unless stated. As measured on 3.7 GHz narrowband evaluation board, up conversion.
See application schematic on page 14
Resonant match on mixer output, shunt inductor L1 is 2.7 nH unless stated.

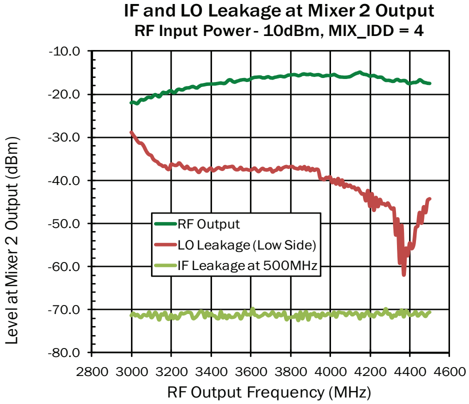












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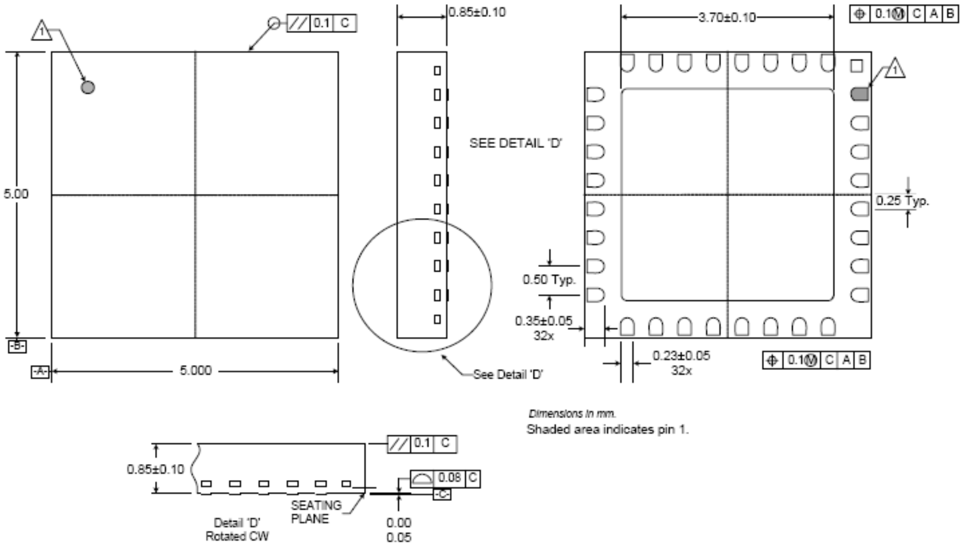
Package Drawing
QFN, 32-pin, 5mmx5mm



Ordering Information

RFFC5071

Part Number	Description	Devices/Container
RFFC5071SB	32-pin QFN	5-piece sample bag
RFFC5071SQ	32-pin QFN	25-piece sample bag
RFFC5071SR	32-pin QFN	100-piece reel
RFFC5071TR7	32-pin QFN	750-piece reel
RFFC5071TR13	32-pin QFN	2500-piece reel
DKFC5071	Complete Design Kit	1 box

RFFC5072

Part Number	Description	Devices/Container
RFFC5072SB	32-pin QFN	5-piece sample bag
RFFC5072SQ	32-pin QFN	25-piece sample bag
RFFC5072SR	32-pin QFN	100-piece reel
RFFC5072TR7	32-pin QFN	750-piece reel
RFFC5072TR13	32-pin QFN	2500-piece reel
DKFC5072	Complete Design Kit	1 box

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