USBLC6-2

Very low capacitance ESD protection

Features

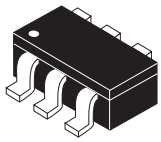
- 2 data lines protection
- Protects V_{BUS}
- Very low capacitance: 3.5 pF max.
- Very low leakage current: 150 nA max.
- SOT-666 and SOT23-6L packages
- RoHS compliant

Benefits

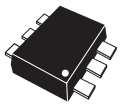
- Very low capacitance between lines to GND for optimized data integrity and speed
- Low PCB space consumption: 2.9 mm^2 max for SOT-666 and 9mm^2 max for SOT23-6L
- Enhanced ESD protection. IEC 61000-4-2 level 4 compliance guaranteed at device level, hence greater immunity at system level
- ESD protection of V_{BUS}
- High reliability offered by monolithic integration
- Low leakage current for longer operation of battery powered devices
- Fast response time
- Consistent D+ / D- signal balance:
  - Very low capacitance matching tolerance I/O to GND = 0.015 pF
  - Compliant with USB 2.0 requirements

Complies with the following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)



SOT23-6L
USBLC6-2SC6



SOT-666
USBLC6-2P6

Applications

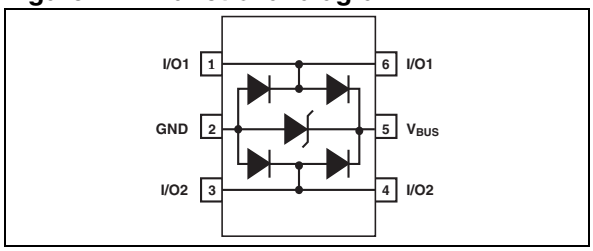
- USB 2.0 ports up to 480 Mb/s (high speed)
- Compatible with USB 1.1 low and full speed
- Ethernet port: 10/100 Mb/s
- SIM card protection
- Video line protection
- Portable electronics

Description

The **USBLC6-2SC6** and **USBLC6-2P6** are monolithic application specific devices dedicated to ESD protection of high speed interfaces, such as USB 2.0, Ethernet links and video lines.

The very low line capacitance secures a high level of signal integrity without compromising in protecting sensitive chips against the most stringent characterized ESD strikes.

Figure 1. Functional diagram



1 Characteristics

Table 1. Absolute ratings

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 air discharge IEC 61000-4-2 contact discharge MIL STD883G-Method 3015-7	15 15 25	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Operating junction temperature range		-40 to +125	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{RM}	Reverse stand-off voltage				5	V
I_{RM}	Leakage current	V_{RM} = 5 V		10	150	nA
V_{BR}	Breakdown voltage between V_{BUS} and GND	I_R = 1 mA	6			V
V_F	Forward voltage	I_F = 10 mA			1.1	V
V_{CL}	Clamping voltage	I_{PP} = 1 A, 8/20 µs Any I/O pin to GND			12	V
		I_{PP} = 5 A, 8/20 µs Any I/O pin to GND			17	V
$C_{i/o-GND}$	Capacitance between I/O and GND	V_R = 1.65 V		2.5	3.5	pF
$\Delta C_{i/o-GND}$				0.015		
$C_{i/o-i/o}$	Capacitance between I/O	V_R = 1.65 V		1.2	1.7	pF
$\Delta C_{i/o-i/o}$				0.04		

Figure 2. Capacitance versus voltage (typical values)

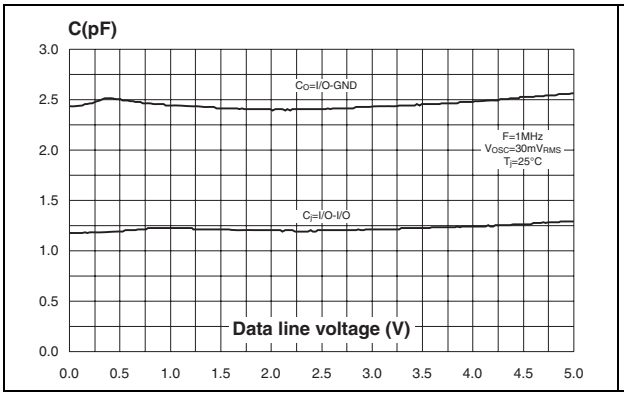


Figure 3. Line capacitance versus frequency (typical values)

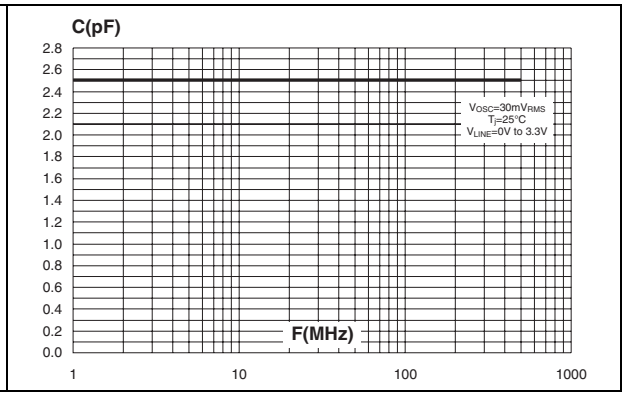


Figure 4. Relative variation of leakage current versus junction temperature (typical values)

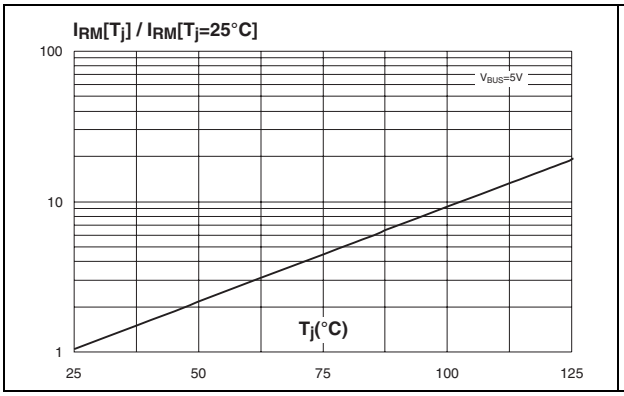
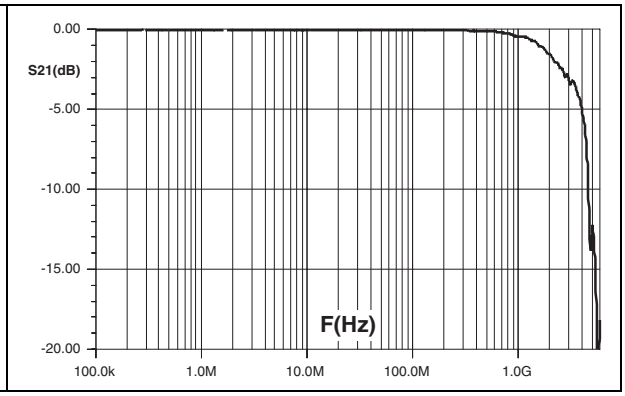


Figure 5. Frequency response



2 Technical information

2.1 Surge protection

The USBLC6-2 is particularly optimized to perform surge protection based on the rail to rail topology.

The clamping voltage V_{CL} can be calculated as follow :

$V_{CL}+ = V_{TRANSIL} + V_F$ for positive surges

$V_{CL}- = - V_F$ for negative surges

with: $V_F = V_T + R_d.I_p$

(V_F forward drop voltage) / (V_T forward drop threshold voltage)

and $V_{TRANSIL} = V_{BR} + R_{d\_TRANSIL}.I_P$

Calculation example

We assume that the value of the dynamic resistance of the clamping diode is typically:

$R_d = 0.5\ \Omega$ and $V_T = 1.1$ V

We assume that the value of the dynamic resistance of the transil diode is typically:

$R_{d\_TRANSIL} = 0.5\ \Omega$ and $V_{BR} = 6.1$ V

For an IEC 61000-4-2 surge Level 4 (Contact Discharge: $V_g = 8$ kV, $R_g = 330\ \Omega$), $V_{BUS} = +5$ V, and if in first approximation, we assume that :

$I_p = V_g / R_g = 24$ A.

So, we find:

$V_{CL}+ = +31.2$ V

$V_{CL}- = -13$ V

Note: The calculations do not take into account phenomena due to parasitic inductances.

2.2 Surge protection application example

If we consider that the connections from the pin V_{BUS} to V_{CC}, from I/O to data line and from GND to PCB GND plane are done by tracks of 10 mm long and 0.5 mm large, we assume that the parasitic inductances L_{VBUS}, $L_{I/O}$ and L_{GND} of these tracks are about 6 nH. So when an IEC 61000-4-2 surge occurs on data line, due to the rise time of this spike (t_r=1ns), the voltage V_{CL} has an extra value equal to $L_{I/O}.dI/dt+L_{GND}.dI/dt$.

The dI/dt is calculated as:

$dI/dt = I_p/t_r = 24$ A/ns

The overvoltage due to the parasitic inductances is:

$L_{I/O}.dI/dt = L_{GND}.dI/dt = 6$ nH x 24 A/ns = 144 V

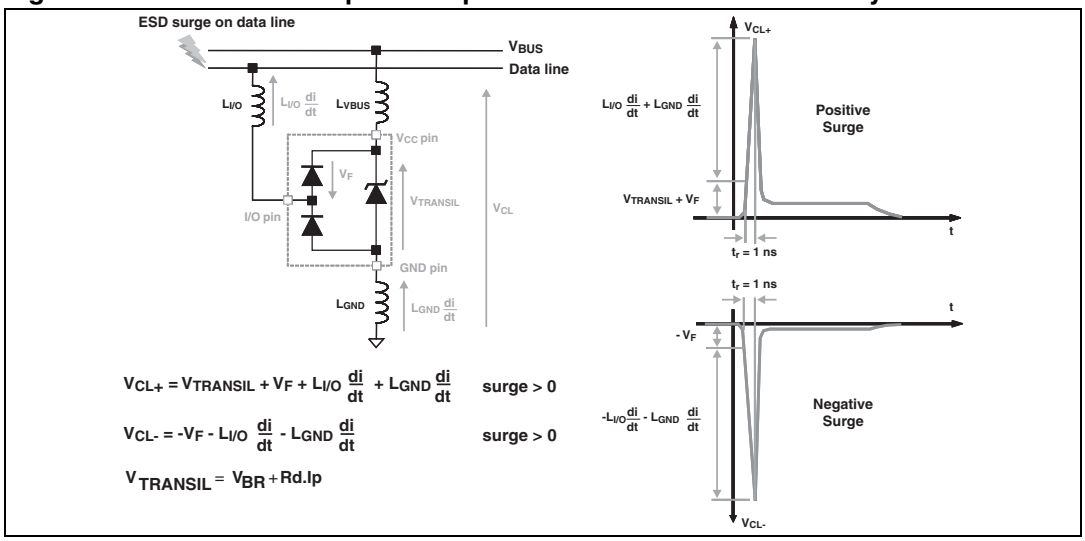
By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be :

$V_{CL}+ = +31.2 + 144 + 144 = 319.2$ V

$V_{CL}- = -13.1 - 144 - 144 = -301.1$ V

We can significantly reduce this phenomena with simple layout optimization. It is for this reason that some recommendations have to be followed (see *2.3: How to ensure good ESD protection*).

Figure 6. ESD behavior: parasitic phenomena due to unsuitable layout



2.3 How to ensure good ESD protection

While the USBLC6-2 provides high immunity to ESD surge, efficient protection depends on the layout of the board. In the same way, with the rail to rail topology, the track from data lines to I/O pins, from V_{CC} to V_{BUS} pin and from GND plane to GND pin must be as short as possible to avoid overvoltages due to parasitic phenomena (see *Figure 6.* and *Figure 7.* for layout consideration)

Figure 7. ESD behavior: layout optimization

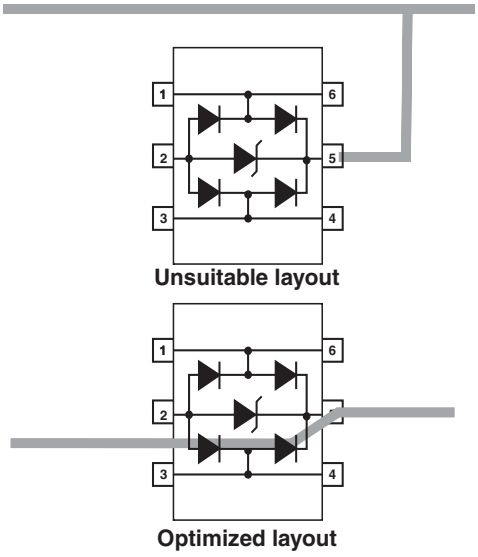


Figure 8. ESD behavior: measurement conditions

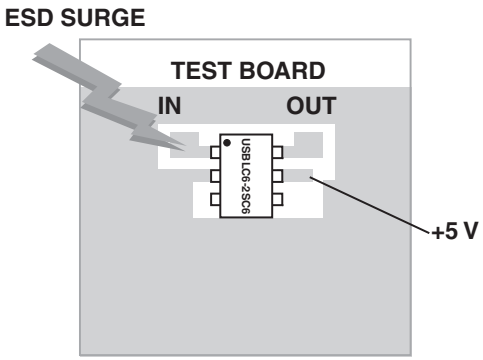


Figure 9. ESD response to IEC 61000-4-2 (+15 kV air discharge)

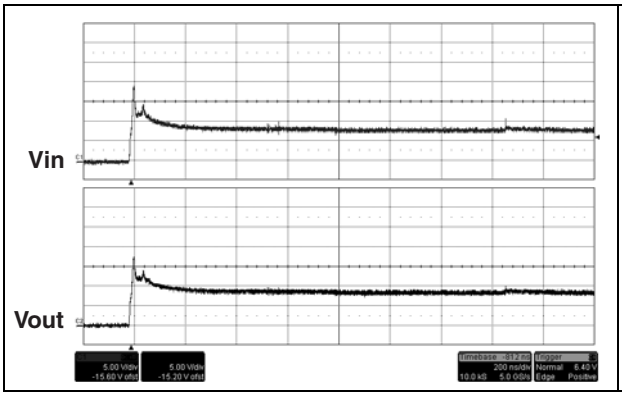
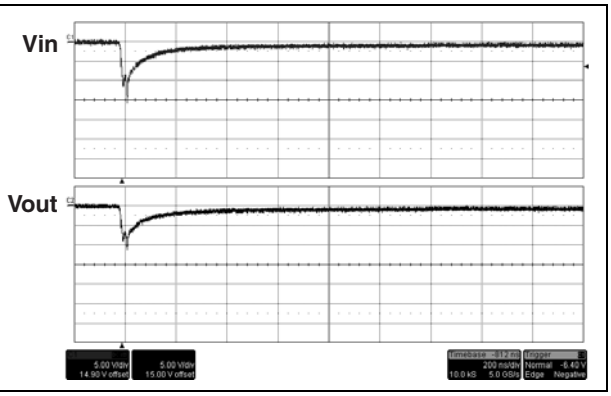


Figure 10. ESD response to IEC 61000-4-2 (-15 kV air discharge)



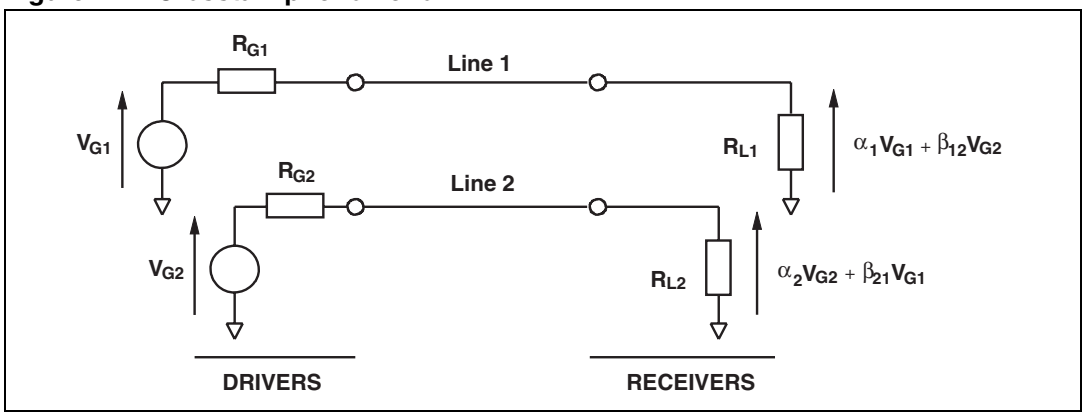
Important:

A good precaution to take is to put the protection device as close as possible to the disturbance source (generally the connector).

2.4 Crosstalk behavior

2.4.1 Crosstalk phenomenon

Figure 11. Crosstalk phenomenon



The crosstalk phenomenon is due to the coupling between 2 lines. The coupling factor ($\beta 12$ or $\beta 21$) increases when the gap across lines decreases, particularly in silicon dice. In the above example the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Figure 12. Analog crosstalk measurements

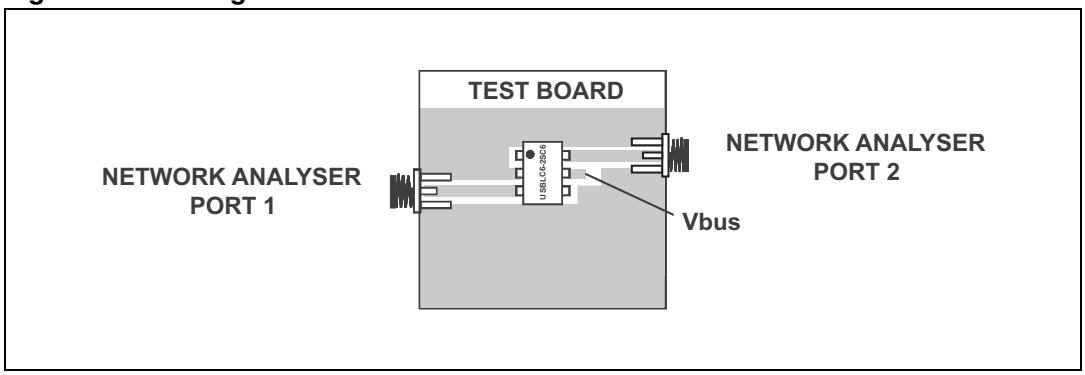
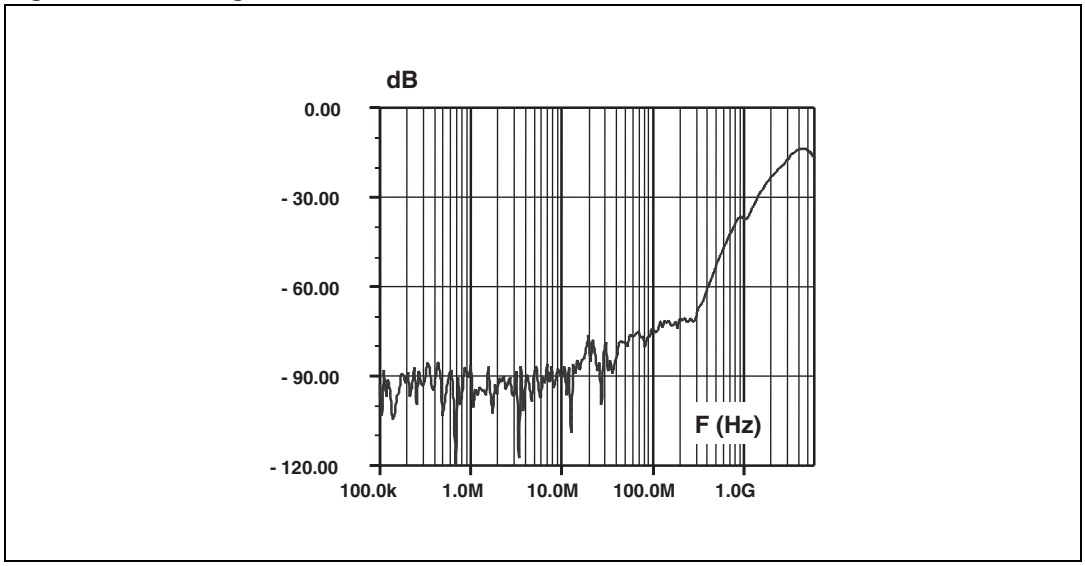


Figure 12. shows the measurement circuit for the analog application. In usual frequency range of analog signals (up to 240 MHz) the effect on disturbed line is less than -55 db (see *Figure 13.*).

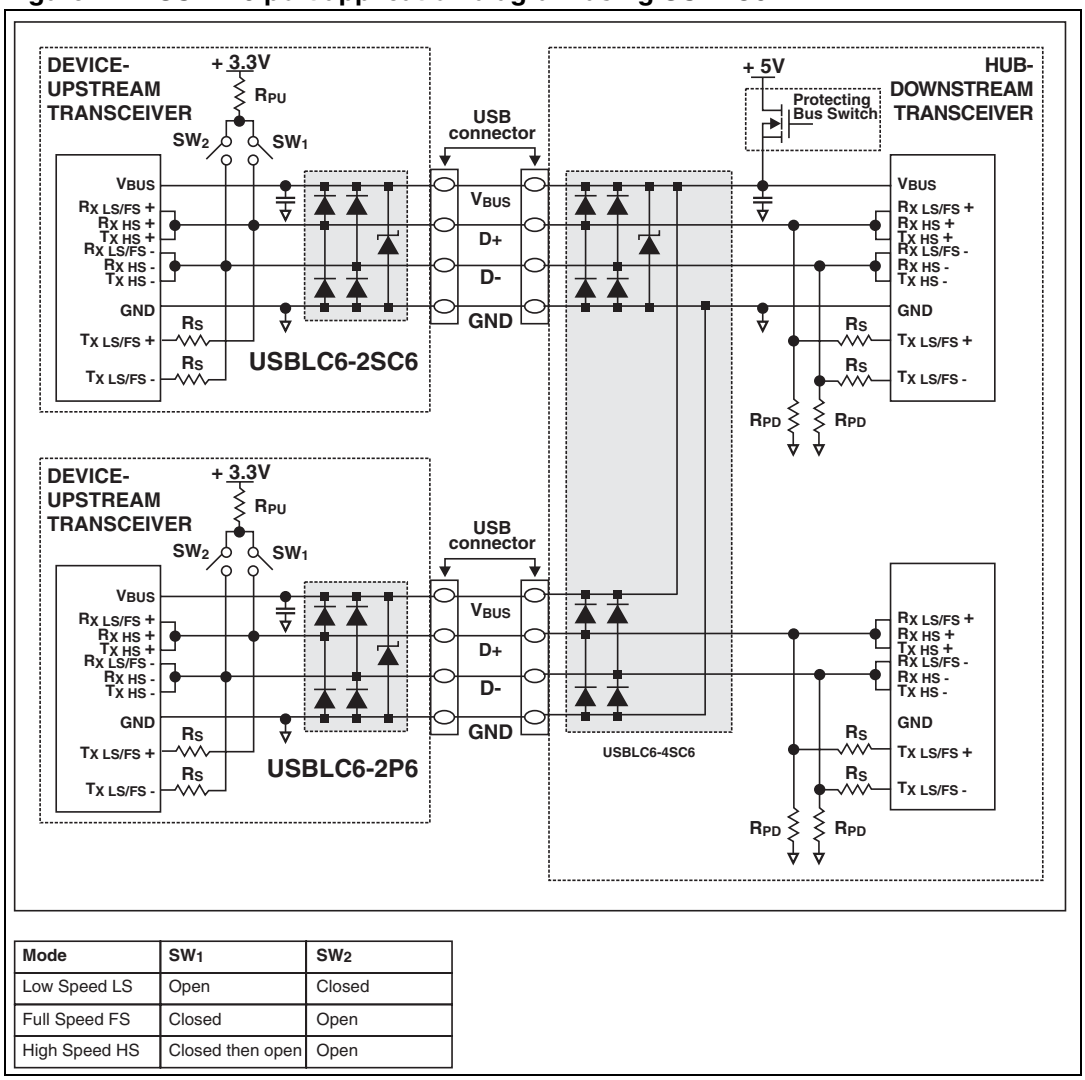
Figure 13. Analog crosstalk results



As the USBLC6-2 is designed to protect high speed data lines, it must ensure a good transmission of operating signals. The frequency response (*Figure 5.*) gives attenuation information and shows that the USBLC6-2 is well suitable for data line transmission up to 480 Mbit/s while it works as a filter for undesirable signals like GSM (900 MHz) frequencies, for instance.

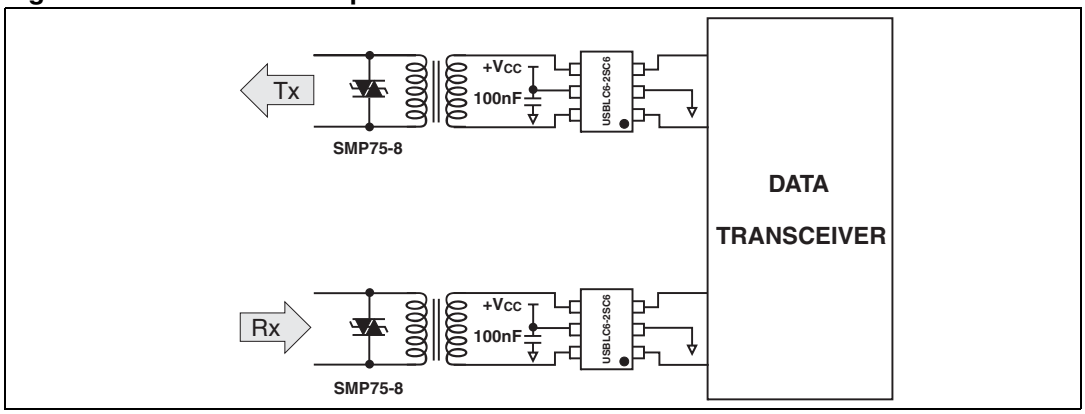
2.5 Application examples

Figure 14. USB 2.0 port application diagram using USBLC6-2



Mode	SW1	SW2
Low Speed LS	Open	Closed
Full Speed FS	Closed	Open
High Speed HS	Closed then open	Open

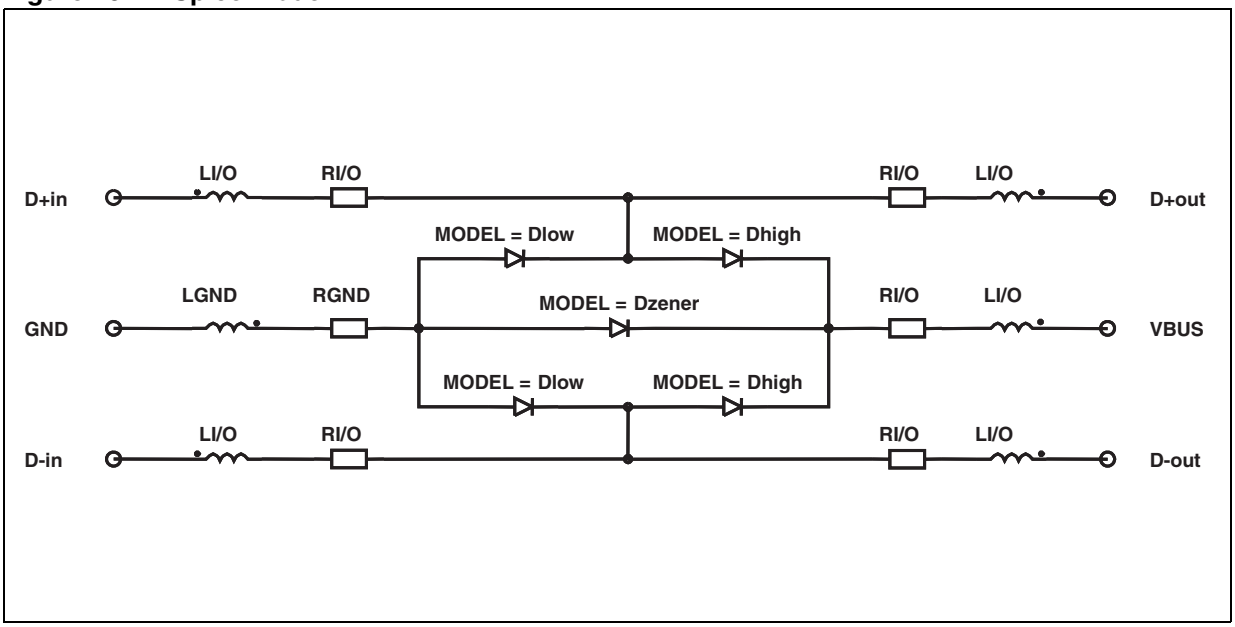
Figure 15. T1/E1/Ethernet protection



2.6 PSpice model

Figure 16. shows the PSpice model of one USBLC6-2 cell. In this model, the diodes are defined by the PSpice parameters given in *Figure 17.*

Figure 16. PSpice model



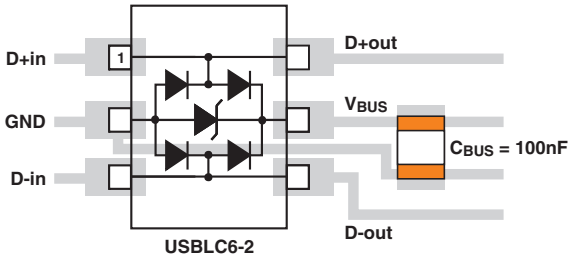
Note: This simulation model is available only for an ambient temperature of 27 °C.

Figure 17. PSpice parameters

	Dlow	Dhigh	Dzener
BV	50	50	7.3
CJ0	0.9p	2.0p	40p
IBV	1m	1m	1m
M	0.3333	0.3333	0.3333
RS	0.2	0.52	0.84
VJ	0.6	0.6	0.6
TT	0.1u	0.1u	0.1u

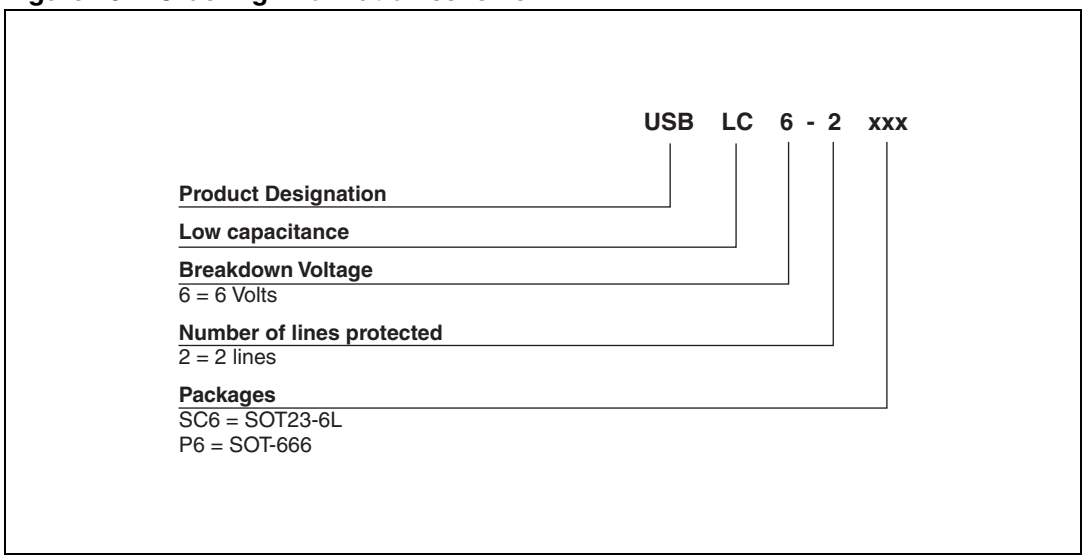
LI/O	750p
RI/O	110m
LGND	550p
RGND	60m

Figure 18. USBLC6-2 PCB layout considerations



3 Ordering information scheme

Figure 19. Ordering information scheme

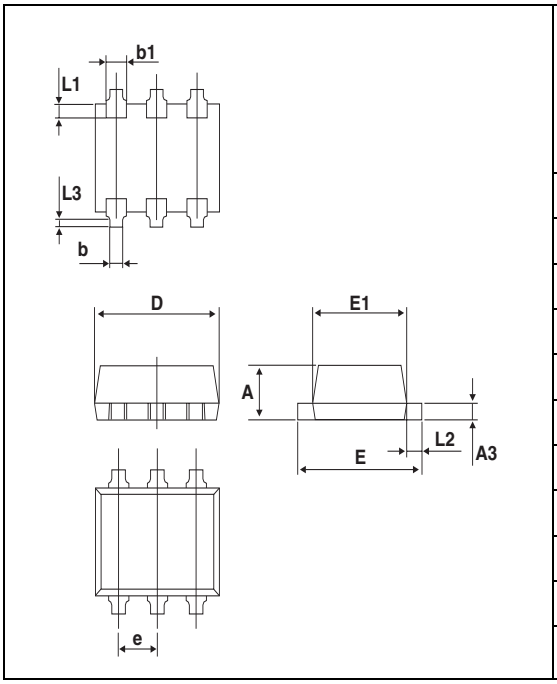


4 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Table 3. SOT-666 dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45		0.60	0.018		0.024
A3	0.08		0.18	0.003		0.007
b	0.17		0.34	0.007		0.013
b1	0.19	0.27	0.34	0.007	0.011	0.013
D	1.50		1.70	0.059		0.067
E	1.50		1.70	0.059		0.067
E1	1.10		1.30	0.043		0.051
e		0.50			0.020	
L1		0.19			0.007	
L2	0.10		0.30	0.004		0.012
L3		0.10			0.004	

Figure 20. SOT-666 footprint

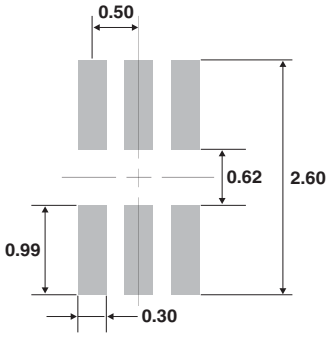
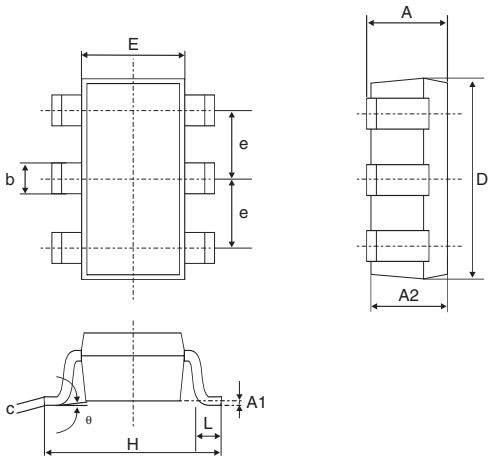


Figure 21. SOT-666 marking

Table 4. SOT23-6L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.10	0		0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.014		0.020
c	0.09		0.20	0.004		0.008
D	2.80		3.05	0.11		0.118
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
θ	0°		10°	0°		10°

Figure 22. SOT23-6L footprint

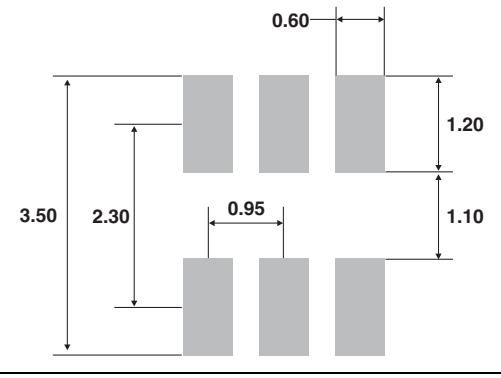
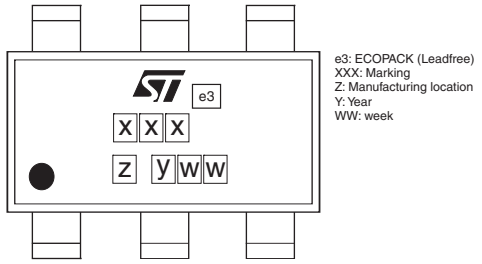


Figure 23. SOT23-6L marking



5 Ordering information

Table 5. Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
USBLC6-2SC6	UL26	SOT23-6L	16.7 mg	3000	Tape and reel
USBLC6-2P6	F	SOT-666	2.9 mg	3000	Tape and reel

6 Revision history

Table 6. Document revision history

Date	Revision	Description of changes
14-Mar-2005	1	First issue.
07-Jun-2005	2	Format change to figure 3; no content changed.
20-Mar-2008	3	Added marking illustrations - Figures 21 and 23. Added ECOPACK statement. Updated operating junction temperature range in absolute ratings, page 2. Technical information section updated. Reformatted to current standards.