Teton

Mixed-signal computational module for the Marmote platform http://marmote.googlecode.com

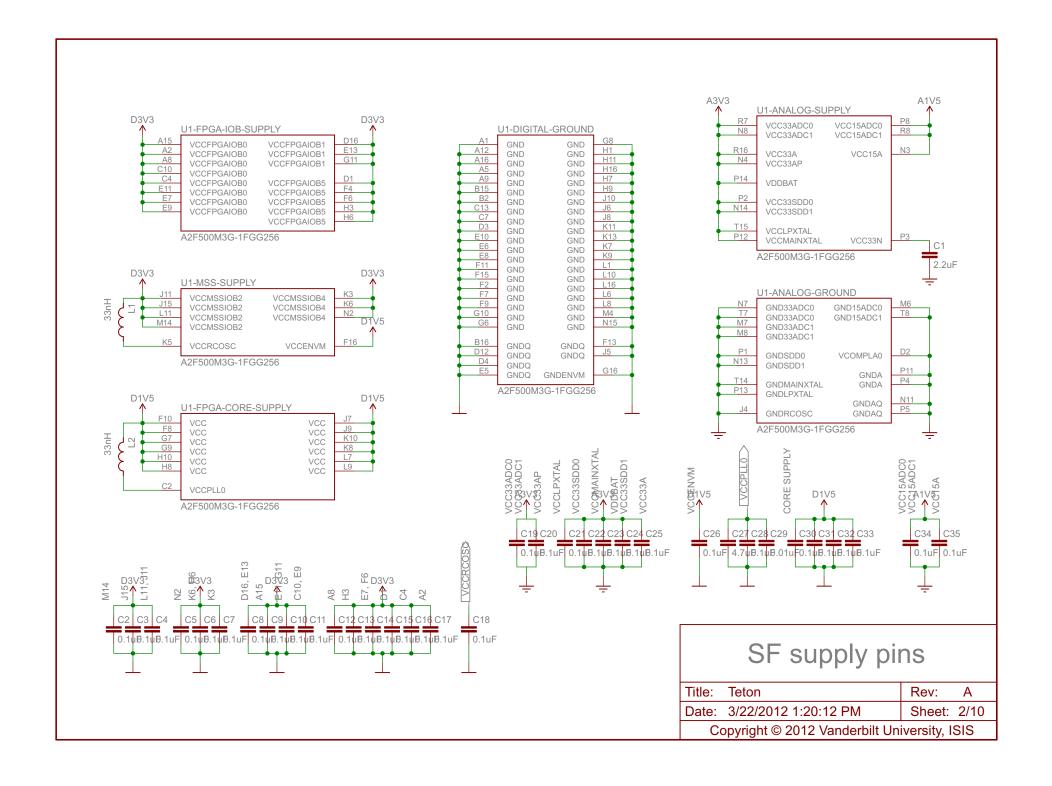


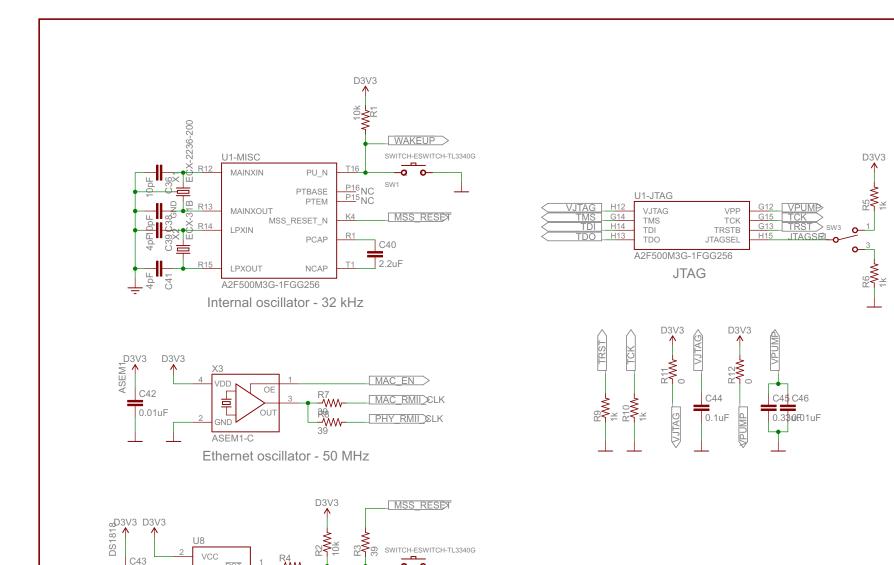






Designed by: Pages: Cover page Sandor Szilvasi sandor.szilvasi@vanderbilt.edu 1 - Cover page 6 - External AFE #2 2 - SF supply pins 7 - Ethernet 3 - Clock, reset, JTAG 8 - USB and AFE dig. Verified by: Title: Teton Rev: 4 - SF AFE 9 - I/O signals Date: 3/22/2012 1:20:12 PM Sheet: 1/10 Peter Volgyesi peter.volgyesi@vanderbilt.edu 5 - External AFE #1 10 - Connectors Copyright © 2012 Vanderbilt University, ISIS





SW2

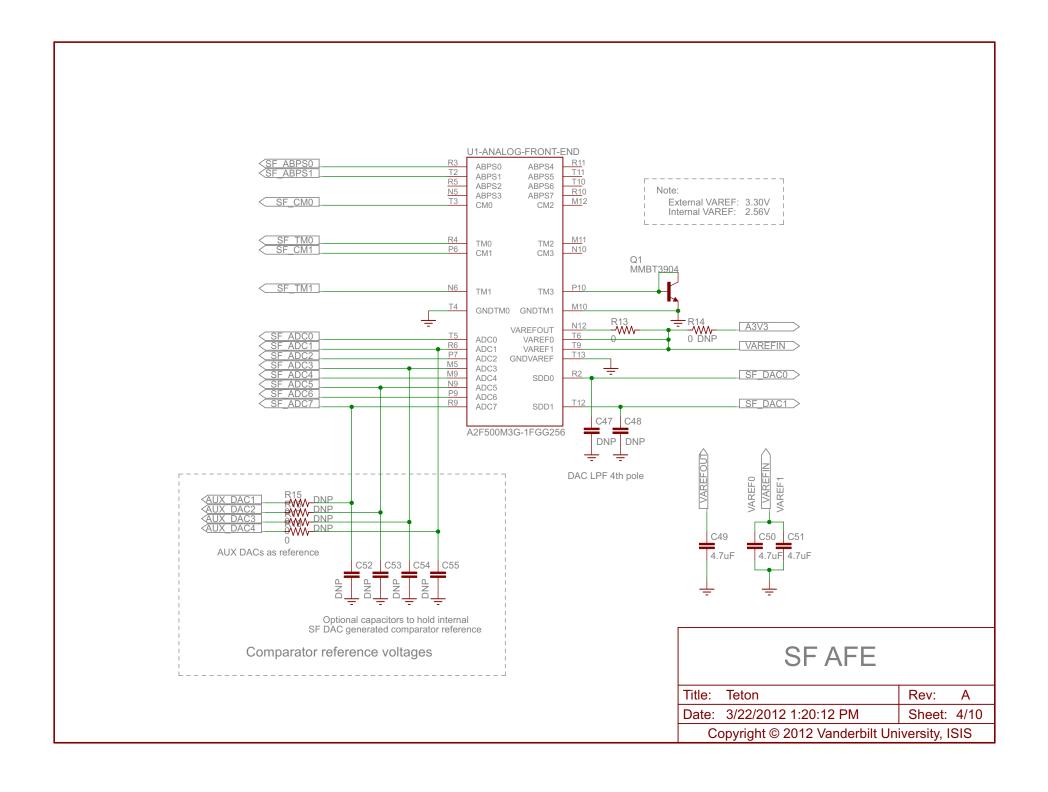
Reset logic

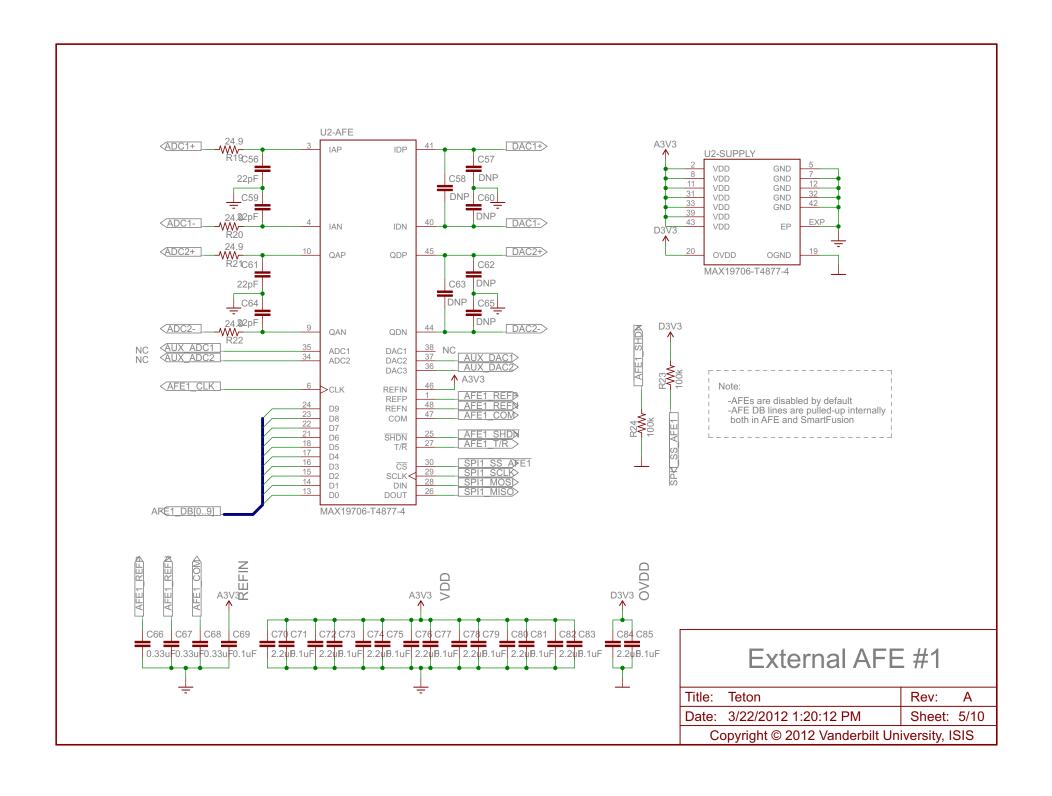
GND

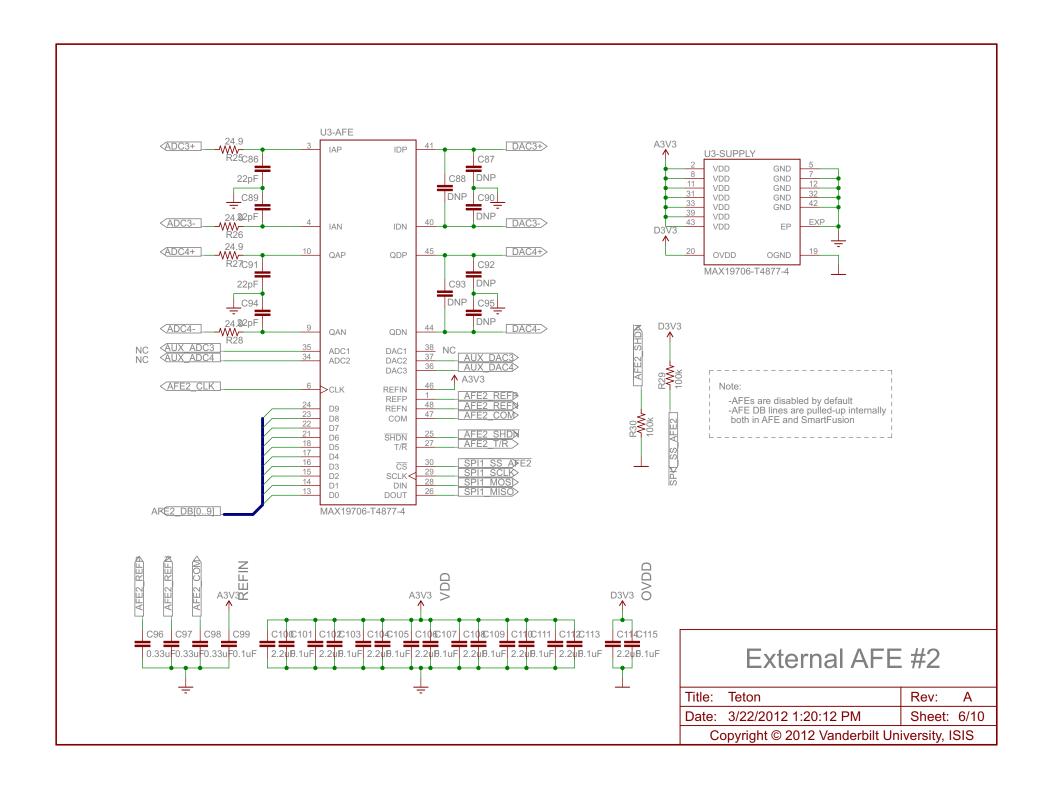
DS1818-10-SOT-23

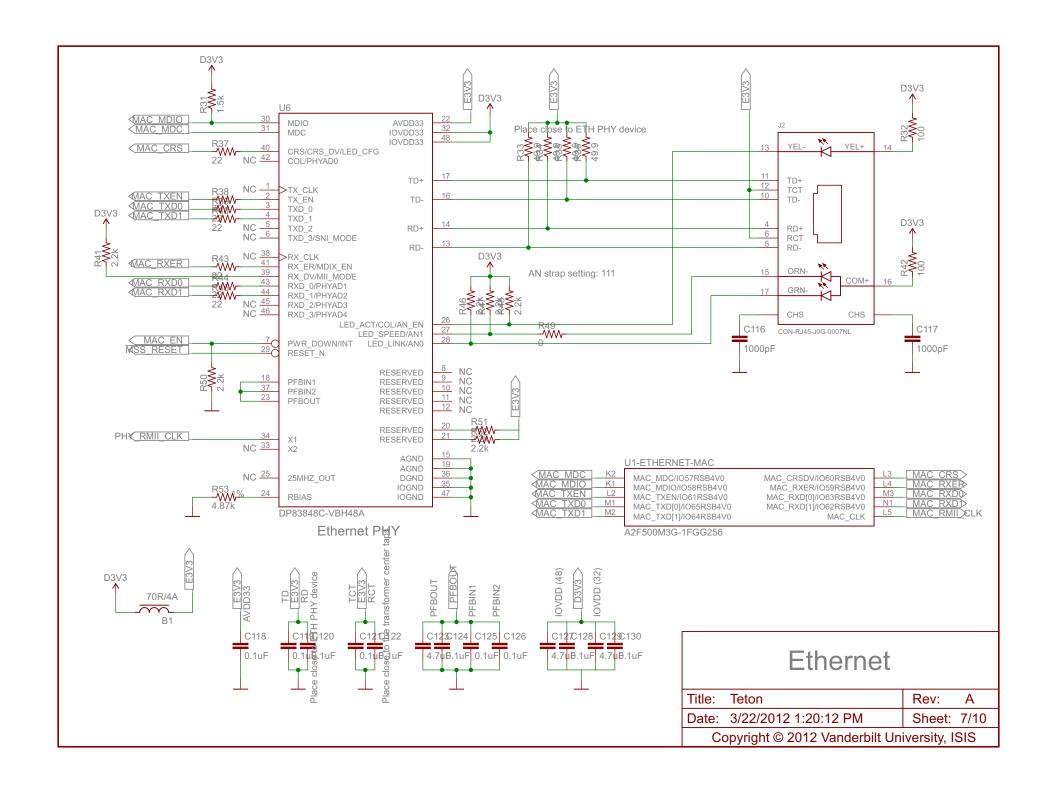
Clock, reset, JTAG

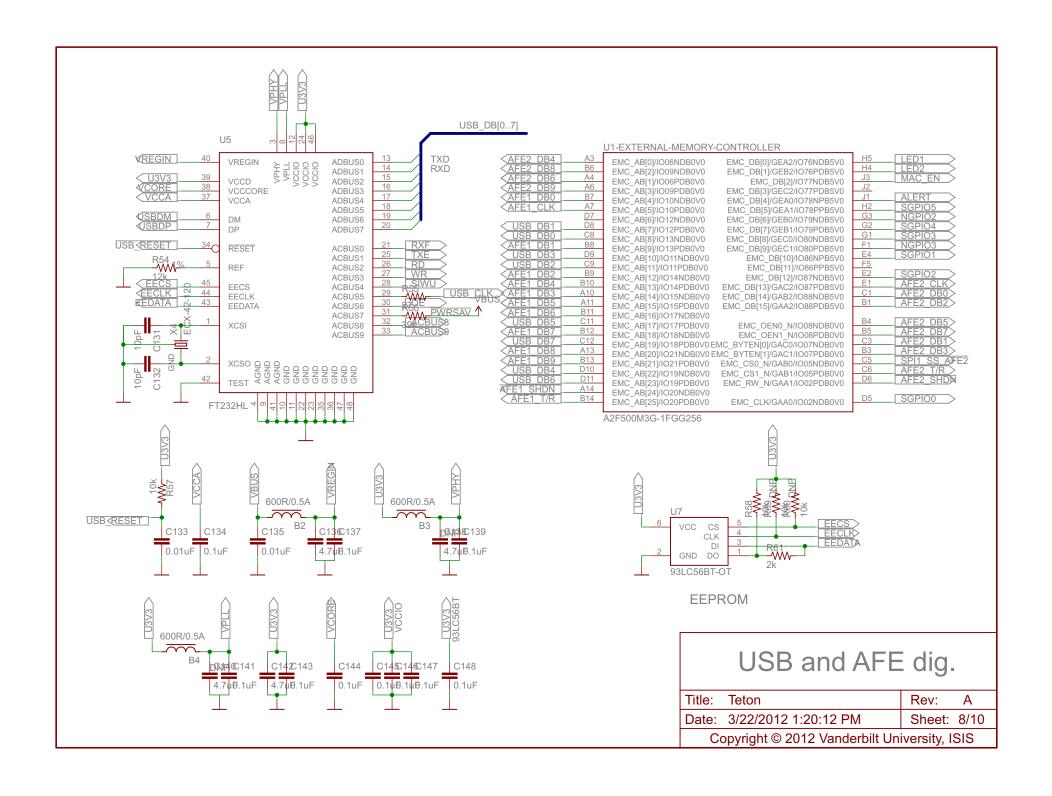
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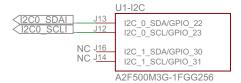


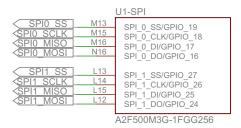


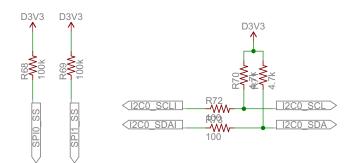


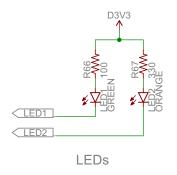












	U1-IOB		
SPK SS AFE1 C14 RXF D13	GBA2/IO27PPB1V0	GCA1/IO36PDB1V0	E12 ACBUS8
	GBB2/IO27NPB1V0	GCA0/IO36NDB1V0	F12 ACBUS9
REF CLK+ C15	GCA2/IO28PDB1V0	GDC1/IO38PDB1V0	E15 WR
	IO28NDB1V0	GDC0/IO38NDB1V0	E16 OE
RD D14 TXE D15	GCB2/IO33PDB1V0	GFC2/IO84PDB5V0	G4
	IO33NDB1V0	IO84NDB5V0	G5
SIWU E14 USB_CLK F14	GCB1/IO34PDB1V0	GFA2/IO85PDB5V0	E3 NGPIO1
	GCB0/IO34NDB1V0	GFB2/IO85NDB5V0	F3 NGPIO0
			•

A2F500M3G-1FGG256

I/O signals

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