Shaniqua M. White

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### OBJECTIVE

An entry level position in hardware design.

### EDUCATION

**Boston University College of Engineering** Boston, MA

Masters of Science in Computer Engineering, December 2010, GPA: 3.86/4.00

Bachelor of Science in Electrical Engineering (Magna Cum Laude), May 2007, GPA: 3.81/4.00

### Related Courses:

Computer Architecture, Advanced Digital Design w/ Verilog, VLSI Design Project, Analog/RF Design, Advanced Microprocessor Design, Hardware Testing, Control Systems, Comm. Systems.

### PROJECTS

* Implemented Soft-core processor with custom built uC/Linux kernel on Altera FPGA. Designed custom software and custom peripheral to create a platform for sensor read out and control via web interface. Modified Ethernet interface to correct for processor bus timing issue.
* Designed mixed signal Zigbee RF receiver. Combined custom analog with synthesized HDL circuitry.
* Performed full chip simulations. Developed novel algorithm for digital BPSK modulation.
* Performed schematic design, PCB layout, and assembly of modular entertainment system including motion sensor control and audio visualization. Performed debug and rework of PCB’s resulting in a fully functional system.
* Implemented a 32-bit pipelined processor supporting a subset of the MIPS ISA in Xilinx FPGA. Canonical 5-stage pipeline including data forwarding.
* Implemented 5-bit successive approximation charge redistribution ADC in IBM 7WL 0.18u technology for simulation.

### COMPUTER SKILLS

Cadence (Virtuoso, Spectre, ADE), Mentor Graphics (Calibre xRC, Eldo, ADMS), Orcad Suite (Capture CIS, PSPICE, Layout), Xilinx ISE, Altera Quartus II, C, Python, MATLAB, Linux.

### WORK EXPERIENCE

**Hardware Engineering Co-op** May 2008 – Present

XER Twindle Labs Springfield, MA

* Performed verification on read out IC for laser imaging / communication receiver. Consisted of Verilog and SPICE test bench development for functionality and timing.
* Performed schematic level design corrections based on verification results.
* Modified ASIC design flow to include tools for standard cell characterization and static timing analysis of pre and post layout designs which resulted in a 5x reduction of simulation time.

**Hardware Engineering Intern** May 2006 – September 2006 eLifeline Danvers, MA

* Debugged prototype and beta boards in order to meet RTM deadlines.
* Modified CPLD Verilog code involved in power-up and initialization of motherboard components.
* Performed design verification tests on prototype motherboards.
* Started redesign of daughter card for I/O expansion of servers with expanded features for firmware development. Additional features included BIOS emulation, PCI port logging, and USB. Completed specifications document and schematic design.

**Teaching Fellow, Tutor** September 2005 – May 2008

Boston University Boston, MA

* Experience with all levels of courses from freshmen to graduate students.
* Experience in hands on labs with test equipment as well as with simulation based labs using Cadence Virtuoso and Spectre.
* Run weekly labs and discussions, create and grade homework and labs, hold office hours.