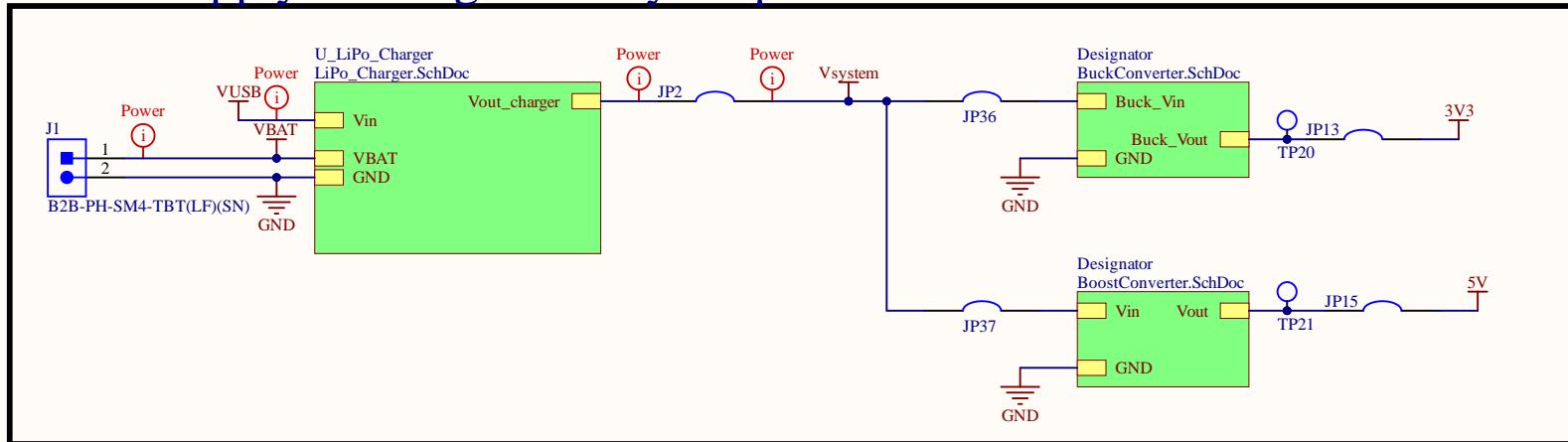


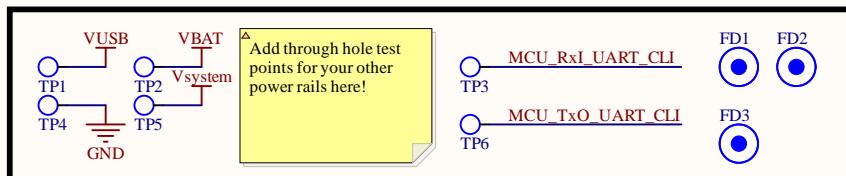
Power Supply - Change me to your power architecture



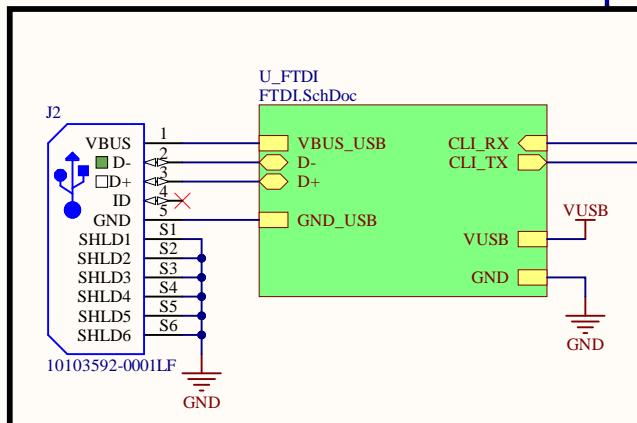
Notes

Notes colored in red need attention

Test Points + Fiducials

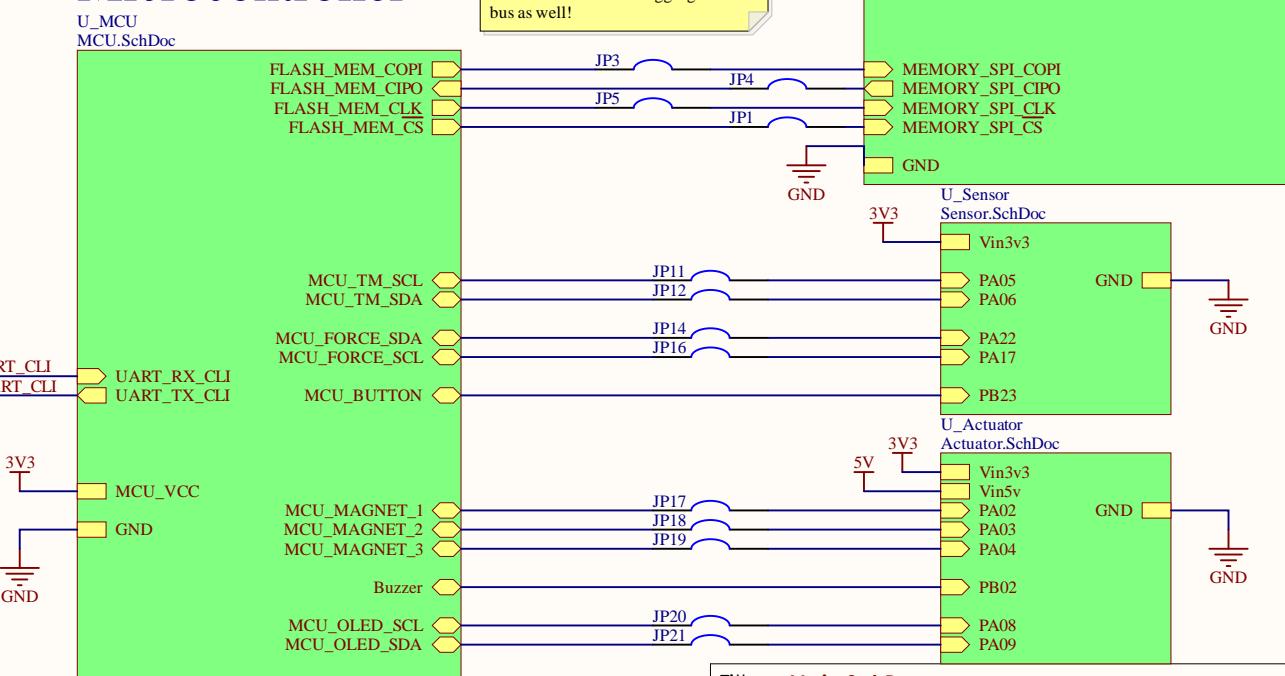


USB Connector + FTDI Chip



NOTE:
The FTDI Chip is an useful chip that allows us to convert USART messages into USB signals. It allows us to connect the MCU directly to the USB port of a computer and use the serial terminal (it is the same bridge used on the SAMW25 Xplained Board). The FTDI device also contains protection circuitry for the USB.

Microcontroller

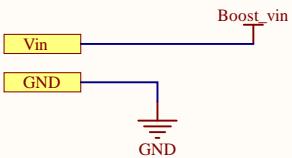


Title: **Main.SchDoc**

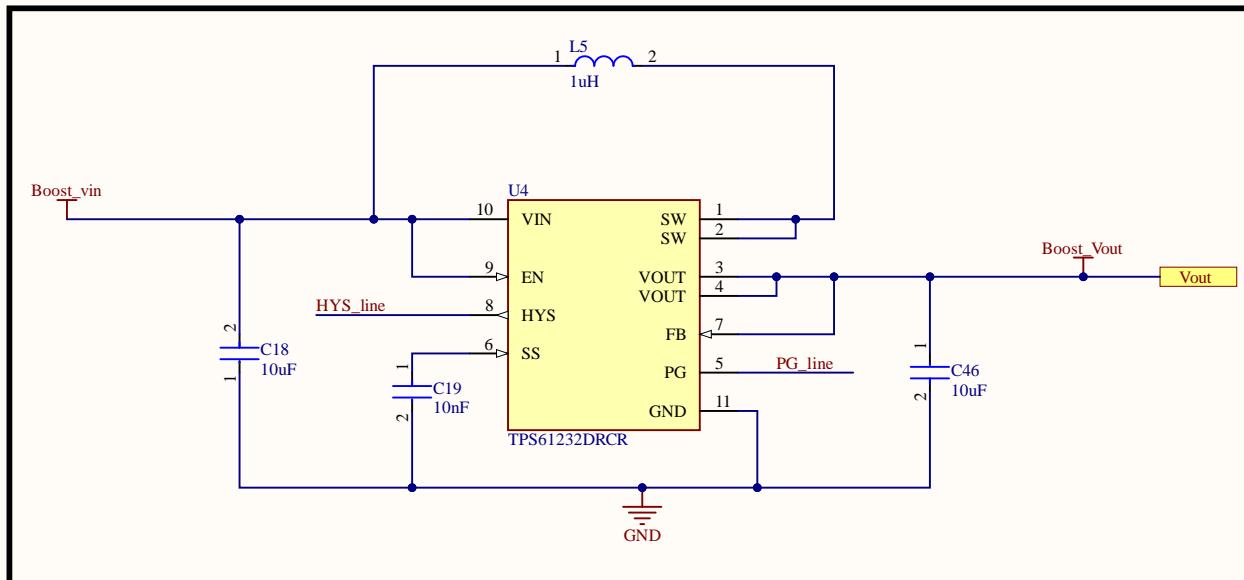
Desc:

Size: Letter	Auth: Huawei Chen/PinYu Yu	Proj: ESE5160_ExampleLayoutProject - Team1.PnPCB
VCs: Not in version control		
Date: 2024/3/4 19:35:00	AD Ver. 24.1.2.44	Doc. * Sheet 1 of 9
File: C:\Users\marsc\AppData\Local\Temp\Releases\Snapshot\1\Main.SchDoc		Electrical and Systems Engineering

A



BoostConverter



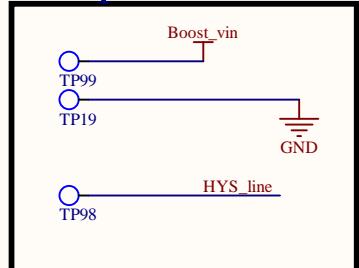
The Boost_vin and Ground is using a through hole test point.
The HYS is using a Surface mount test point.
The PG is connected to a LED to see if function or not

B

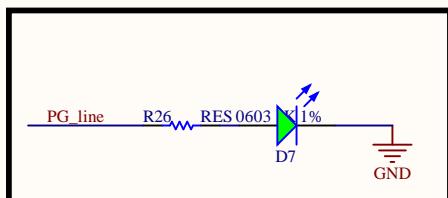
C

D

Testpoints



Boost PG LED



Title: **BoostConverter.SchDoc**

Desc:

Size: Letter

Auth: PinYi Yu

Proj: ESE5160_ExampleLayoutProject - Team1.Pcb

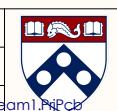
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Date: 2024/3/4 19:35:00

AD Ver. 24.1.2.44

Doc. *

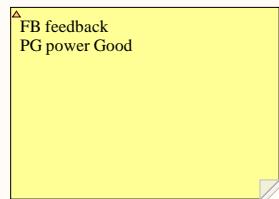
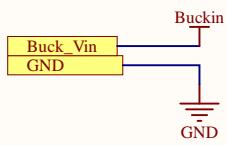
Sheet 2 of 9



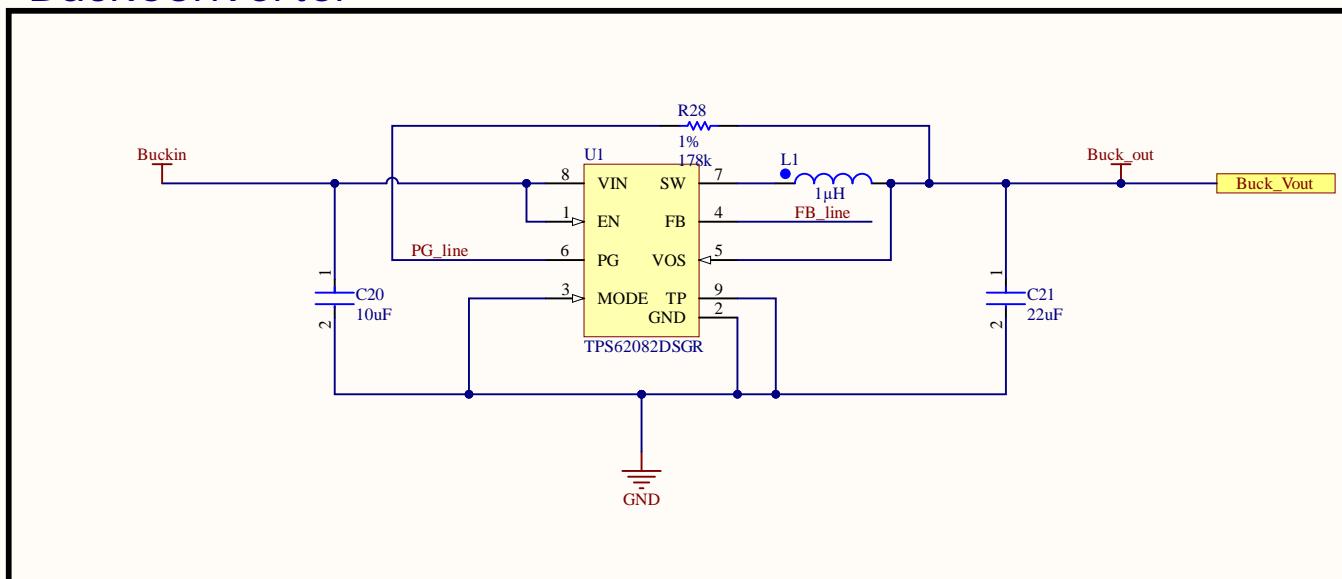
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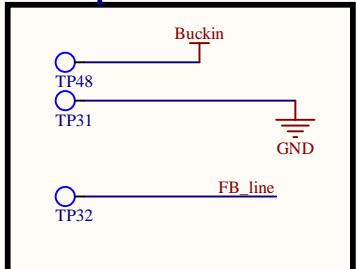
BuckConverter



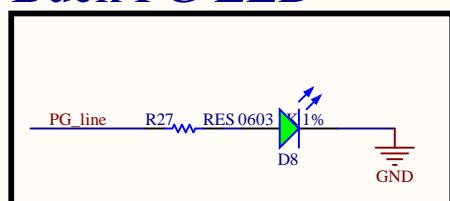
C

[▲]The Buckin and GND is using a through hole test point.
The FB is using a Surface mount test point.
The PG is connected to a LED to see if functioning or not.

Testpoints



Buck PG LED



Title: **BuckConverter.SchDoc**

Desc:

Size: Letter Auth: Huawei Chen

Proj: ESE5160_ExampleLayoutProject - Team1.Pcb

VCS: Not in version control

Date: 2024/3/4 19:35:00 AD Ver. 24.1.2.44 Doc. *

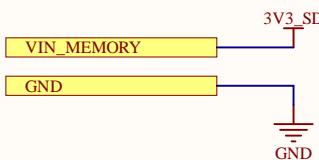
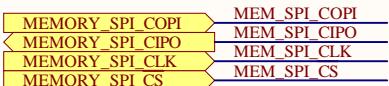
Sheet 3 of 9



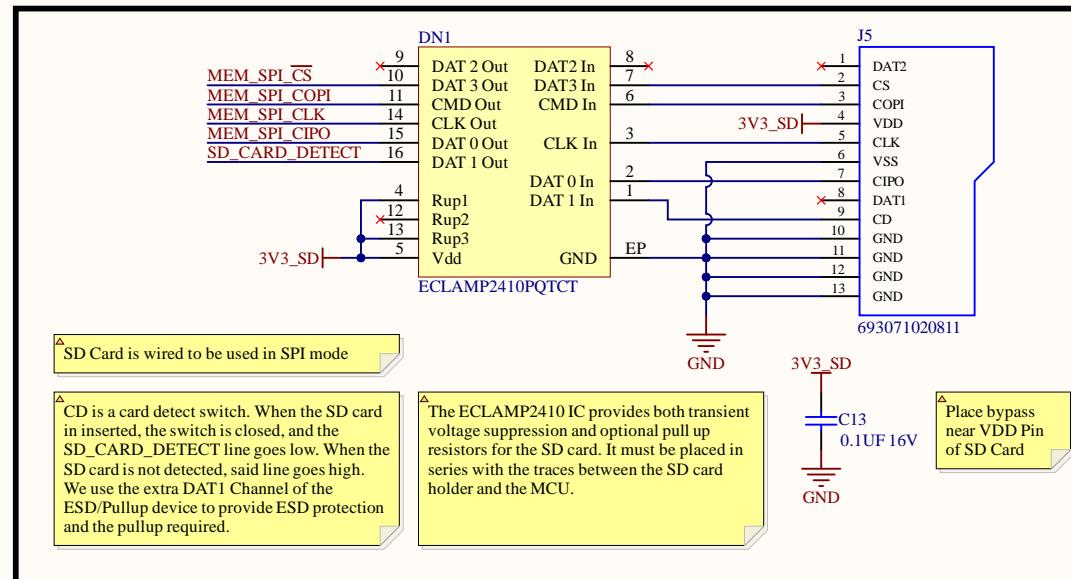
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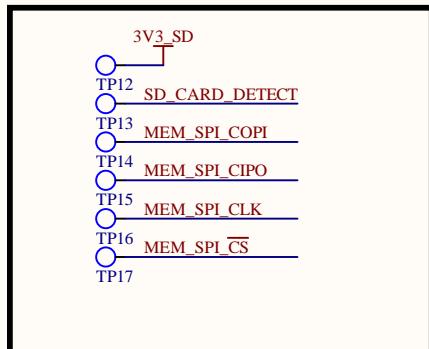
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SD CARD



TESTPOINTS

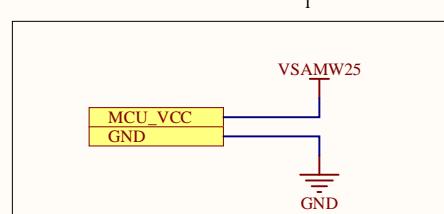


Title: Memory.SchDoc		
Desc:		
Size: Letter	Auth: HuaweiChen/PinYu Yu	Proj: ESE5160_ExampleLayoutProject - Team1.PjBob
VCS: Not in version control		www.seas.upenn.edu
Date: 2024/3/4 19:35:00		AD Ver. 24.1.2.44 Doc. * Sheet 4 of 9
File: C:\Users\marsc\AppData\Local\TempReleases\Snapshot\1\Memory.SchDoc		



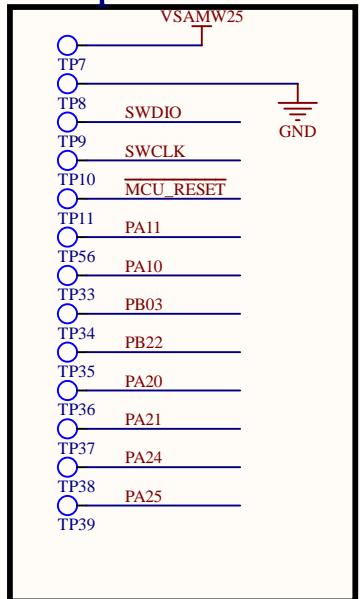
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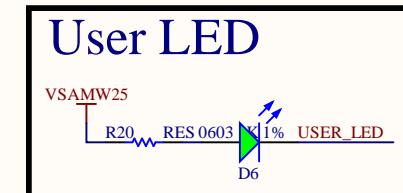


MCU_TM_SCL	PA05
MCU_TM_SDA	PA06
MCU_MAGNET_1	PA02
MCU_MAGNET_2	PA03
MCU_MAGNET_3	PA04
Buzzer	PA22
MCU_FORCE_SCL	PA17
MCU_FORCE_SDA	PA08
MCU_OLED_SCL	PA09
MCU_OLED_SDA	PA10
MCU_BUTTON	USER_BUTTON

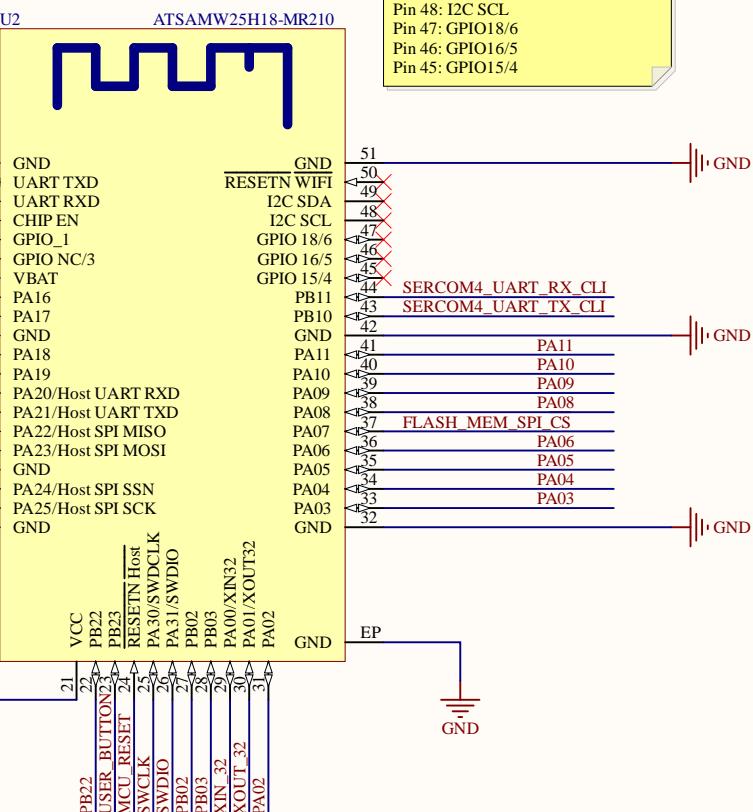
Testpoints



All of the test points are through hole



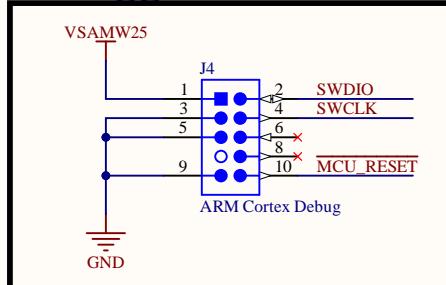
The following pins attach to the WINC1500, not the SAMD21, and must not be used in the design:
Pin 6: GPIO NC/3
Pin 5: GPIO_1
Pin 4: CHIP EN



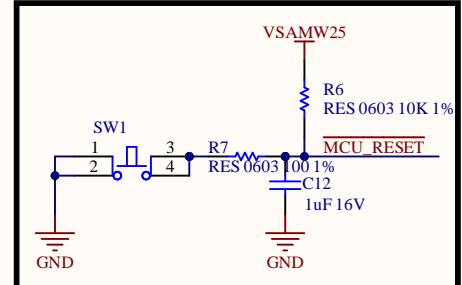
The following pins attach to the WINC1500, not the SAMD21, and must not be used in the design:
Pin 50: RESETN_WIFI
Pin 49: I2C SDA
Pin 48: I2C SCL
Pin 47: GPIO18/6
Pin 46: GPIO16/5
Pin 45: GPIO15/4

SERCOM1_PAD2_SPI_CIPO	FLASH_MEM_CIPO
SERCOM1_PAD2_SPI_COPI	FLASH_MEM_CPO
SERCOM1_PAD3_SPI_SCK	FLASH_MEM_CLK
FLASH_MEM_SPI_CS	FLASH_MEM_CS
SERCOM4_UART_RX_CLI	UART_RX_CLI
SERCOM4_UART_TX_CLI	UART_TX_CLI

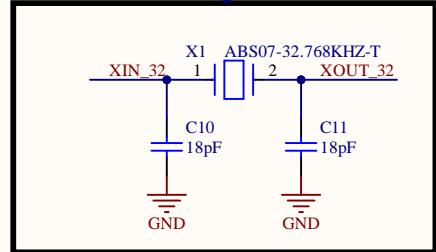
Debugger Port



Reset Button



32.768 Crystal



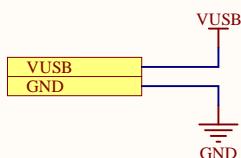
Calculation of crystal load capacitors:
Cext = 2x (Ccrystal - Cpara - Cpcb)
Ccrystal = 12.5pF (from crystal datasheet)
Cpara = 3.15pF (from MCU datasheet)
Cpcb = 0.5pF (estimate)
Cext = 2x(12.5pF - 3.15pF - 0.5pF) = 17.7pF

Title: **MCU.SchDoc**

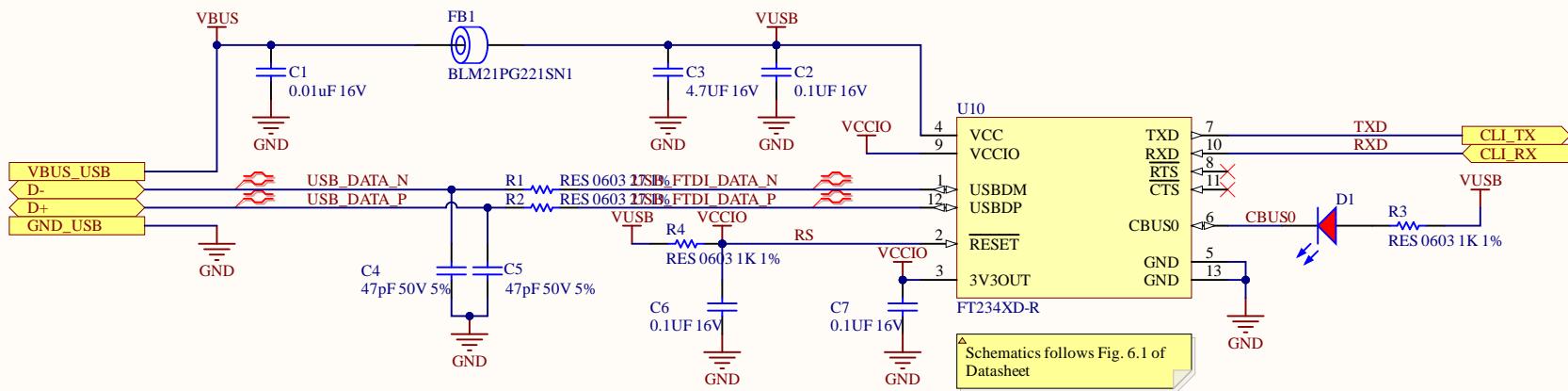
Desc:

Size: Letter	Auth: Huawei Chen/PinYi Yu	Proj: ESE5160_ExampleLayoutProject - Team1.Pcb
VCS: Not in version control		
Date: 2024/3/4 19:35:00	AD Ver. 24.1.2.44	Doc: * Sheet 5 of 9
File: C:\Users\marsc\AppData\Local\Temp\Releases\Snapshot\1\MCU.SchDoc		Electrical and Systems Engineering

A



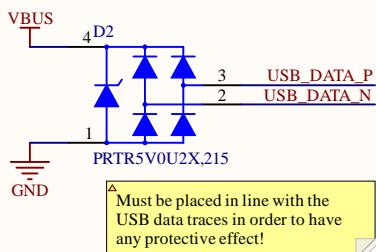
USB to Serial FTDI Chip



B

C

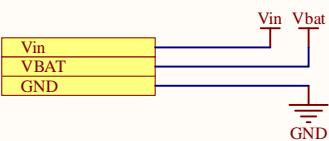
USB ESD Protection



D

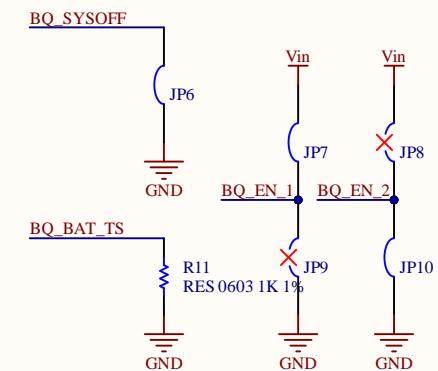
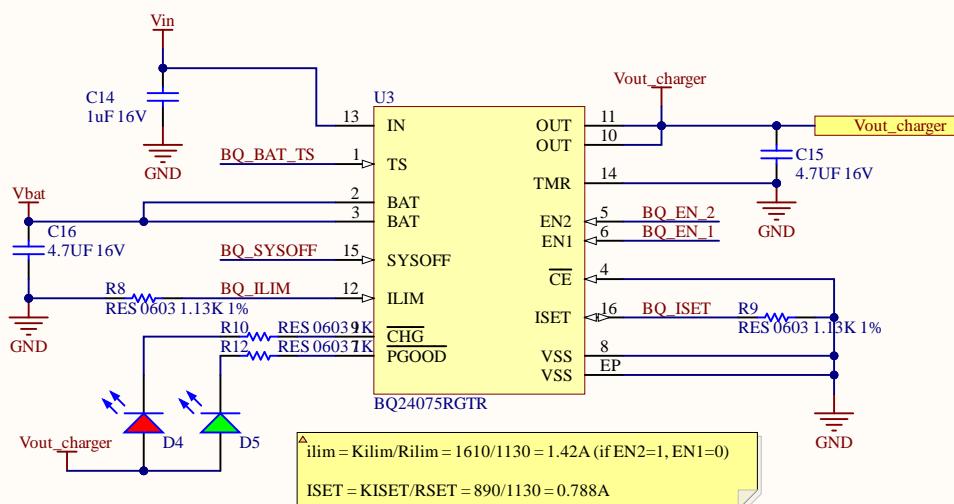
Title: FTDI.SchDoc		Penn Engineering UNIVERSITY OF PENNSYLVANIA
Desc:		
Size: Letter	Auth: Huawei Chen/PinYi Yu	Proj: ESE5160_ExampleLayoutProject - Team1.Pcb
VCS: Not in version control		www.seas.upenn.edu
Date: 2024/3/4 19:35:01	AD Ver. 24.1.2.44	Electrical and Systems Engineering
File: C:\Users\marsc\AppData\Local\TempReleases\Snapshot\1\FTDI.SchDoc		

A



Δ Please see Table 1 of BQ24075 FOR current setup. You can change BQ EN1 and BQ EN 2 if you want! Currently with BQ EN 1 = 1 and BQ EN 2 = 2, the current from the USB is limited to 500 mA.

B



C

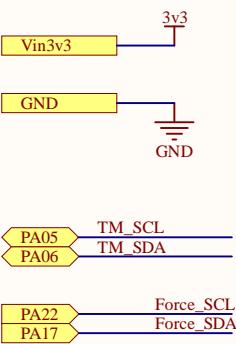
D

Title: *LiPo_Charger.SchDoc*

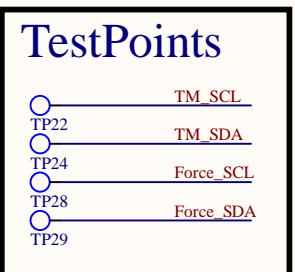
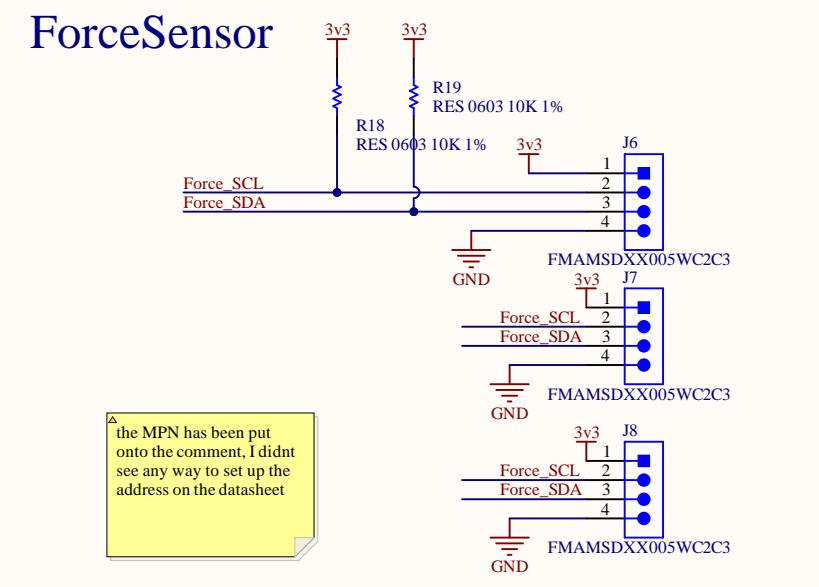
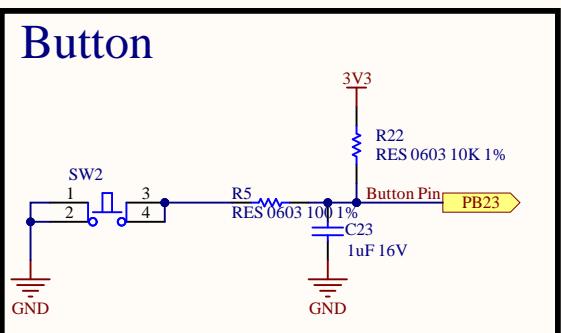
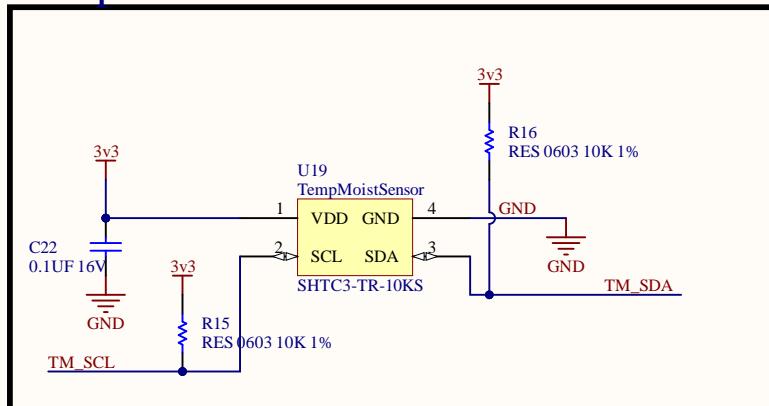
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VCS: Not in version control		
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File: C:\Users\marsc\AppData\Local\TempReleases\Snapshot\1\LiPo_Charger.SchDoc		www.seas.upenn.edu Electrical and Systems Engineering





TempMoistSensor



Title: **Sensor.SchDoc**

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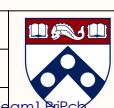
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VCS: Not in version control

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Sheet 8 of 9 File: C:\Users\marsc\AppData\Local\TempReleases\Snapshot\1\Sensor.SchDoc

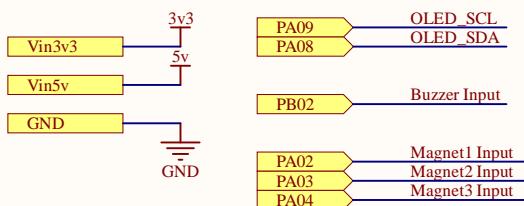


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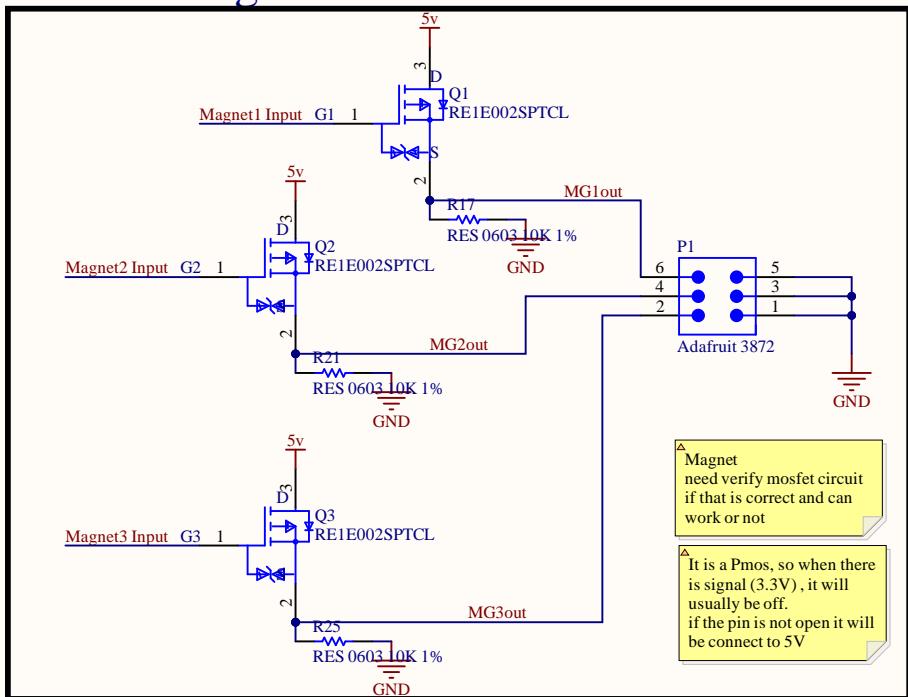
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A



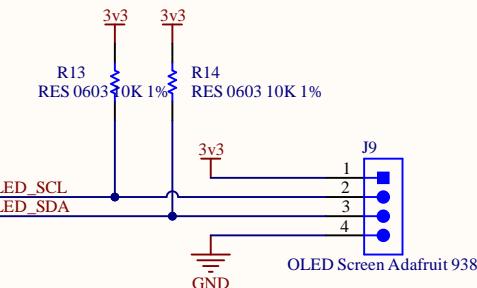
Electric Magnets



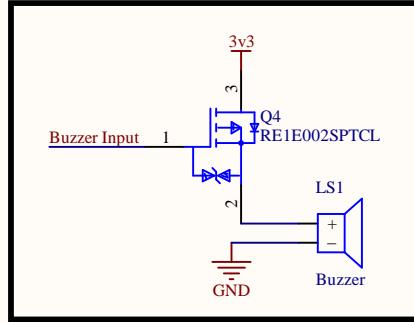
Testpoints

TP76	OLED_SCL
TP23	OLED_SDA
TP25	MG1out
TP26	MG2out
TP27	MG3out

OLED Screen



Buzzer



Title: **Actuator.SchDoc**

Desc:

Size: Letter	Auth: Huawei Chen/PinYi Yu	Proj: ESE5160_ExampleLayoutProject - Team1.Pcb
VCS: Not in version control		
Date: 2024/3/4 19:35:01	AD Ver. 24.1.2.44	Doc. * Sheet 9 of 9



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A B C D E F

Four (4) Layers
Dimensions: 67x84
Thickness: 1.53mm
Material: PP-006; Core-009
All layers are unmirrored - should be able to "see straight through"
Scoring: Yes

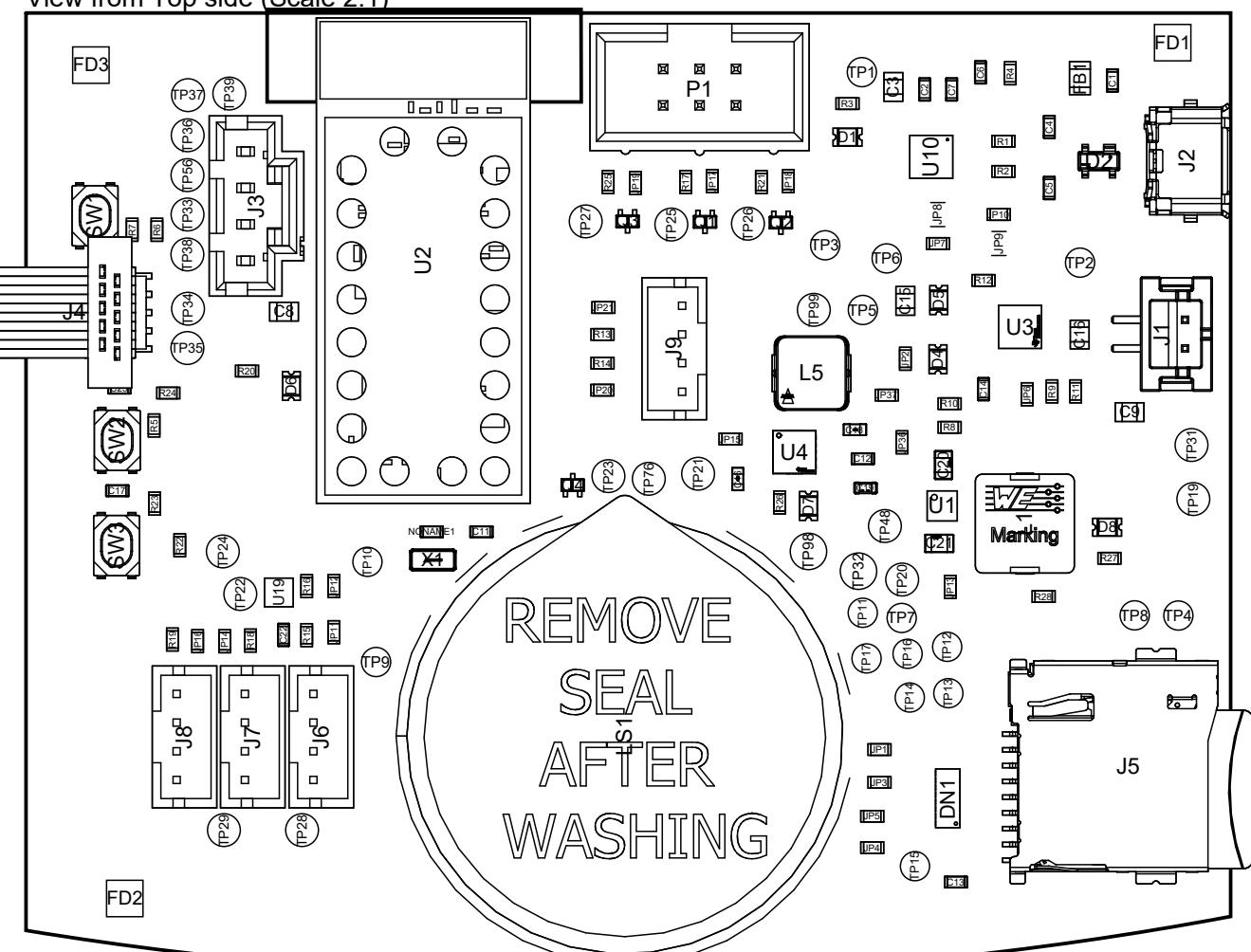
Finished Thickness: 1.53mm
Surface Finish: ENIG
Gold Fingers: Yes
Outer Layer Finish Copper: 1oz
Inner Copper: 0.5oz
Number of Holes Per Board: 351
Minimum Hole size: 0.20mm
Minimum Trace (Outer layer): 6mil
Minimum Space (Outer layer): 6mil
Minimum Trace (Inner layer): None (no Trace)
Minimum Space (Inner layer): None (no Trace)
Solder Mask: Yes
Solder Mask Sides: Top and Bottom
Solder Mask Color: Green
Solder Mask Type: LPI
Solder Mask Finish: Standard (Semi-Gloss)
Silk Screen: Yes
Logo Allowed: Silk Screen
Silk Screen Sides: Top and bottom
Silk Screen Color: White
Internal Slots: No
Counter Sink: No
Counter Bore: No
Edge Plating: No
Route and Retain: N/A
Scoring: N/A
Controlled Impedance: No
Controlled Dielectric: No
Thru-Hole Via in Pad: No
Thickness Tolerance: +/-10%
UL Marking Required: No
Rohs Marking: No
ITAR?: No

Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Surface Material	Top Overlay			Legend	GTO
	Copper	Top Solder	0.03mm	Solder Resist	Solder Mask	GTS
	Copper	Top Layer	0.04mm		Signal	GTL
	Prepreg		0.33mm	PP-006	Dielectric	
	CF-004	GroundPlane	0.02mm		Signal	G1
	Core		0.71mm	Core-009	Dielectric	
	CF-004	PowerPlane	0.02mm		Signal	G2
	Prepreg		0.33mm	PP-006	Dielectric	
	Copper	Bottom Layer	0.04mm		Signal	GBL
	Surface Material	Bottom Solder	0.03mm	Solder Resist	Solder Mask	GBS
		Bottom Overlay			Legend	GBO

Total thickness: 1.53mm

View from Top side (Scale 2:1)



A

B

C

D

E

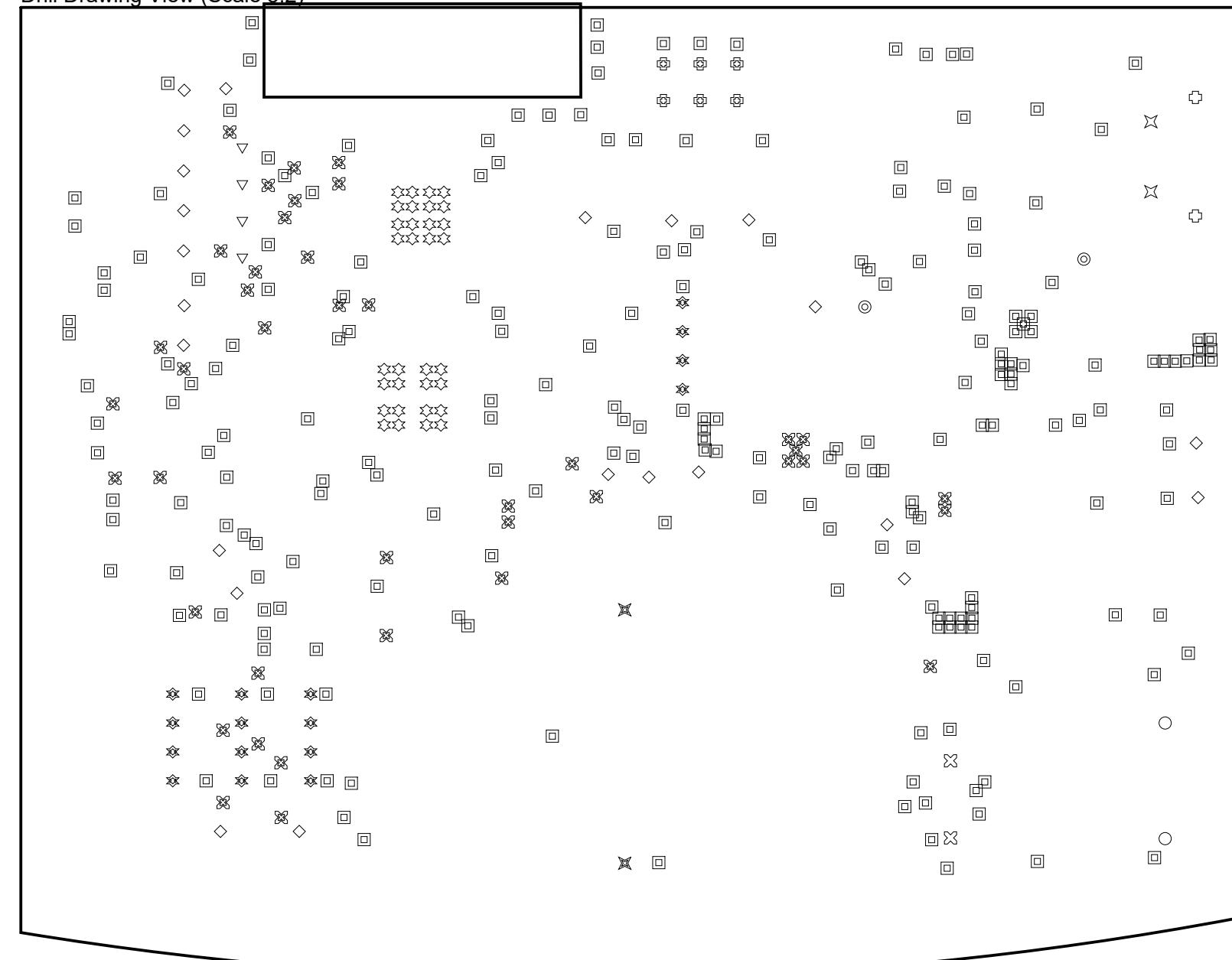
F

A B C D E F

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
✖	41	0.20mm	Plated	
◻	219	0.20mm	Plated	
✖	32	0.25mm	Plated	
✖	2	0.32mm	Plated	
✖	2	0.65mm	Plated	
◎	2	0.69mm	Plated	
✚	2	0.70mm	Plated	
▽	4	0.89mm	Plated	
✖	16	0.90mm	Plated	
○	2	0.90mm	Non-Plated	
◇	23	1.02mm	Plated	
✖	6	1.10mm	Plated	
✖	2	1.20mm	Plated	
353 Total				

Drill Drawing View (Scale 5:2)



A B C D E F

A

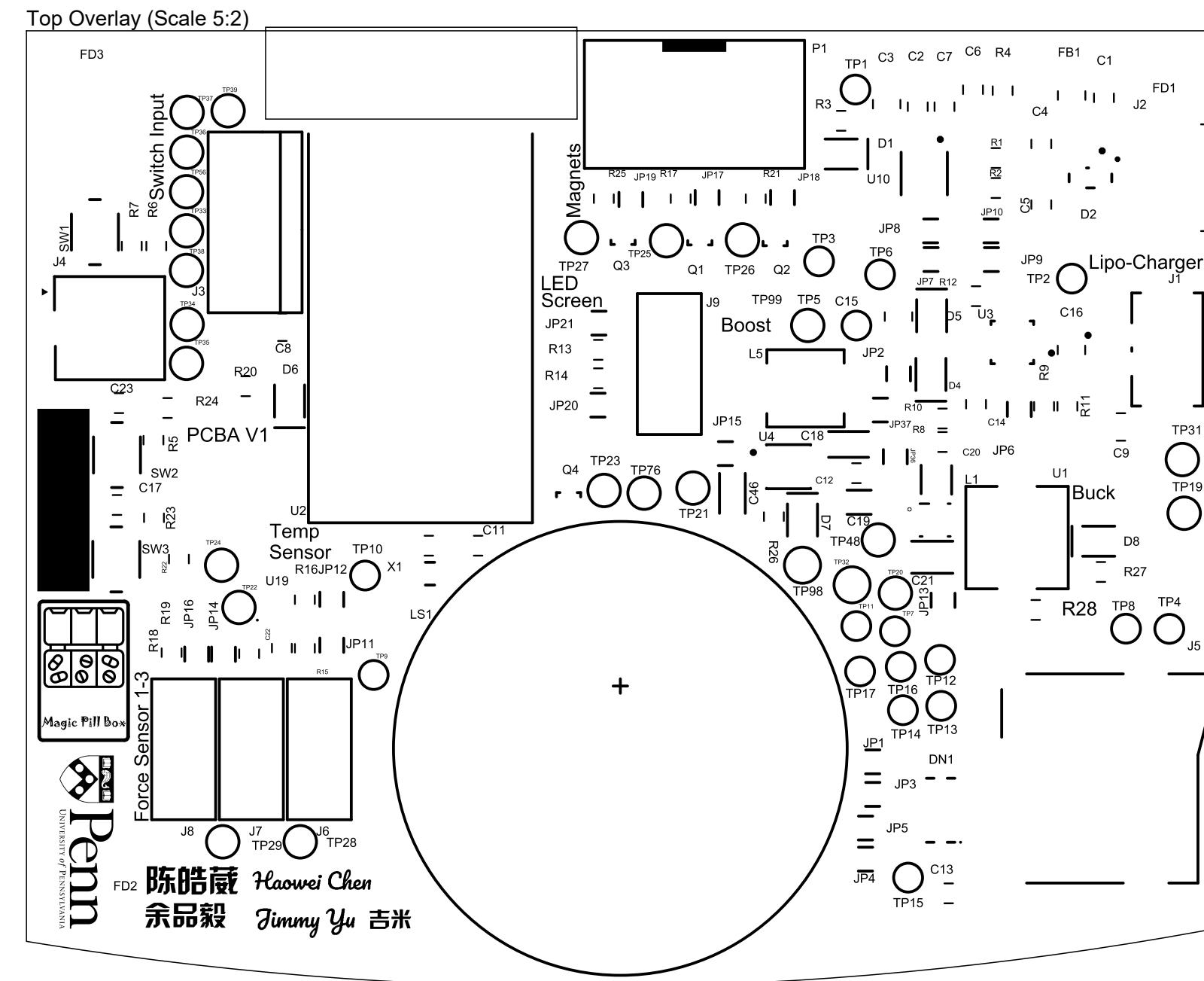
B

C

D

E

F

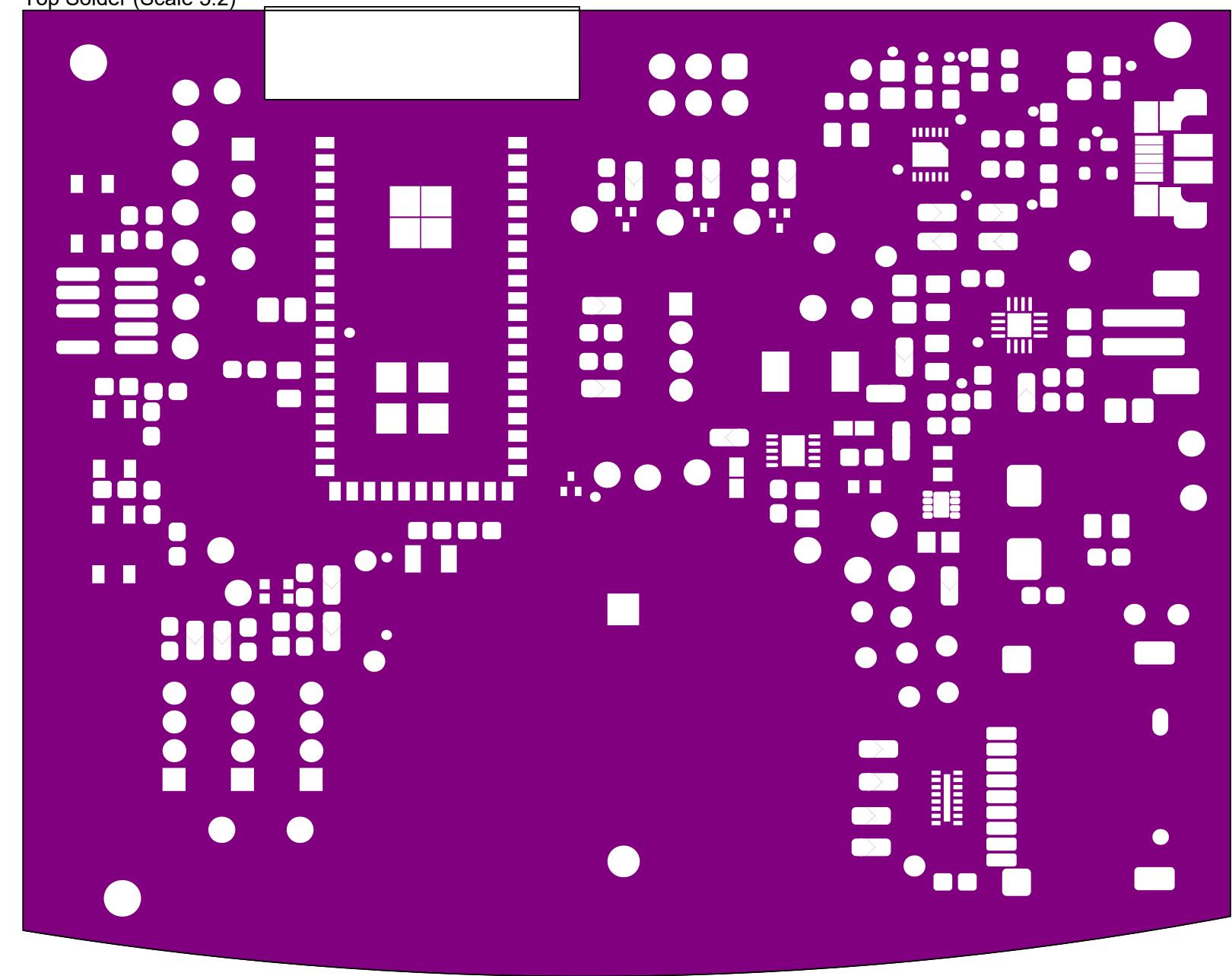


A B C D E F

1

1

Top Solder (Scale 5:2)



2

2

3

3

4

4

Title: StarterBoardFabrication.PCBDwf		Penn Engineering	
Desc:		UNIVERSITY OF PENNSYLVANIA	
Size: Letter	Auth: *	Proj: ESE5160_ExampleLayoutProject - Team1.PCB	www.seas.upenn.edu
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A B C D E F

A

B

C

D

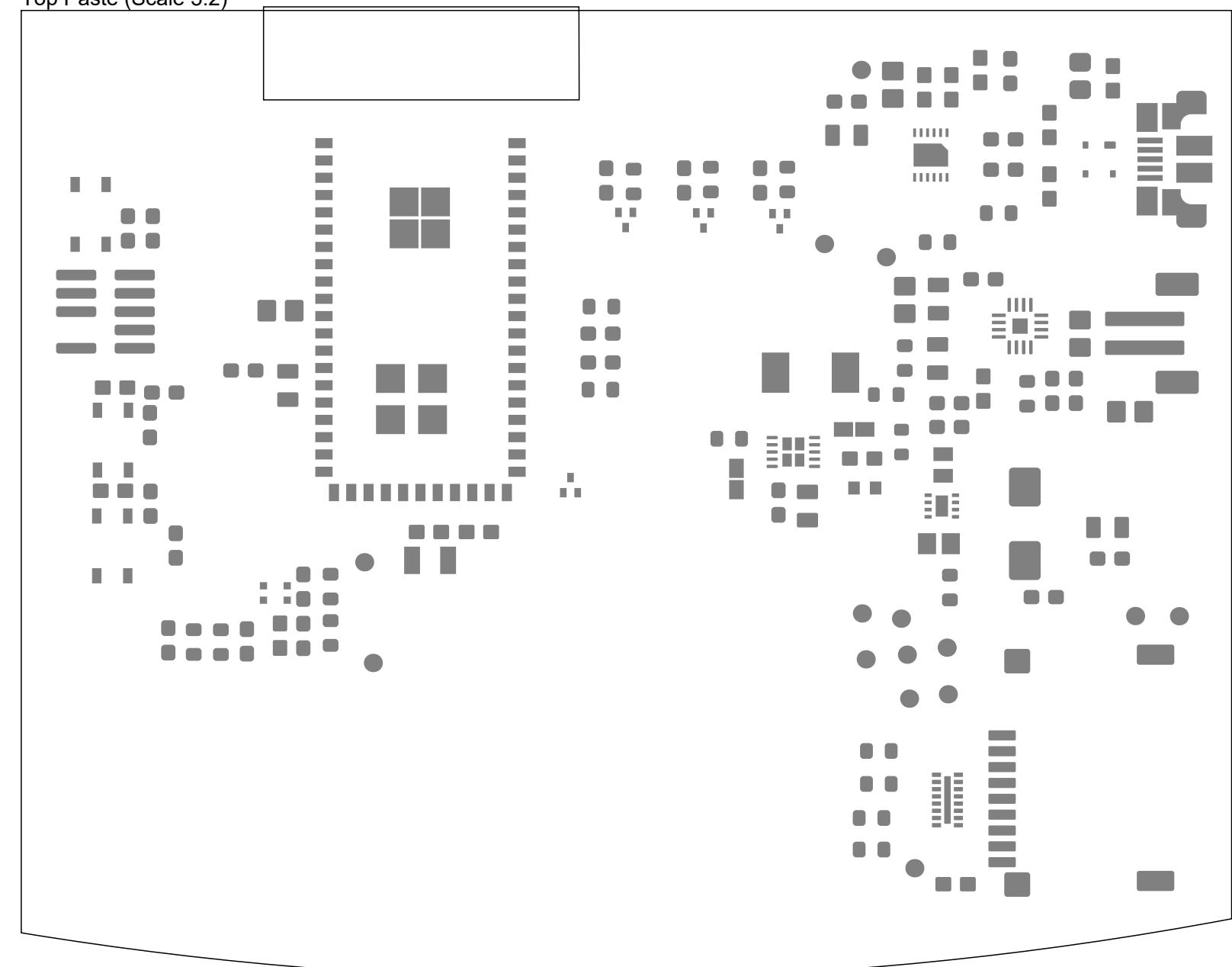
E

F

1

1

Top Paste (Scale 5:2)



2

2

3

3

4

4

A

B

C

D

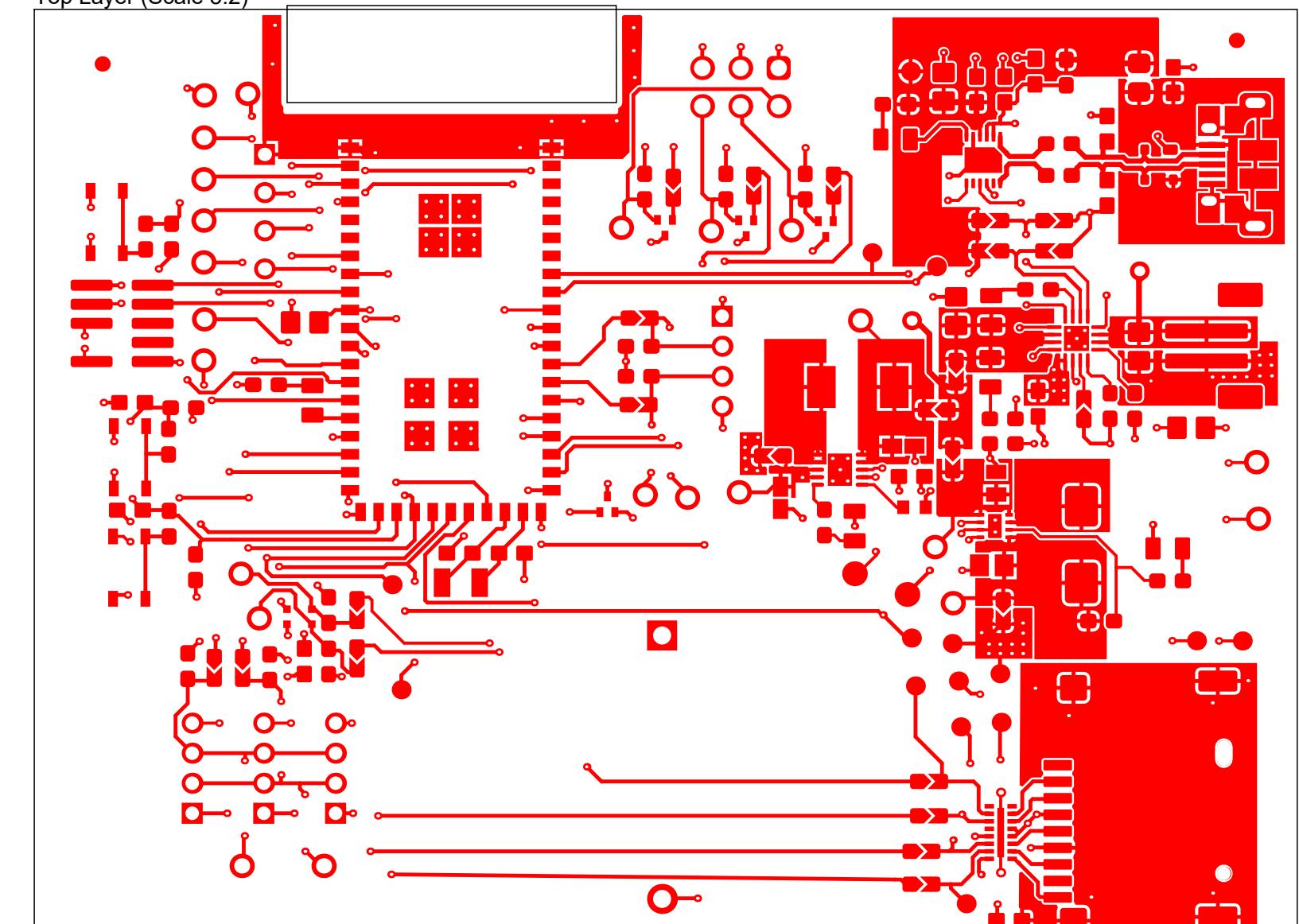
E

F

A B C D E F

1
2
3
4

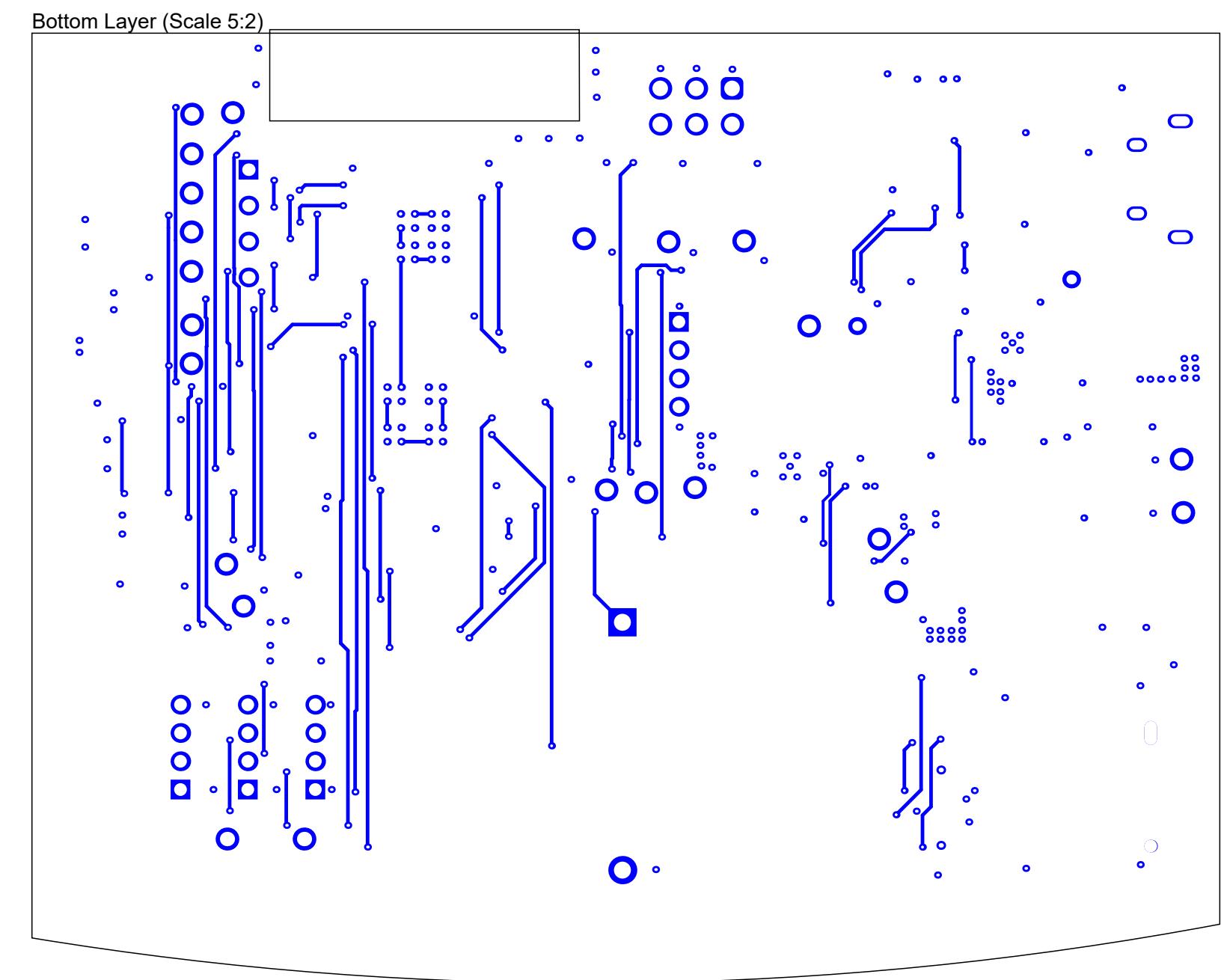
Top Layer (Scale 5:2)



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A B C D E F

A B C D E F



Title: StarterBoardFabrication.PCBDwf		Penn	
Desc:		Engineering	
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A B C D E F

A

B

C

D

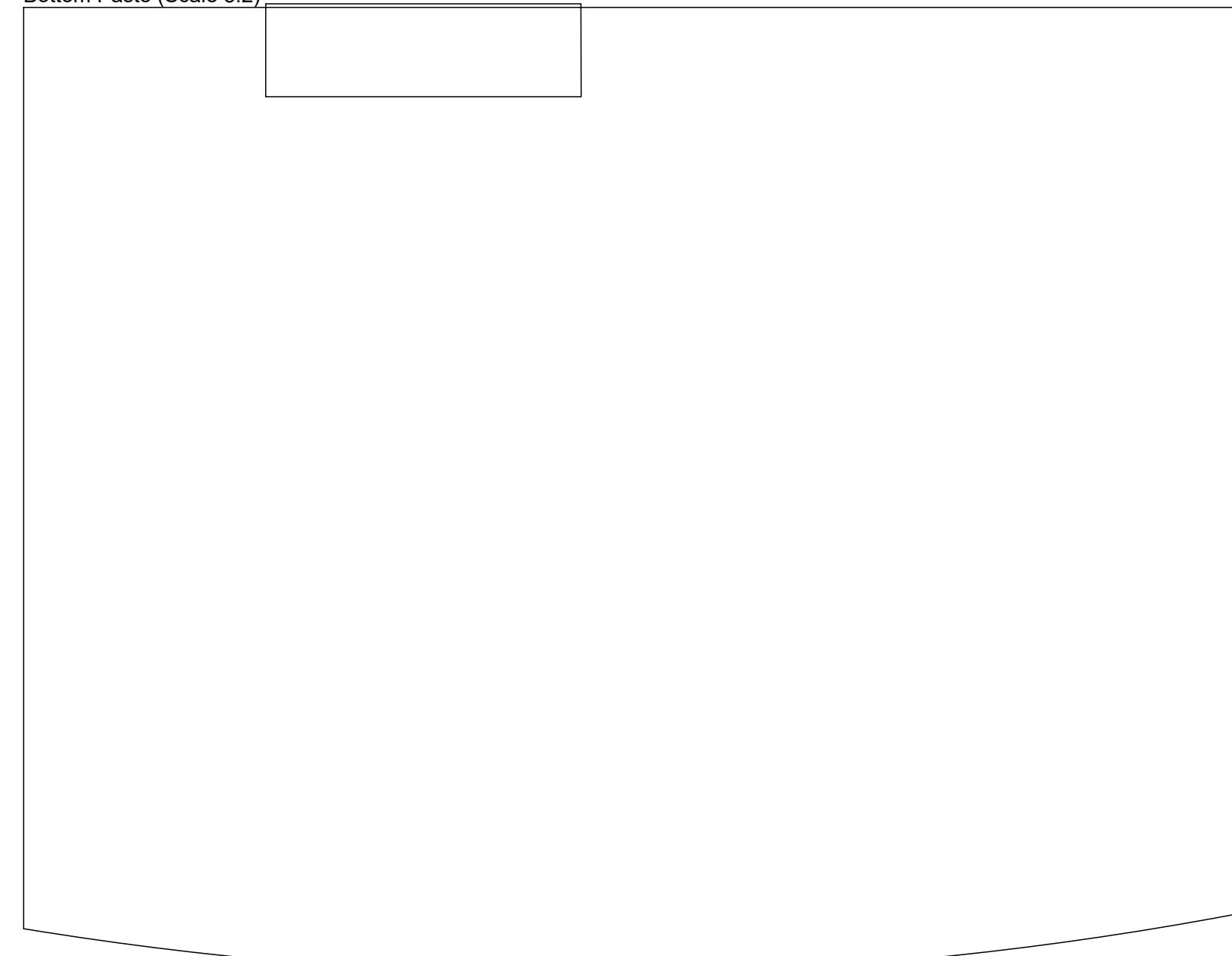
E

F

1

1

Bottom Paste (Scale 5:2)



2

2

3

3

4

4

Title: StarterBoardFabrication.PCBDwf	Penn
Desc:	Engineering
Size: Letter	Auth: *
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A

B

C

D

E

F

A

B

C

D

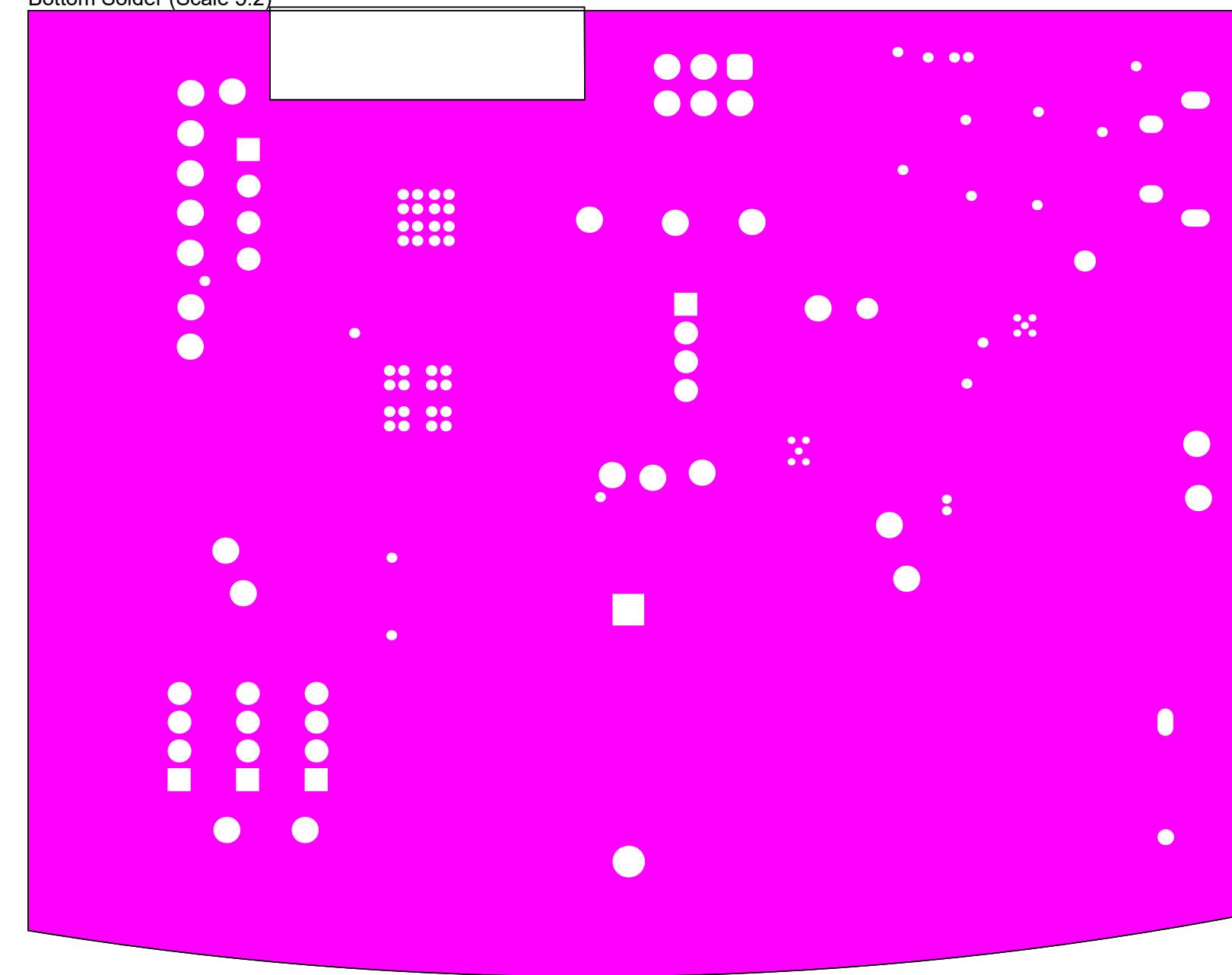
E

F

1

1

Bottom Solder (Scale 5:2)



2

2

3

3

4

4

Title: StarterBoardFabrication.PCBDwf		Penn Engineering	
Desc:		UNIVERSITY OF PENNSYLVANIA	
Size: Letter	Auth: *	Proj: ESE5160_ExampleLayoutProject - Team1.PCB	www.seas.upenn.edu
=VCS: '+VersionControl_ProjFolderRevNumber			Electrical and Systems Engineering
=Date: '+CurrentDate+'	CurentName+ApplianceName+BuildNumber		
=File: '+DocumentFullPathAndName			

A

B

C

D

E

F

A

B

C

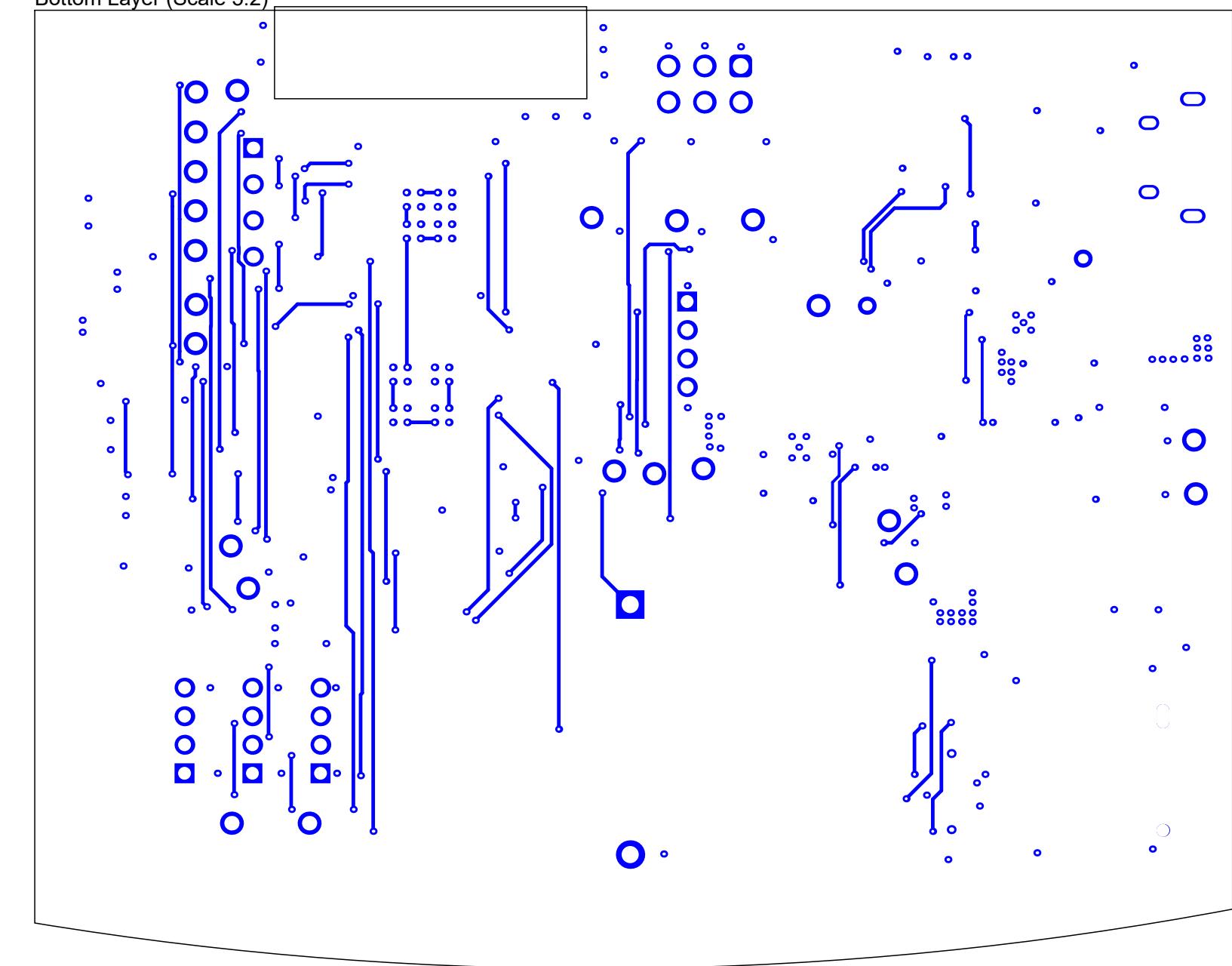
D

E

F

1
2
3
41
2
3
4

Bottom Layer (Scale 5:2)



A

B

C

D

E

F

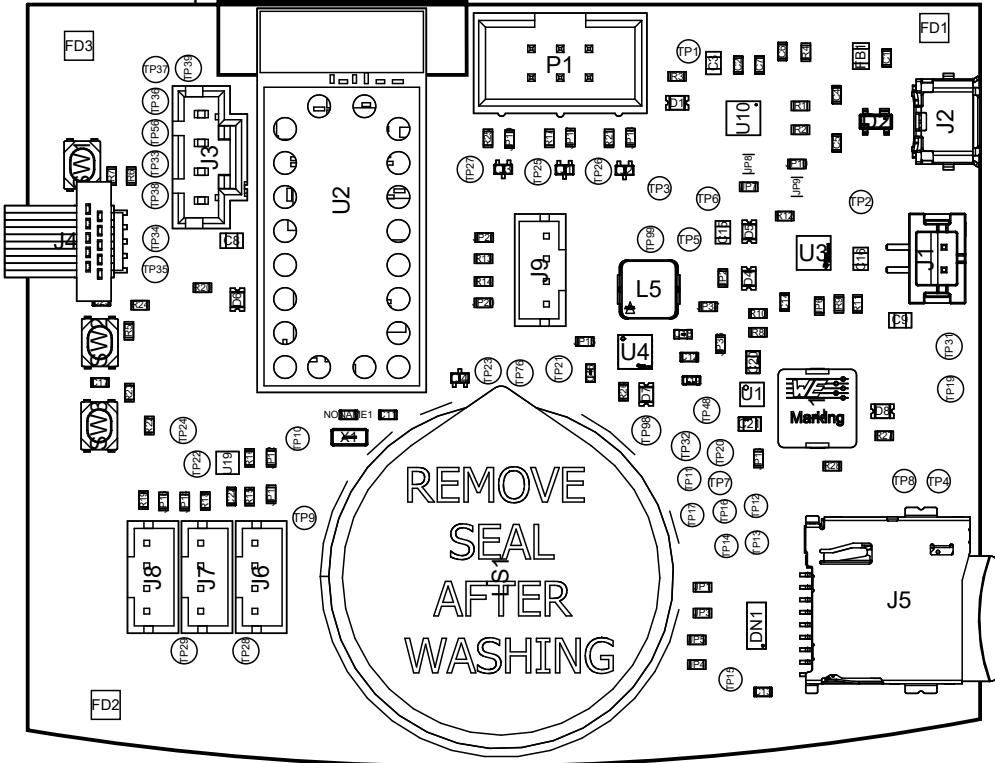
A

B

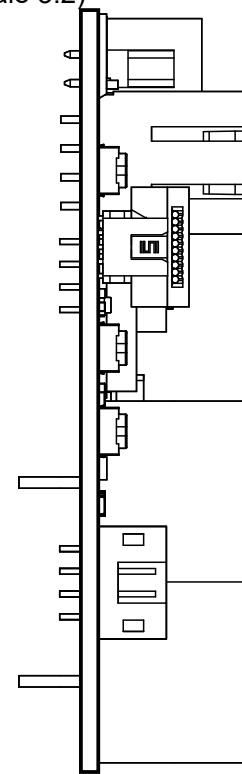
C

D

View from Top side (Scale 3:2)



View from Left side (Scale 3:2)



Title: **StarterBoardAssembly.PCB**

Desc:

Size:Letter

Auth:*

Proj:ESE5160_ExampleLayoutProject - Team1.PPCB

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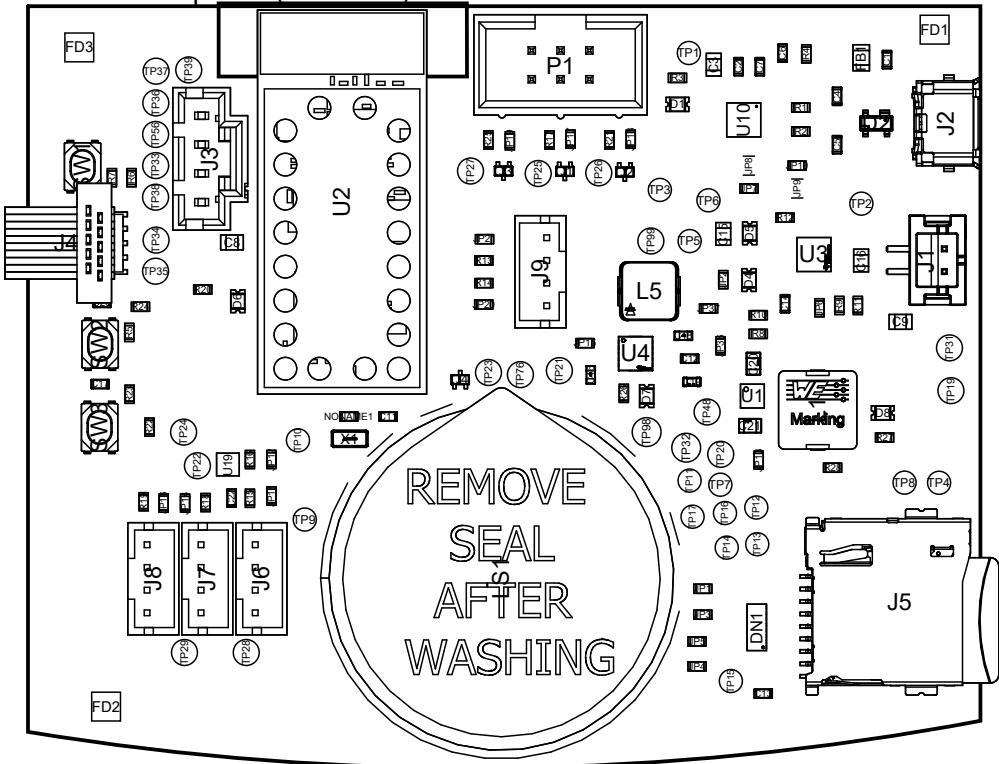
A

B

C

D

View from Top side (Scale 3:2)



Realistic View

Title: **StarterBoardAssembly.PCDBdwf**

Desc:

Size:Letter

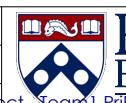
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Proj:ESE5160_ExampleLayoutProject - Team1.PPCB

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A

B

C

D