Notes	Port name	Offset	15	14	13 Bit	12	11	10	9	8	7	6	5
Input port/Function 1 = pullup, 0 = pulldown 0 = input, 1 = output 0 = I/O, 1 = Peripheral 1 = Pull Enabled	P1IN PxOUT PxDIR PxSEL PxREN	0x20 0x21 0x22 0x26 0x27	×	×	×	×	×	×	×	× Port	1 is	not c	conne
Input port/Function 1 = pullup, 0 = pulldown 0 = input, 1 = output 0 = I/O, 1 = Peripheral 1 = Pull Enabled	P2IN PxOUT PxDIR PxSEL PxREN	0x28 0x29 0x2A 0x2E 0x2F	×	×	×	×	×	×	×	×	ooo UART CTS		0 L X UART RXD
Input port/Function 1 = pullup, 0 = pulldown 0 = input, 1 = output 0 = I/O, 1 = Peripheral 1 = Pull Enabled	P3IN PxOUT PxDIR PxSEL PxREN		×	×	×	×	×	×	×	×			
Input port/Function 1 = pullup, 0 = pulldown 0 = input, 1 = output 0 = I/O, 1 = Peripheral 1 = Pull Enabled	P4IN PxOUT PxDIR PxSEL PxREN	0x1C 0x1D 0x1E 0x1F 0x10	×	×	×	×	×	×	×	×	ooo DSCSW_STS	0 0 1 OOT_EN	×

Input port/Function 1 = pullup, 0 = pulldown 0 = input, 1 = output 0 = I/O, 1 = Peripheral 1 = Pull Enabled	P5IN PxOUT PxDIR PxSEL PxREN	0x30 0x31 0x32 0x33 0x12	×	×	×	×	×	×	×	×			ooo R03 (unused)
Input port/Function 1 = pullup, 0 = pulldown 0 = input, 1 = output 0 = I/O, 1 = Peripheral 1 = Pull Enabled	P6IN PxOUT PxDIR PxSEL PxREN		×	×	×	×	×	× Poi	× t 6 n	× ot pa	ırt of	this	proce
Input port/Function 1 = pullup, 0 = pulldown 0 = input, 1 = output 0 = I/O, 1 = Peripheral 1 = Pull Enabled	P7IN PxOUT PxDIR PxSEL PxREN	0x38 0x3A 0x3C 0x3E 0x14	×	×	×	×	×	×	×	×	0 0 1 LED4	0 0 L LED3	0 0 1 LED2
Input port/Function 1 = pullup, 0 = pulldown 0 = input, 1 = output 0 = I/O, 1 = Peripheral 1 = Pull Enabled	P8IN PxOUT PxDIR PxSEL PxREN	0x39 0x3B 0x3D 0x3F 0x15	×	×	×	×	×	×	×	×	OOOO TCD DO	ooo CCD D1	ooo CCD D2
Input port/Function	P9IN	0x08	×	×	×	×	×	×	×	×	LED12	LED11	LED10

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1 = pullup, 0 = pulldown 0 = input, 1 = output 0 = I/O, 1 = Peripheral 1 = Pull Enabled	PxOUT PxDIR PxSEL PxREN	0x0A 0x0C 0x0E 0x16									1 1 0 0 0	1 1 0 0	1 1 0 0
Input port/Function 1 = pullup, 0 = pulldown 0 = input, 1 = output 0 = I/O, 1 = Peripheral 1 = Pull Enabled	P10IN PxOUT PxDIR PxSEL PxREN	0x09 0x0B 0x0D 0x0F 0x17	×	×	×	×	×	×	×	×	×	×	×

4	3	2	1	0	10/
					Word.
ected					
O L X UART TXD				UART RTS	This is UCA0. Also, CTS and RTS are connected as general logic
X 1 0				1 0 0	0x01 0x30 0x00
	J4 SCLK	J4 MISO	J4 MOSI		This is USB0
	1 1 0	1 1 0	0 1 0		0xC0 0x0E 0x00
×	CS0	CS1	×	QRESET	
	0SO 1 0 0	1 0 0		1 0 0	0x4D 0x00 0x00

LED9	0 0 0	LCD D3	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
LED8	0 0 0	LCD D4	o o o /Cl, /PBIN	
LED7	0 0 0	CD D5	o 0 Buffer DIR	
LED6	0 0 0	PCD D6	O O L LCD_BKLT	
LED5	0 0 0	CD D7	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SVSIN (unused)
	0x00 0x00 0x00	Yes, bits are backwards. Also, this is a bi-directional bus.	0x00 0x00 0x00 0xF0 0xF7 0x00 0x00	

1 1	1	1 1	1 1	1 1	0xFF 0xFF
0 0	0	0	0	0	0x00
0	0	0	0	0	0x00
×	1 0 0	M/W 1 1 0 0	Ш 0 1 0	NO T / CD ON 0	0x05 0x0F 0x00 0x00