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Fire-Flyer AI-HPC: A Cost-Effective Software-Hardware Co-Design for Deep Learning

Wei An, Xiao Bi, Guanting Chen, Shanhuang Chen,Chengqi Deng, Honghui Ding, Kai Dong, Qiushi Du, Wenjun Gao, Kang Guan, Jianzhong Guo, Yongqiang Guo, Zhe Fu, Ying He, Panpan Huang, Jiashi Li, Wenfeng Liang, Xiaodong Liu, Xin Liu, Yiyuan Liu, Yuxuan Liu, Shanghao Lu, Xuan Lu, Xiaotao Nie, Tian Pei, Junjie Qiu, Hui Qu, Zehui Ren, Zhangli Sha, Xuecheng Su, Xiaowen Sun, Yixuan Tan, Minghui Tang, Shiyu Wang, Yaohui Wang, Yongji Wang, Ziwei Xie, Yiliang Xiong, Yanhong Xu, Shengfeng Ye, Shuiping Yu, Yukun Zha, Liyue Zhang*, Haowei Zhang, Mingchuan Zhang, Wentao Zhang, Yichao Zhang, Chenggang Zhao, Yao Zhao, Shangyan Zhou, Shunfeng Zhou, Yuheng Zou

DeepSeek-AI, Beijing, China
research@deepseek.com

***Abstract*—The rapid progress in Deep Learning (DL) and Large Language Models (LLMs) has exponentially increased demands of computational power and bandwidth. This, combined with the high costs of faster computing chips and interconnects, has significantly inflated High Performance Computing (HPC) construction costs. To address these challenges, we introduce the Fire-Flyer AI-HPC architecture, a synergistic hardware-software co-design framework and its best practices. For DL training, we deployed the Fire-Flyer 2 with 10,000 PCIe A100 GPUs, achieved performance approximating the DGX-A100 while reducing costs by half and energy consumption by 40%. We specifically engineered HFReduce to accelerate allreduce communication and implemented numerous measures to keep our Computation-Storage Integrated Network congestion-free. Through our software stack, including HaiScale, 3FS, and HAI-Platform, we achieved substantial scalability by overlapping computation and communication. Our system-oriented experience from DL training provides valuable insights to drive future advancements in AI-HPC.**

***Index Terms*—High Performance Computing, Cost-Effective, All-Reduce, Best Practices, Deep Learning, Machine Learning, Large Language Models, Artificial Intelligence Infrastructure**

I. Introduction

In recent years, Deep Learning (DL) [1] has developed rapidly and is widely used in image recognition, speech recognition, content generation, autonomous driving, and other areas. The rapid development of DL is fundamentally tied to the support rendered by data. Training with copious amounts of data demands massive computational resources. Relying on Moore's Law [2], computer speeds double every two years on average, but the pace of DL far exceeds this speed. In particular, Large Language Models (LLMs) [3]–[7] that have become popular in recent years have exploded the demand for computational resources and memory. The parameters of LLMs can reach tens to thousands of billions, requiring hundreds or thousands of GPUs for training. Although LLM training is challenging, the emerging capabilities resulting from more parameters have shown the benefits of continued model expansion. Since then, researchers have gone down the path of making models bigger and never looked back. To acquire more computational resources, people have to expand more nodes. This leads to a surge in the cost of building AI infrastructure. How to reduce the cost of new data centers and how to build cost-effective clusters are also hot and challenging problems. Moreover, more nodes lead to higher energy consumption, which contradicts this era's goal of reducing carbon emissions and achieving carbon neutrality. Reducing energy consumption is also a challenging problem.

In this paper, leverage our practical experience accumulated over the years to propose cost-effective strategies cost-effective strategies for constructing AI-HPC systems suitable for deep learning and LLMs.

***Fire-Flyer AI-HPC Architecture**:* We have deployed a cluster composed of 10,000 PCIe A100 GPUs for Deep Learning training purposes. Details about the GPU nodes and network topology are provided in Section III-A, where we compare our architecture to the NVIDIA DGX-A100 [8] in terms of cost-effectiveness and lower CO_2 emissions. In contrast, we must invest more in software optimizations to address the performance challenges of the PCIe architecture. The following sections will discuss about software-hardware co-design.

Key Technical Topics in our Architecture

- **Network Co-Design**: The Two-Layer Fat-Tree Network [9] integrates storage and computation network, as shown in Section III-B. The entire network is divided into two zones, and the platform supports cross-zone tasks. To prevent congestion, we employed various network tunings detailed in Section VI-A.
- **HFReduce**: Achieves computation-communication overlap via asynchronous allreduce on the CPU, outperforming NVIDIA Collective Communications Library (NCCL) [10] on our PCIe architecture, as discussed in Section IV.

Authors are listed in alphabetical order of their surnames.

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- **HaiScale**: As described in Section V, optimizes parallelism methods for our PCIe architecture, such as Data Parallelism (DP), Pipeline Parallelism (PP) [11] [12], Tensor Parallelism (TP) [13] [14], Experts Parallelism (EP) [15]–[17], Fully Sharded Data Parallel(FSDP) [18] and Zero Redundancy Optimizer(ZeRO) [19].
- **3FS Distributed File System**: Addresses I/O bottlenecks in big data AI tasks, configures with our communication and network tuning, reduces congestion in storage and computation integrated network topology, as detailed in Section VI-B.
- **HAI Platform** [20]: Offers task scheduling, fault handling, and disaster recovery, enhancing utilization and reducing costs. It provides an open-box solution for deep-learning researchers. It is already open-sourced: https://github.com/HFAiLab/hai-platform

Stability and Robustness: These are crucial topics in HPC. Our systems are equipped with robust mechanisms to handle hardware failures, minimizing downtime and impact on operations. These mechanisms, discussed in Section VII, include:

- Disaster recovery through our checkpoint manager
- A validator utility for detecting hardware failures
- An overview of real hardware failure data from our cluster over the past year.

We hope these insights will be beneficial to industry peers and researchers alike.

Discussion and Future Work: In Section VIII, we address some common questions regarding PCIe architecture, such as congestion control, maintenance cost, and stability compared with other architectures. In Section IX, we propose the next generation of PCIe architecture, which is aimed at Mixture-of-Experts Large Language Models training and primarily utilizes multi-NICs and a Multi-Plane network.

II. Background

A. Evolution of Deep Learning

The revolution in Machine Learning and Deep Learning began in 2012 with AlexNet [21], which outperformed traditional methods in image classification, marking the onset of big data utilization and increased computational demands. The emergence of ResNet [22], with its deeper layers, further broadened the horizons of image processing, truly bringing about the "deep" in "Deep Learning". At the same time, big data-driven model training nudged the evolution of data storage technology, leading to the advent of all-flash SSD distributed file systems.

Fast forward to 2017, Google's Transformer [23] made its grand entry, introducing the concept of "Attention is all you need", shaking up the field of Natural Language Processing (NLP). With the advent of more complex models like AlphaFold [24] and AlphaZero [25] highlighting the need for more computational power and memory, revealing the limitations of traditional FP64 / FP32 computing devices.

Entering the 2020s saw the rise of LLMs as a game-changer in the AI sector. Research indicates that an upscale in the number of language model parameters and computational budget

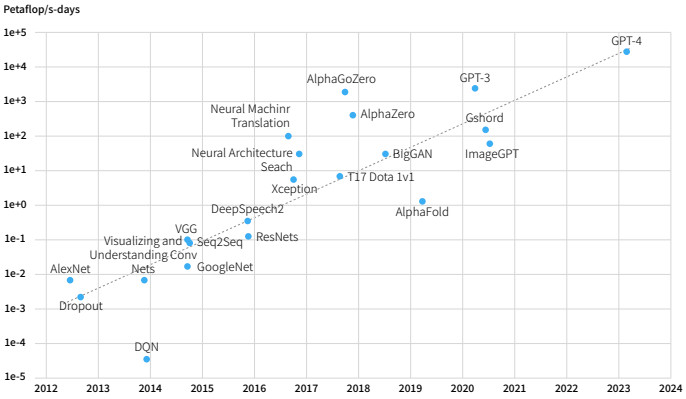


Figure 1: The Exponential Growth of Computational Power for Deep Learning.

can significantly enhance model performance, given adequate training data. Consequently, despite requiring colossal computational resources, efforts are being made to train large models on tens or hundreds of billions or even trillions of parameters. Pioneering examples include GPT-3 [26] and PaLM [27], which occupy close to 1TB of GPU Memory. Recognizing the potential, industry giants have set up large AI clusters to train LLMs while constantly investing in computational power chips.

The shift towards the Mixture-of-Experts (MoE) Models [28]–[30] architecture starting from GPT-4 [7], and the recent AI Generated Content (AIGC) multi-modal (Sora [31]) has amplified the demand for memory and computational resources. However, as AI development outpaces hardware development, leading to skyrocketing training costs, adopting cost-saving solutions has become imperative.

Figure 1 illustrates the exponential growth of computational power for DL. And as summarized in Figure 2 [32], while AI's demand for computational power is growing at 10x per year, Moore's Law lags behind with hardware FLOPs increase at only 3.0x every two years, DRAM bandwidth at 1.6x, and interconnect bandwidth at 1.4x. This disparity necessitates more machines, raising DL training costs, particularly for LLM training, where the computational power required surpasses that of traditional HPC applications.

B. Challenges and Solutions in Models Training

In Deep Learning training, a single task demands hundreds of GPUs and consumes substantial storage and network resources. This massive scale introduces system-level challenges:

1) Efficiency: Firstly, achieving efficient training at this magnitude is crucial. Model FLOPs Utilization (MFU), which assesses the ratio of observed throughput to theoretical maximum throughput (assuming 100% peak FLOPS), serves as the standard metric for evaluating training efficiency. Training LLMs involves dividing models among GPUs that communicate extensively for progress. Besides communication, factors like operation optimization, data pre-processing, and GPU memory consumption significantly influence MFU. Multiple parallel strategies are employed to enhance efficiency:

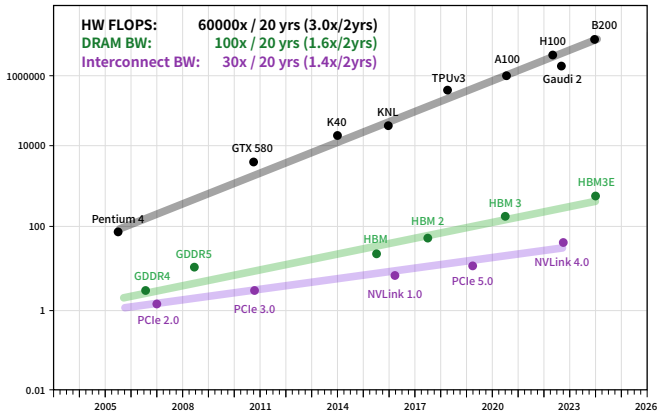


Figure 2: Scaling of Peak Hardware FLOPS, and Memory/Interconnect Bandwidth.

- **Data Parallelism (DP):** Models and optimizer states are replicated across multiple devices with data evenly distributed to all. For LLMs training, the Zero Redundancy Optimizer (ZeRO) [19] further enhances this method by sharding these states on each data parallel process and using allgather and reduce-scatter for parameter fetching and gradient calculation.
- **Pipeline Parallelism (PP):** Each device holds a portion of the model layers with each training batch divided into micro-batches for pipeline execution. Efficient scheduling strategies like GPipe [11], PipeDream 1F1B [12], and Zero Bubble Pipeline Parallelism (ZBPP) [33], are required to minimize "pipeline bubbles".
- **Tensor Parallelism (TP):** This involves placing a model layer on multiple GPUs that perform computations in parallel [13] [14]. It includes row-wise and column-wise parallelism, necessitating allgather and all2all for input splitting and output merging.
- **Expert Parallelism (EP)**: MoE Models' different expert models are distributed on different GPUs during MoE training [15]–[17]. The gate model selects tokens for allocation during input, with corresponding tokens sent to experts model via all2all communication.
- **Fully Sharded Data Parallel (FSDP)** is an implementation based on the ZeRO Stage 3 algorithm [19]. FSDP partitions the model's parameters, optimizer states, and gradients, distributing them across different GPUs, with each GPU retaining only $1/n$ of the total. During forward propagation, FSDP performs an allgather operation to assemble the complete parameters, which are then released after the forward pass is completed. Similarly, during backward propagation, FSDP conducts an allgather operation to obtain the complete parameters, followed by backward computation to calculate gradients. It then performs a reduce-scatter operation to synchronize gradients across all GPUs, resulting in each GPU holding $1/n$ of the reduced gradients. Finally, FSDP updates the $1/n$ parameters using each GPU's $1/n$ gradients and optimizer states. FSDP reduces GPU memory usage by maintaining only $1/n$ of the parameters, gradients, and optimizer states on each GPU, enabling training of larger-scale models.

There are additional strategies and algorithms to accelerate training or reduce memory usage, such as **Activation Recomputation** [34], [35], as well as enhanced communication and computation overlap during parallelism [36], among others.

2) Stability: The second challenge is achieving high-stability training at scale, i.e., maintaining efficient training throughout the process. Stability is vital from a production standpoint as training a big model with a trillion tokens may span several weeks. In DL training, stragglers and hardware failures are common occurrences rather than outliers. Stragglers can decelerate tasks involving hundreds of GPUs, emphasizing the importance of stability and task recovery time.

C. HPC and AI Clusters of This Era

1) HPC Inadequacies for AI Training: Traditional supercomputers such as TianHe-2A [37], Stampede 2 [38], and Sunway TaihuLight [39] primarily focus on double precision calculations and do not support the FP16 precision, rendering them unsuitable for DL training. Fugaku [40], despite its high performance, does not support tensor GEMM acceleration, a key component for DL workloads. Although these supercomputers may not be well-suited for DL training, their robust high-performance networks and extensive experience in large-scale cluster construction offer valuable insights and lessons for subsequent researchers.

2) GPU based HPC: Supercomputers like Frontier [41], Aurora [42], Summit [43] and Perlmutter [44] utilize high-performance GPUs to tackle large-scale computations. It's worth mentioning that Perlmutter utilizes an all-flash storage system, achieving a peak bandwidth of 5TB/s. Indeed, conducting DL training on these GPU-based HPCs yields significant performance.

3) GPU Clusters of Large Companies: Meta, formerly Facebook, has developed its AI-HPC using a software-hardware co-design approach, with one system utilizing IB and another employing RoCE [45], [46]. ByteDance initially implemented a DL cluster with a mix of CPU and PCIe GPU [47]. However, with the advent of the LLMs era, they adopted an architecture similar to DGX, building a cluster with over 10,000 GPUs [48]. Alibaba has developed its own HPN network [49] for LLMs training using NVIDIA H800 GPUs. NVIDIA also has its own AI-HPC Eos [50], which will feature 576 DGX H100 systems totaling 4,608 H100 GPUs. While this will provide a considerable boost in computational power for AI tasks, the high cost of DGX systems raises questions about economic viability.

4) AI DSA Clusters: Custom-designed AI DSA (Domain Specific Architecture) accelerators like Google's TPU [51] , utilize highly advanced optical switch reconfigurable networks. Alternatives to traditional GPU setups, like Intel Habana Gaudi [52], are also available. Teslahas introduced the Dojo [53], [54] supercomputer , which uses System on

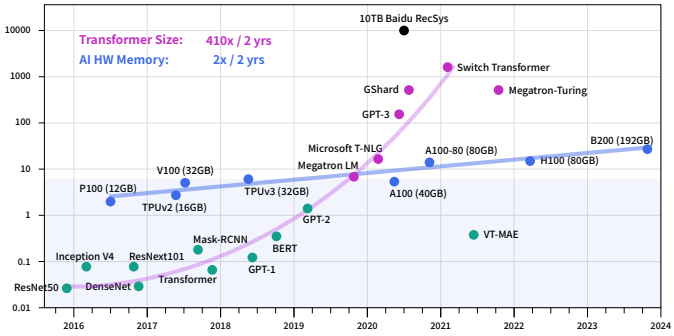


Figure 3: Size of Model Parameter and Accelerator Memory

Wafer technology to build an entire silicon wafer as a single chip. Huawei has designed the Ascend AI DSA chip [55], [56], which remains competitive with NVIDIA, as noted by NVIDIA CEO Jensen Huang. These accelerators are tailored for efficient execution of AI workloads, offering specialized features to optimize model training and inference. However, their software ecosystems, while progressing, still require further development to match the maturity of NVIDIA's offerings.

5) Cloud Service Providers: Cloud service providers, such as Azure, offer flexible and scalable resources for AI training. Despite their convenience and easy accessibility, the costs can accumulate significantly over time. For long-term projects spanning around two years, these costs could amount to purchasing an entire dedicated cluster. Therefore, this option may not be the most economical choice for extensive AI computations.

D. Challenges in AI Infrastructure

As models continue to grow larger, DL training requires thousands of GPUs. Additionally, researchers often need to train multiple models simultaneously. Therefore, a cluster with at least tens of thousands of GPUs can meet the needs of AI practitioners. In addition to increasing the scale of the cluster nodes and adding more GPUs, there's also a need to find ways to save on the overall system construction costs. These costs include but are not limited to power support, cooling, networking, storage, fault handling, disaster recovery, etc. Building a cost-effective AI-HPC system is a significant challenge. The question of how to construct a high-performance, efficient, economical, and environmentally friendly HPC to meet AI training requirements has become a hot topic. Some works, such as [57] analyzes the construction of HPC, discussed the interconnection of heterogeneous clusters, cooling systems. AI applications such as Peng Cheng Cloud Brain II [58] discussed their strategies for building and improving AI computing power and cluster communication efficiency, which helped them achieve first place in IO500 and AIPerf rankings.

Drawing from our extensive experience in Deep Learning spanning over the past decade, we have conducted considerable exploration in terms of cost-effectiveness. This work primarily discusses our practices for achieving cost-effectiveness and high-performance across different models and stages.

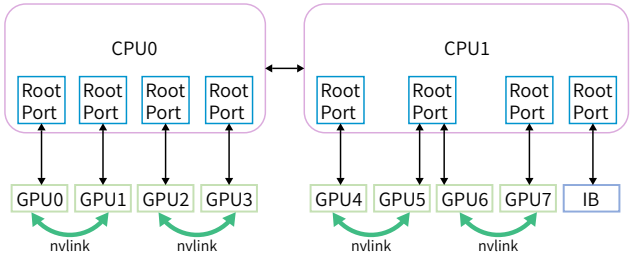


Figure 4: In-node Architecture: 8 PCIe GPUs and 1 InfiniBand (IB) NIC are directly connected to the CPU. Note that GPU5/6 share the same PCIe root port, while IB occupies one independently.

Table I: Our Arch and DGX-A100 Server Hardware Details

	Our PCIe Arch	DGX-A100
CPU	2 * AMD 32 Cores EPYC Rome/Milan CPU	2 * AMD 64 Cores EPYC 7742 CPU
Memory	512GB 16-Channels DDR4-3200Mhz	2048GB 16-Channels DDR4-3200Mhz
GPU	8 * PCIe-A100-40GB	8 * SXM-A100-40GB
NICs	1 * Mellanox InfiniBand cx6 200Gbps NIC	9 * Mellanox InfiniBand cx6 200Gbps NIC
NVLINK	600 GB/s between each pair of GPUs	600 GB/s interconnect among all 8 GPUs

III. Fire-Flyer 2: Our Approach For Deep Learning and Early LLM Training

As mentioned in the Background Section, LLMs generally require significant memory resources. In contrast, many other models necessitate considerably less memory, as illustrated in Figure 3. Popular models like ResNet [22], Mask-RCNN [59], BERT [60], MAE [61], among others, all have a parameter volume less than 1B, signifying relatively low memory requirements. Therefore, when designing a cluster primarily for deep learning model training, and with insights gleaned from our Fire-Flyer 1 experiments, we deemed it prudent to incorporate PCIe A100 GPUs, which proved to be sufficient during its construction in 2021.

A. Fire-Flyer 2: PCIe A100 GPU Architecture

In our training workloads, the bandwidth requirements for both storage IOs and computation communication across 8 NVIDIA PCIe A100 GPUs can be met by a single 200Gbps NVIDIA Mellanox ConnectX-6 (CX6) InfiniBand (IB) NIC. We employed the following computation node architecture , as shown in Figure 4:

- 8 NVIDIA A100 PCIe GPUs and 1 Mellanox CX6 200Gbps IB NIC: directly connect to the CPU, without using a PCIe switch
- IB NIC occupies a separate PCIe root complex, thus avoiding performance interference with the GPU.
- Reserved the possibility of NVLink Bridge addition in design: As expected, when the LLM era arrived, we indeed added an NVLink Bridge between PCIe cards.

Table I shows our arch details and compared with NVIDIA standard DGX-A100 server.

B. Network Topology: Two-Layer Fat-Tree with Storage and Computation Integrated

We selected the **Fat-Tree** [9] topology as our primary network architecture due to its exceptionally high bisection bandwidth, making it the preferred choice for AI-HPC and high-throughput storage environments. Although the Dragonfly topology [62], [63] also offers comparable cost-effectiveness and performance, its lack of sufficient bisection bandwidth makes it unsuitable for our **integrated storage and computation network design**. At the time of implementation, various RoCE (RDMA over Converged Ethernet) [64] technologies were not as mature as they are today, so we opted for InfiniBand (IB) as our network solution. Mellanox QM8700 InfiniBand Switch, offering 40 ports at 200 Gbps, was utilized. Our cluster, consisting of 10,000 A100 GPUs, includes approximately 1,250 GPU compute nodes and nearly 200 storage servers, although a Two-Layer Fat-Tree can accommodate up to 800 nodes (configured with 20 spine switches and 40 leaf switches).

To reduce costs, , we opted for a two-zone network configuration instead of a three-layer Fat-Tree solution, as shown in Figure 5. Each zone consists of an 800-port Fat-Tree connected to approximately 600 GPU compute nodes. Each storage server equipped with two IB NICs, respectively connected to different zones, hence all GPU compute nodes could share a set of storage services. Additionally, the two zones are interconnected with a limited number of links. Our HAI Platform scheduling strategy ensured that cross-zone computing tasks were limited to one at most. Whether using NCCL [10] or our in-house developed communication library HFReduce, it can be run across zones by using a double binary tree algorithm [65]. Our scheduler ensures that in this topology, only one pair of nodes communicates across zones. Consequently, even tasks requiring all nodes can efficiently run on the entire Fire-Flyer 2 AI-HPC.

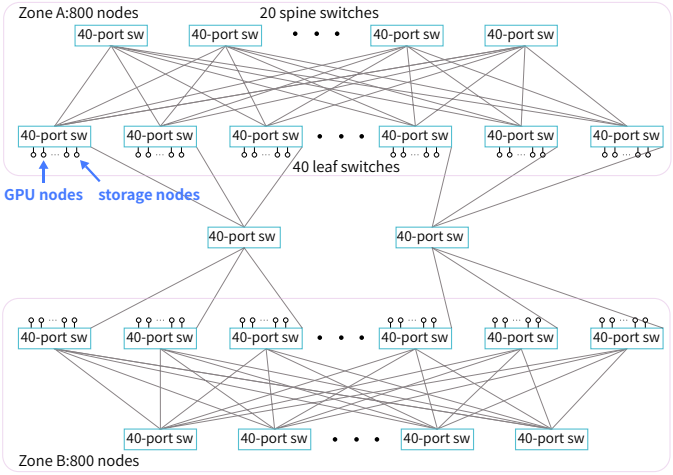


Figure 5: Network Topology: Two complete Two-Layer Fat-Tree connected together.

Table II: A100 PCIe Compared to DGX-A100.

	Our Arch	DGX Arch
TF32 GEMM (TFLOPS/GPU)	107	131
FP16 GEMM (TFLOPS/GPU)	220	263
Relative Performance	83%	100%
Node Relative Price	60%	100%
Cost–Performance Ratio	1.38	1
Power Consumption (Watts)	2500	4200

Table III: Relative Cost Comparison.

	Our Arch	PCIe Arch with Three Layer Fat-Tree	DGX Arch
Number of Switches	122	200	1320
Network Price	350	600	4000
Server Price	11250	11250	19000
Total Price	11600	11850	23000

C. Cost Performance of Our Architecture

Compared to the NVIDIA DGX-A100 [8] architecture, our approach using PCIe A100 achieves approximately 83% of the performance in TF32 and FP16 General Matrix Multiply (GEMM) benchmarks. However, it offers substantial reductions in both costs and energy usage, achieving 60% of the GPU cost and energy consumption, as detailed in Table II.

Contrasting with the DGX-A100 cluster, which necessitates a Three-Layer Fat-Tree encompassing 10,000 access points and involving 320 core switches, 500 spine switches and 500 leaf switches, amounting to 1,320 switches in total (as shown in Table III), our architecture only requires 122 switches. This arrangement is significantly more cost-efficient. Even when compared to a similarly sized three-layer Fat-Tree network with 1,600 access points, which includes 40 core switches and 160 spine and leaf switches (totaling 200 switches), our design facilitates a saving of 40% in networking costs.

Furthermore, by utilizing an 800-Ports Frame Switch, we have further reduced the cost of optical modules and cables. While there is a performance gap due to the inherent differences between PCIe card specifications and SXM, we generally achieved 80% of the DGX-A100 performance at merely 60% of the cost. Additionally, we managed to trim energy consumption by 40%, thereby reducing CO_2 emissions. In terms of cost-performance, we regard this approach as both effective and successful.

IV. HFReduce: Hardware Software Co-Design in Network

In large-scale deep learning training, allreduce is essential for aggregating gradients across GPUs. To optimize communication among PCIe GPUs in our architecture, we developed HFReduce, a library specifically designed for efficient allreduce operations. The core strategy of HFReduce, illustrated in Figure 6, involves performing intra-node reduction first, followed by inter-node allreduce of the reduced data from the 8

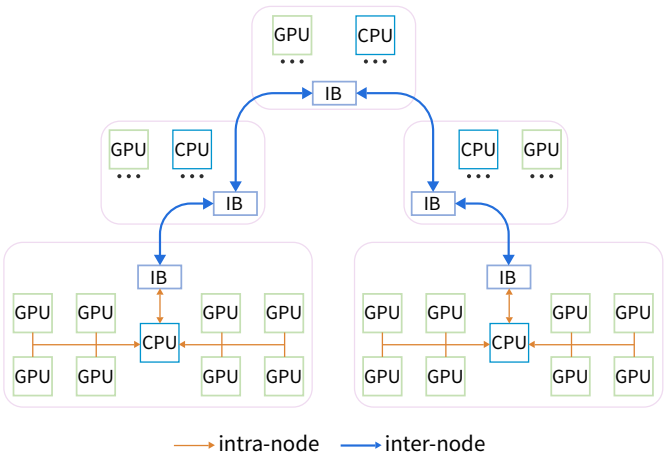


Figure 6: HFReduce Schematic: 1) do intra-node reduce, 2) do inter-node allreduce by CPU, 3) finally transfer reduced data to GPU.

GPUs within each node. This inter-node allreduce leverages a Double Binary Tree Algorithm [65], akin to NCCL, and is pipelined by dividing data into chunks for transfer via Remote Direct Memory Access (RDMA), ensuring high performance. HFReduce is versatile and can be applied to any scenario requiring allreduce, as well as general reduce and broadcast operations.

A. HFReduce Algorithm Steps

Intra-node reduction, as shown in the Algorithm 1:

1) When the gradients data on the GPUs require allreduce, HFReduce asynchronously transfers these data to the CPU memory. This Device-To-Host (D2H) Transfer can utilize GDRCopy [66] for small data and MemCpyAsync for larger data.
2) Upon the arrival of the gradients in memory, perform reduction add operation using CPU vector instructions.

Inter-node reduction, as shown in the Algorithm 2:

1) Use the Double Binary Tree Algorithm [65] for inter-node allreduce, facilitating transfers between nodes using RDMA verbs implementation.
2) Finally, the CPU returns reduced gradients to the GPU via PCIe (Host-To-Device Phase).

The final Host-To-Device (H2D) Transfer can be optimized by utilizing GDRCopy to write data to four GPUs within the same NUMA node, effectively reducing reads from host memory by threefold compared to MemCpyAsync. This efficiency is achieved because GDRCopy can read data from host memory and temporarily cache it in the CPU caches, allowing data to be written to the four GPUs without additional reads from host memory.

B. Advantages of HFReduce over NCCL

*1) **Reduced PCIe Bandwidth Consumption**:* Let n be the total number of GPUs involved in the communication. In NCCL's ring topology, each unit of data needs to go through $2n-1$ transmissions, each consuming one unit of inbound bandwidth of one GPU and one unit of outbound bandwidth of another GPU. This means for a single unit of data, it consumes $\frac{2n-1}{n}$ unit of PCIe bidirectional bandwidth. In contrast, for each unit of data, HFReduce only requires one D2H and one H2D data transfer, only one unit of PCIe bidirectional bandwidth is consumed. In our machine architecture, the performance of NCCL is mainly limited by PCIe bandwidth. Therefore, HFReduce can achieve better performance than NCCL.

*2) **No GPU Kernel Overhead**:* HFReduce utilizes the GPU's Copy Engine (CE) for PCIe asynchronous transfers. In contrast, NCCL's allreduce operation requires GPU kernel execution, which can affect other computational kernels on the GPU. HFReduce achieves complete asynchrony with no overhead.

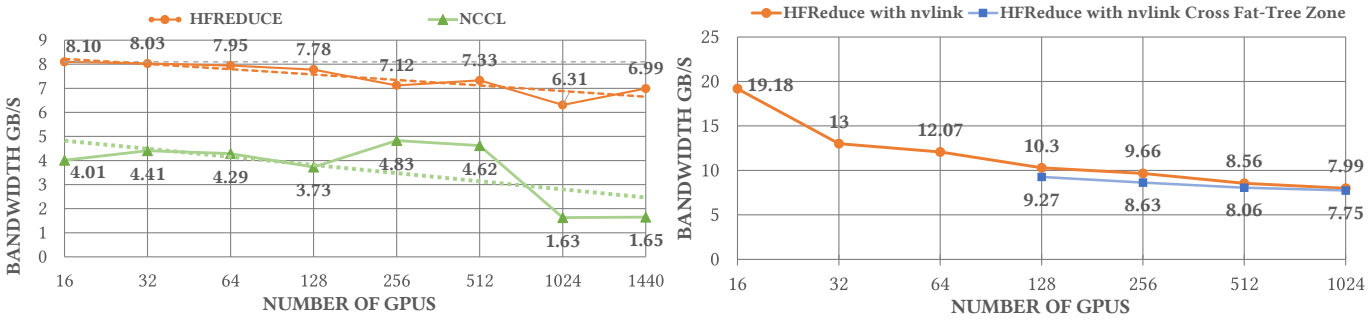
As demonstrated in Figure 7a, HFReduce can reach a inter-node bandwidths of 6.3-8.1GB/s when performing allreduce with a data size of 186 MiB on the Fire-Flyer 2 AI-HPC, while NCCL's inter-node bandwidth is only 1.6-4.8GB/s.

Algorithm 1: Intra Node Reduce.

```
Data: Dg: data need to allreduce
Result: Dc: data reduced in this node
Split Dg by Chunk_Size
for Dg-i in Splited-Dg do
    // Transfer GPU Memory Data to CPU memory
    Dc_i = MemCopyAsync Dg_i to CPU Mmeory
end
for i in Splited_Count do
    while every GPU's Dg_i → Dc_i finished do
        // Wait for chunk-i transfer finished in this node
        for j in GPU_Count do
            // do intra-node reduce
            Dc_i += GPU-j's Dc_i
        end
        // do inter-node reduce
        Do_Internode_reduce(Dc_i)
    end
end
```

C. Performance Improvements: HFReduce with NVLink

By installing the NVLink Bridge for PCIe A100 GPUs, efficient communication is enabled between paired GPUs via the 600 GB/s NVLink. To alleviate the memory bound issue of the original HFReduce, we implemented another allreduce pattern, termed **HFReduce with NVLink**. The core concept involves initially performing a reduction operation among GPUs interconnected by NVLink before passing the gradient to the CPU. Subsequently, when the CPU returns the result, it splits the result data and returns them to the paired GPUs connected by NVLink respectively, then performs allgather via NVLink. As illustrated in Figure 7b, HFReduce with NVLink achieves inter-node bandwidths exceeding 10 GB/s.



(a) HFRudce and NCCL Allreduce Speed.

(b) HFReduce with NVLink (Cross Fat-Tree Zone).

Figure 7: Strong Scalability: (a) Network Bandwidth when HFReduce and NCCL do allreduce test with 186MiB data, scale from 16 to 1440 GPUs. (b) HFReduce with NVLink, and Cross Fat-Tree Zone. Note that tasks utilizing fewer than 128 GPUs do not require cross-zone nodes and are restricted by platform defaults.

Algorithm 2: Inter Node Reduce.

```
Data: DL:local node reduced data by Algorithm 1
Data: DR: received other node reduced data
Result: Dg: reduced data transfer to GPU
// Pass 1: reduce data,individual thread
for i in Chunk_Size do
    receive data DR_i from prev node
    if DL_i ready then
        DL_i +=DR_i // reduce data
    end
    if Thread is root of Tree then
        send DL_i to prev node // Dg_i finished, go parse 2
    else
        send DL_i to next node
    end
end
//
// Pass 2: gather reduced data,individual thread
receive data DR_i from next node
for j in GPU_Count do
    Dg_i = MemCopyAsync DR_i to GPU-j // Dg_i is allreduced
end
send DL_i to prev node
```

D. Deep Analysis of HFReduce

1) Key Technical Strategies in Implementation:

- Using GDRCopy accelerate small data transfer in D2H, and educing reads from host memory by three times compared to MemCpyAsyn.
- Intra-Node Reduction: CPU utilizes SIMD instructions and supports FP32 / FP16 / BF16 / FP8 datatypes.
- NUMA Awareness: D2H destination memory is interleaved across two NUMA nodes for maximum bandwidth. Memory for CPU-added results and network-received data is bound to the IB-Nic's NUMA node to minimize latency.
- Inter-Node Reduce:Implements a Double Binary Tree allreduce algorithm [65] via ibverbs RDMA Write, avoiding additional overhead.

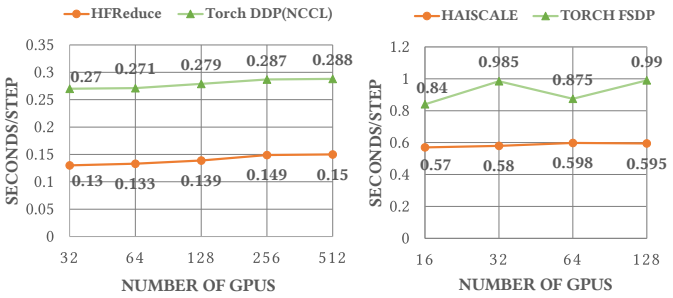
2) HFReduce Overcomes Limitations of EPYC Rome CPU: We consulted AMD and NVIDIA engineers to identify the root cause of NCCL's suboptimal performance on PCIe architecture, particularly with EPYC Rome CPU servers. It was determined that the Rome CPUs do not support the chained write feature, which can significantly accelerate PCIe peer-to-peer (P2P) transfers between GPUs and IB NICs. Our tests indicate that the maximum bandwidth between the GPU and IB NIC on Rome CPUs is approximately 9 GiB/s, making the observed 4GB/s all-reduce bandwidth for NCCL understandable. HFReduce circumvents this limitation by utilizing the CPU for reduction and transferring data through IB and host memory.

*3) **Bottlenecks of HFReduce**:* When considering the total memory operations on a single node during HFReduce, several factors contribute to its performance limitations:

1) D2H Phase requires 8 write operations.
2) Intra-node Reduce Add Phase involves 8 read operations and 1 write operation.
3) Inter-node Allreduce Phase: IB send demands 2 read operations, while IB receive requires 2 write operations, along with 1 read operation for reduce add.
4) H2D Phase Utilizing GDRCopy can reduce this to only 2 read operations, whereas MemCopy necessitates 8 read operations.

In total, the memory operations amount to 24 times the original data size in the GPU. A host equipped with 16 channels of DDR4-3200MHz memory can achieve a practical memory access speed of 320GB/s. Consequently, the theoretical maximum speed of HFReduce is approximately 13.3GB/s, but when considering the allreduce algorithm bandwidth and network bandwidth, this value realistically approximates 12GB/s. However, our tests only achieved slightly over 8GB/s.

The root cause of this discrepancy is another limitation of the EPYC CPUs. As previously mentioned, our GPU5 and



(a) HFReduce v.s. Torch DDP. (b) HaiScale v.s. Torch FSDP.

Figure 8: Weak Scalability: (a) Training VGG16, HFReduce compared to PyTorch DDP's NCCL backend (b) Training GPT2-Medium HaiScale compared to Torch, both using FSDP.

GPU6 are directly connected to the CPU via the same PCIe Root Complex Port (also known as the PCIe Host Bridge). In AMD EPYC Rome and Milan CPUs, the maximum bandwidth from the Root Complex Port to the CPU's internal bus is about 37.5GB/s. Although a PCIe 4.0 x16 port can achieve over 27GB/s from GPU to CPU, when two GPUs transfer data concurrently, the bandwidth is limited to around 37GB/s. Furthermore, if bidirectional data transfer occurs simultaneously, this bandwidth decreases even further. As a result, HFReduce does not reach its theoretical speed.

Employing NVLink with HFReduce offers a functional method to alleviate these bottlenecks. However, it is worth noting that the next-generation CPUs, such as the EPYC Genoa, still face issues with PCIe Host Bridge bandwidth, which cannot support two full-speed PCIe ports simultaneously. We hope AMD will address this issue in future iterations.

V. HaiScale: Special Optimization for Deep Leaning Models Training

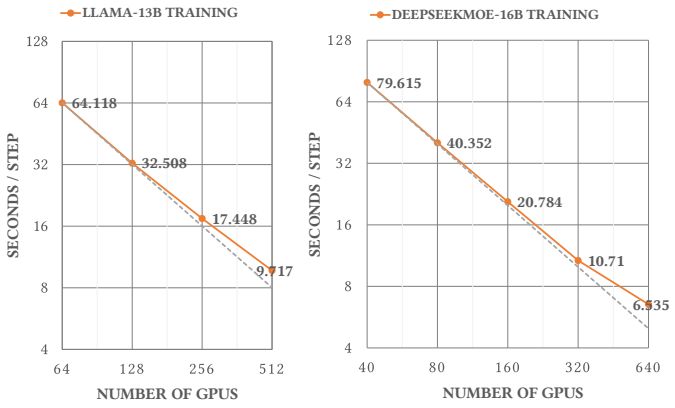
A. HaiScale DDP Overlap AllReduce in Training

HaiScale Distributed Data Parallel (DDP) is a training tool that utilizes HFReduce as its communication backend, in contrast to PyTorch's DDP [67] which employs NCCL as its backend. During the backpropagation phase, HaiScale DDP performs an asynchronous allreduce operation on the computed gradients, allowing this communication to overlap with the computation involved in backpropagation.

As previously mentioned, HFReduce does not depend on GPU Streaming Multiprocessors (SM) for reduction computation, enabling completely asynchronous allreduce without impacting performance. As shown in Figure 8a, training VGG16 model [68] with HFReduce takes only half the time compared to using Torch DDP's NCCL backend, achieving nearly 88% parallel scalability when scale from 32 GPUs to 512.

B. LLMs Training Optimization

Our HaiScale framework various parallelism strategies for training large language models (LLMs), similar to Megagron [69] and DeepSpeed [70]. We have made specific engineering optimizations for our PCIe architecture across Data Parallelism (DP), Pipeline Parallelism (PP) [11] [12], Tensor Parallelism (TP) [14], Expert Parallelism (EP) [15]–[17].



(a) Train LLaMa-13B (b) Train DeepSeekMoE-16B

Figure 9: Strong Scalability: (a) Train LLaMa-13B with a config of sequence length 2048, batch size 4096, pipeline parallel 4. (b)Train DeepSeekMoE-16B with a config of sequence length 4096, batch size 4608, pipeline parallel 10.

1) NVLink Bridge Enables Tensor Parallel between PCIe GPUs: With the advent of LLMs, we integrated the NVLink Bridge into our system. This addition established a bandwidth of 600GB/s between each pair of GPUs, enabling more efficient when performing Tensor Parallelism.

2) Pipeline Parallelism Optimization in PCIe Architecture: In our architecture, there is only one IB NIC for 8 GPUs on a single node, which can lead to network bandwidth contention during Pipeline Parallelism (PP). We solve this by configuring Data Parallelism (DP) rank, making the 8 GPUs on the same node belong to different DP ranks which staggers the timing of PP for each DP rank. As Figure 9a shown, when scaling from 64 GPUs to 512 GPUs, the training step time for LLaMa-13B [71] reduces significantly from 64.118 seconds to 9.717 seconds, achieving a parallel efficiency of **91%** at 256 GPUs.

We also benchmarked the training performance of our DeepSeekMoE-16B model [72] on Fire-Flyer 2 AI-HPC. As shown in Figure 9b, scaling from 40 GPUs to 640 GPUs reduced the time per training step from 79.615 seconds to 6.535 seconds, achieving a parallel efficiency of 76.14%. Notably, with 320 GPUs, the step time was 10.71 seconds, resulting in a parallel efficiency of **92.92%**, demonstrating excellent scalability.

3) Fully Sharded Data Parallel (FSDP): Both HaiScale's FSDP and PyTorch's FSDP [18] are implementations based on the ZeRO Stage-3 algorithm [19]. The details of this implementation are already discussed in Section II-B1.

HaiScale's FSDP offers better engineering implementation, optimizing memory management to reduce fragmentation specific to model adjustments. And we overlap allgather and reduce-scatter communication with forward and backward computation, split the optimization step during backward propagation for enhanced overlap. As shown in Figure 8b, training GPT2-medium [73], we achieve 95% parallel scalability when scaling from 16 to 128 GPUs. ompared to PyTorch's FSDP, HaiScale's FSDP reduces training time by nearly half.

C. Summary

Our AI-HPC design meets DL requirements, and with the addition of the NVLink Bridge, it meets the training needs of early-stage LLMs, reaching the utilization upper limit of PCIe GPUs. However, due to the inherent gap between PCIe card specifications and SXM, there is a certain performance discrepancy. Considering overall performance, basic setup cost, and energy consumption, we achieved 80% performance at half the cost. We believe Fire-Flyer 2 AI-HPC is a successful practice in terms of cost-effectiveness.

VI. Advanced Cost-Effective and Co-Design Optimizations

A. Ensuring Minimal Congestion in Our Computation-Storage Integrated Network

As previously stated, our cost-effective network integrated computation communication and storage traffics together. To achieve maximum bandwidth, it is essential to isolate interference between different types of traffic and control network congestion. In practice, we implemented the following measures:

1) Divergence of Different Traffics: In typical training tasks, there are four different types of traffic: HFReduce communication, NCCL communication, 3FS storage traffic, and other traffic. By using InfiniBand's Service Level (SL) technology [74] [75], we assign different value of SL when establishing connections between nodes and map SL to IB physical queues Virtual Lanes (VLs) [74] [75]. The use of Virtual Lanes ensures that flows in distinct lanes do not interfere with each other. Ultimately, we configured their proportions to implement traffic isolation, thereby preventing network congestion caused by Head-of-line (HOL) blocking [76] and different traffic collisions.

2) Topology Adjustment and Route Optimization: In high-throughput storage scenarios, there naturally exist many incast communication patterns, leading to certain congestion in the network. Under such circumstances, we observed that enabling adaptive routing would lead to more severe congestion spread in the network. Therefore, we opted for a static routing strategy. Based on the static routing scheme, to evenly disperse storage traffic into leaf $\rightarrow$ spine links, we distribute various nodes (storage, computation, management nodes) evenly disperse storage traffic into leaf $\rightarrow$ spine links.

3) NCCL Optimization: We adjusted the NCCL topology to route through the IB NIC and GPUs within the same NUMA node. This adjustment reduced PCIe congestion caused by CPU chiplet interconnects. Additionally, by using PCIe Relaxed Ordering [77], we further reduced congestion and increased bandwidth.

4) Network Tuning in 3FS: 3FS implements a request-to-send control mechanism to mitigate the congestion. Details are discussed in the next subsection, Key Techinical Points of 3FS.

B. High-Throughput Distributed File System: 3FS

1) Overview: 3FS is our in-house developed high performance distributed file system, akin to WekaFS [78], DAOS [79], [80], and BeeGFS [81]. However, the design and implementation of 3FS specifically focus on fully utilizing the high IOPS and throughput of NVMe SSDs and the RDMA network.

Table IV: Storage Node Hardware Details

CPU	1 * AMD 64 Cores EPYC 7742 CPU
Memory	512GB 8-Channels DDR4-3200Mhz
NICs	2 * Mellanox InfiniBand CX6 200Gbps NIC
Data SSDs	16 * 15.36TB PCIe 4.0x4

2) 3FS Storage Node Hardware: In Fire-Flyer 2 AI-HPC, we deployed 180 storage nodes, as shown in Table IV, each node contains 16 PCIe 4.0 NVMe SSDs and 2 Mellanox CX6 200Gbps InfiniBand HCAs. With totally 360 * 200Gbps outbound InfiniBand HCAs, the system can total provide 9TB/s outbound bandwidh, and we actually achieved total **read throughput of 8TB/s**. The total 2880 NVMe SSDs provide over 20PiB storage space with an mirror data redundancy.

3) Key Techinical Points of 3FS: The 3FS system comprises four roles: cluster manager, meta service, storage service and client. Meta and storage services send heartbeats to cluster manager. All services and clients poll cluster configuration and service status from the manager. Multiple cluster managers are present, with one elected as the primary.

File system meta data are stored in tables of a distributed key-value storage system. Each file or directory has a unique inode ID. The File inode/directory ID and meta data, such as file size and location information of the file content data, are stored as key-value pairs in the inode table. A separate directory entry table stores key-value pairs of $(parent\_dir\_inode\_id, entry\_name)$: $(entry\_inode\_id, ...)$ to support iterating entries in a directory and resolving file/directory paths. All states of meta services are persisted on the distributed key-value storage system. Several meta services run concurrently to handle meta requests from clients.

The storage service has an implementation of Chain Replication with Apportioned Queries (CRAQ) [82] to provide strong consistency. CRAQ's write-all-read-any approach helps to unleash the throughput and IOPS of all SSDs. File content are split into chunks, which are replicated over a chain of *storage targets*. A *chain table* contains an ordered set of chains. The meta service selects an offset in the chain table and a stripe size *k* for each file. The file chunks are assigned to the next *k* chains starting at the offset. To distribute read/write traffic evenly to all SSDs, each SSD serves multiple storage targets from different chains. The storage service runs on every storage node and manages a few storage targets.

The storage network has a Fat-Tree topology that provides full bisection bandwidth. By design, each 3FS client can access every storage service. At peak load, incast congestion is

observed on the client side. **To mitigate this congestion, a request-to-send control mechanism is implemented** in storage service and client [83]. After receiving a read request from a client, the service reads data from SSD and asks the client's permission to transfer the data. The client limits the number of concurrent senders. When a storage service is granted the permission to transfer, it sends the data with a RDMA WRITE followed by a RDMA SEND to notify the client. The request-to-send control increases end-to-end IO latency but it's required to achieve sustainable high throughput.

4) 3FS-KV: 3FS-KV is a shared-storage distributed data processing system built on top of 3FS, currently supporting three models: key-value, message queue, and object storage. It supports read-write separation and on-demand startup, allowing it to fully leverage the extremely high I/O throughput provided by 3FS. 3FS-KV supports DeepSeek's KV Context Caching on Disk technology [84], which reduces the cost of LLM serving by an order of magnitude.

C. HAI Platform: a Time-Sharing Scheduling Platform

The principle of time-sharing scheduling is applied to cluster resource management. Users submit tasks, such as running Python / bash code, starting development containers, etc., and the platform interrupts and loads tasks according to current resource requirements, cluster busyness, etc. Task code needs to follow the platform coding rules to ensure that it can be continued from breakpoints, with the specific process as follows:

- Accepting the interruption signal from the cluster;
- Saving checkpoints (model parameters, optimizer parameters, etc.);
- Notifying the cluster of interruptions;
- Recovering from the checkpoint and continuing to run.

The cluster deploying HAI Platform does not pool GPU resources, but classifies and marks them based on computing nodes as basic units, according to resource types, network areas, etc. The HAI Platform encourages users to fully utilize multiple GPUs simultaneously for parallel training, facilitating 99% utilization.

VII. Stability and Robustness

A. Checkpoint Manager

Training LLMs can span several months, during which unavoidable hardware failures may cause training interruptions. To minimize recovery time and support the HAI Platform's interrupt and recovery operations, we developed a checkpoint manager. Additionally, the substantial size of LLM checkpoints necessitated an efficient method for saving and loading them, leveraging the high throughput of 3FS. The checkpoint manager includes the following components:

- Parameters and optimization states are divided into chunks and written to 3FS using the 3FS batch write API, which is significantly faster than normal writes, achieving over 10 GiB/s per node. This enables saving to be completed in just a few seconds.
- Parameters and optimization states are asynchronously transferred from GPU to CPU host memory, with checkpoint saving performed periodically (typically every 5 minutes).
- During the saving process, each tensor is recorded with its index and the offset within the checkpoint., which makes the location of tensors more convenient during the loading process. With the 3FS batch read API, a loading process can be completed in just a few seconds.

Thanks to the high write throughput of 3FS, periodic saving operations can be completed asynchronously in a matter of seconds, without impacting the training process. In the event of hardware failures that interrupt training, only the last 5 minutes of progress are lost. For a cluster with thousands of nodes, this overhead from disaster recovery is minimal.

B. Validator

The best way to enhance device stability is to identify issues before they occur. Therefore, we have developed a set of validator tools to verify whether the hardware is functioning correctly. The platform's automatic operation and maintenance system runs the validator program weekly on nodes to verify their proper functionality. It removes the faulty nodes from the scheduling platform, ensuring that all scheduled nodes are operational. Diagnosing tools like hostping [85] also integrated in our platform, but to find root cause of Hardware Failures is still hard work for operation teams. The validator mainly consists of the following parts:

- Checking hardware frequency, link speed, and link status.
- Testing CPU stress and memory bandwidth.
- GPU Memory test: This involves checking each byte of GPU memory to ensure no data corruption has occurred.
- Running GEMM with full GPU memory occupancy, which can simultaneously check whether there are any operational logic faults in the GPU chip.
- Intra-node allreduce test: checking NVLink bandwidth through upper-level applications.
- Storage bandwidth stress test to make sure storage is functioning normally.

C. Hardware Failures Characterization in Fire-Flyer 2 AI-HPC

In supercomputers and data centers, hardware failures and chip errors can lead to floating-point overflow, non-convergence, or slow convergence during model training [86]. This paper [87] even directly points out that there is a substantial amount of Silent Data Corruption in data center processors, ultimately leading to a variety of complex issues that are difficult to replicate and locate. Indeed, in our practice, we have encountered computational errors and GPU memory errors not detected by Error Correction Code (ECC), which led to models' gradnorm spikes, loss explosions and even non-convergence. How to tackle these hardware failures, promptly identify and categorize them, is a key issue to improve the online rate and overall utilization of cluster nodes.

Table V: Type of GPU Xid Errors and Its Causes

Xid Errors	Analysis
Software Causes: Xid_13/31 Xid_43/45	Triggered by application programs, software-related Xid messages may indicate anomalies in GPU memory affecting code and data segments. However, it's crucial to consider other information for a comprehensive hardware functionality assessment.
NVLink Error: Xid 74	Xid74 indicates errors in NVLink. For PCIe A100, it's mainly occurred on the NVLink Bridge between two GPUs. Its occurrence rate is several orders of magnitude higher than other hardware faults. Apart from stress testing to exclude those that are constantly repeating errors, there isn't a good way to avoid the occurrence of Xid74 issues.
Memory ECC Error: Xid_63/64 Xid_94/95	Triggered when the GPU handles memory ECC errors on the GPU. With the introduction of row remapping technology in A100, most instances can be resolved by simply resetting the GPU to retain optimal performance.
Uncorrectable GPU Failures: Xid_44/48 Xid_61/62/69/79	Thease failures mean an uncorrectable error occurs on the GPU, which is also reported back to the user application. A GPU reset or node reboot is needed to clear this error.
Other Failures: Xid 119	Xid119 means GPU GSP module failed. These failures need to do fieldiag test, and most need to RMA.

*1) **GPU Xid Error**:* An Xid error [88] is a general GPU fault message that originates from the NVIDIA driver, logged into the kernel or event log of the operating system. We have categorized various types of Xid errors and analyzed the potential causes that may lead to such errors, as shown in the Table V.

Table VI in Appendix: Supplementary Characterization shows the Xid errors that have occurred in our Fire-Flyer 2 AI-HPC over the past year. In our PCIe-based system, Xid74, also known as NVLink errors, account for a significant proportion, comprising 42.57% of the total. This high frequency is due to the inherent fault rate of NVLink Bridge connectors, amplified by our extensive use of thousands of GPUs.

Software-related errors such as Xid13, Xid31, Xid43, and Xid45 suggest possible illegal memory access or instructions in user code. Notably, illegal memory access (Xid 43) accounts for 33.48%, highlighting the need for improved memory management. However, these errors may also result from memory data corruption, so hardware faults should be considered if software bugs are ruled out.

Additionally, GPU Memory ECC Errors, such as Xid63, Xid64, Xid94, and Xid95, require special attention as they represent about 2% of the total. Figure 10 illustrates the statistics related to ECC errors in our production cluster over the past six months. It is evident that the number of GPU ECC faults considerably surpasses those from the CPU. Therefore, it is crucial to promptly address GPU ECC faults to ensure that application performance and accuracy remain unaffected.

*2) **Network Flash Cut**:* In addition to CPU and GPU faults, network device malfunctions represent a significant portion of hardware issues. As shown in Figure10, IB link failures account for 30% of hardware faults excluding Xid74. Network

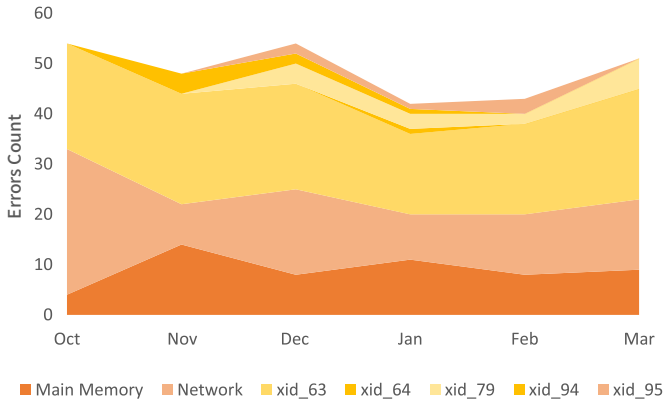


Figure 10: Trends of Memory and Network Failures from 2023 to 2024: "Main Memory" indicates CPU Memory ECC errors, "Network" indicates Network Flash Cuts, and "xids" are related to GPU memory ECC errors. Raw data is available in Appendix: Supplementary Characterization, Table VII

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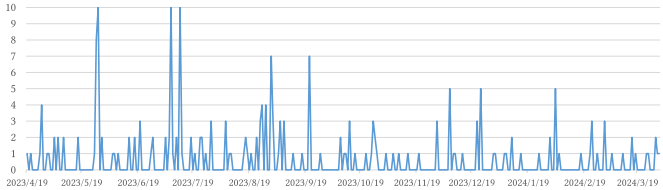

Figure 11: Trends of IB Network Failures: Link Flash Cuts

flash cuts can lead to application communication disruption, even task failures. Since most tasks run on multiple nodes, an issue on a single node can impact many others, further reducing cluster utilization. Figure 11 illustrates the IB link failures data over the past year, with raw data attached in Appendix: Supplementary Characterization, Table VIII, indicating that these issues can occur **randomly** throughout the cluster's operational period.

VIII. Discussion

A. Discussion on Congestion Control in RDMA Networks

Lossless RDMA networks offer several flow-control mechanisms, such as Priority Flow Control (PFC) [89] for RoCE networks and credit-based flow control [90] for IB networks. In network routing, static routing algorithms in IB or ECMP (Equal-Cost Multi-Path) [91] and AR (Adaptive Routing) [92] effectively handle routing issues. However, congestion can still occur when multiple servers send data to a single receiver, potentially blocking the entire network. To mitigate this, IB NICs use DCQCN (Data Center Quantized Congestion Notification) [93] as their congestion control algorithm. While Data Processing Units (DPUs), such as the NVIDIA BF series, allow users to customize congestion control algorithms (like HPCC [94] and TIMELY RTT-based CC [95]), they increase the cost and operational complexity of the cluster.

In practice, we chose to disable DCQCN to avoid its shortcomings, as it could not find parameters that simul-

taneously support HFReduce traffic and 3FS storage traffic in our Computation-Storage Integrated Network. Instead, we employed the network tuning methods mentioned in Section VI-A, ensuring our network operates without congestion control and remains congestion-free.

B. Discussion about NVLink Technology Choices

Initially, we did not use NVLink to avoid extra costs and maintain stability, as HFReduce was sufficient for training requirements at that time. However, as the demand for LLMs increased, we added NVLink specifically for LLM training purposes. The decision to install NVLink should be based on actual needs due to its potential drawbacks.

C. Maintaince Cost Overview

1) Construction Cost: Relative hardware costs are provided in Table II and III. Software costs, contributed by several dozen in-house developers, are just a fraction of the cost for thousands of GPU servers.

2) Power Consumption: The average power consumption comparision during ResNet training is provided in Table II. Including the overhead from IB switches and other nodes, the total energy consumption of the Fire-Flyer 2 AI-HPC does not exceed 4 MW, approximately just over 3 MW.

3) Operation Cost: Operating costs can be estimated by considering power consumption and rack rental costs. By multiplying this figure by the number of nodes and the PUE (Power Usage Effectiveness), the total operating costs can be calculated.

D. Stability Compared with Other Architectures

A recent paper [96] reportsthat NVLink-related failures account for approximately 52.42% (54 out of 103) of total failures, with raw data indicating 54 NVLink Errors, 21 CUDA Errors, 16 Node Failures, 12 ECC Errors, and 12 Network Errors. In comparison, our NVLink-related issues, primarily Xid-74 Errors, as mentioned in Section VII-C1, account for about 42.57% of GPU failures.

IX. Future Work

Future Arch and Integration with New GPU Models

Our next-generation PCIe architecture is designed for MoE (Mixture of Experts) LLM training, where all-to-all performance is crucial. Therefore, the next-gen nodes feature a 1:1 GPU to NIC ratio, comparable to DGX-H100/B100 systems, as illustrated in Figure 12.

We are considering implementing a multi-plane network to reduce costs while maintaining performance. Additionally, we are exploring the use of RoCE switches instead of IB switches, which can significantly lower network expenses. With a 128-port 400 Gbps RoCE switch, a 4-Plane Two-Layer Fat-Trees network can support up to 32,768 GPUs.

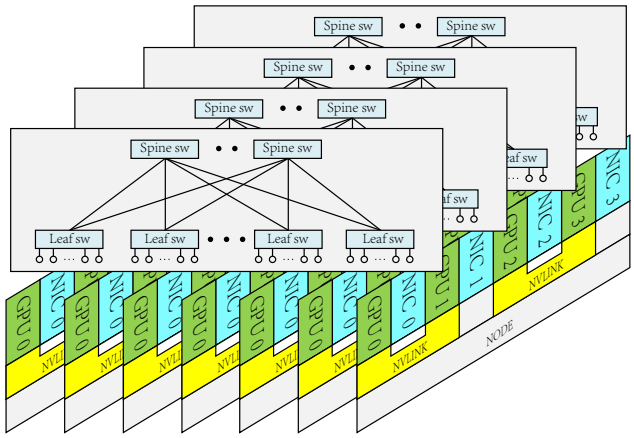

Figure 12: Next Generation PCIe Node Atchitecture with Multi-Plane Fat-Trees Network

X. Conclusions

In this paper, we have shared our experiences and insights from deploying and maintaining the Fire-Flyer 2 AI-HPC, which is equipped with 10,000 PCIe A100 GPUs.Our approach to PCIe architecture and storage-computation integrated network design has resulted in significant cost savings, effectively halving construction costs and demonstrating substantial cost-effectiveness.

In terms of software co-design, we introduced HFReduce and HaiScale to overcome hardware limitations, ensuring scalable performance of the PCIe architecture. Our in-house developed 3FS distributed file system,in conjunction with network co-design, facilitates traffic isolation for both 3FS and HFReduce allreduce traffic, effectively preventing congestion. The comprehensive software stack within the HAI Platform addresses a variety of system faults, from network congestion to hardware failures, thereby ensuring high stability and robustness.

Together, these software and hardware innovations enable our PCIe A100 architecture to achieve 80% the performance of NVIDIA's DGX-A100, while consuming less than 60% of its power. The practical knowledge we have accrued may prove valuable for both industrial and academic sectors. We hope that our work will serve as a reference for others aiming to build their own cost-effective and efficient AI-HPC clusters.

Acknowledgment

We extend our heartfelt gratitude to all our colleagues at DeepSeek-AI and High-Flyer Quant for their invaluable contributions to the Fire-Flyer 2 AI-HPC project. Throughout the four years of design, construction, and operation, their collaborative efforts have been crucial in overcoming numerous challenges. Consequently, Fire-Flyer 2 AI-HPC now supports the training tasks of the DeepSeek-AI series large language models [72], [97]–[101]. We extend a special thanks to the HFAiLab System Team and the Operations Team, whose core contributions have been essential to the success of this endeavor.

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Appendix: Artifact Description/Artifact Evaluation

Artifact Description (AD)

I. Overview of Contributions and Artifacts

A. Paper's Main Contributions

- C_1 Our PCIe A100 architecture managed to attain approximately 80% of NVIDIA DGX A100 performance. TF32 GEMM performance: A100 PCIe 107TFLOPS vs DGX-A100 131TFLOPS. FP16 GEMM performance: A100 PCIe 220TFLOPS vs DGX-A100 263TFLOPS.
- C_2 Our PCIe A100 architecture costs 60% energy consumption of DGX-A100. 2500 Watts A100 PCIe Node vs 4200 Watts DGX-A100.
- C_3 Strong Scalability: HFReduce can achieve an inter-node bandwidth of 7-8GB/s when performing an allreduce test with 186MiB data, scaling from 16 to 1440 GPUs. In the same scenario, NCCL's inter-node bandwidth is only 2-4GB/s.
- C_4 Strong Scalability: Inter-node bandwidth of HFReduce with NVLink can achieve more than 10GB/s. In Cross Fat-Tree Zone operations, HFReduce runs very effectively with minimal performance decay.
- C_5 Weak Scalability: Training VGG16 with HFReduce takes only half the time compared to using the Torch Distributed Data Parallel (DDP) NCCL backend. It achieves nearly 88% parallel scalability when scaling from 32 GPUs to 512.
- C_6 Strong Scalability: When scaling up from 64 GPUs to 512 GPUs, the step time of training LLaMa-13B decreases from 64.118s to 9.717s, achieving a parallel efficiency of 91% at 256 GPUs.
- C_7 Weak Scalability: When training GPT2-medium and scaling from 16 to 128 GPUs, we achieve a parallel scalability of 95%.
- C_8 Our distributed file storage system has achieved a total read throughput of 8TB/s with 180 storage node, 2880 PCIe4.0x4 NVMe SSDs and 360 Mellanox InfiniBand CX6 200G HCAs.

B. Computational Artifacts

Please see files with DOI link:
https://doi.org/10.5281/zenodo.13327567

Download `sc_firefly2_ad_ae.tgz` and extract it. You will get eight folders named `A1` to `A8`, each corresponding to one artifact as follows:

- A_1 sc_firefly2_ad_ae/A1
- A_2 sc_firefly2_ad_ae/A2
- A_3 sc_firefly2_ad_ae/A3
- A_4 sc_firefly2_ad_ae/A4
- A_5 sc_firefly2_ad_ae/A5
- A_6 sc_firefly2_ad_ae/A6
- A_7 sc_firefly2_ad_ae/A7
- A_8 sc_firefly2_ad_ae/A8

Artifact ID	Contributions Supported	Related Paper Elements
A_1	C_1	Table II
A_2	C_2	Table II
A_3	C_3	Figure 7(a)
A_4	C_4	Figure 7(b)
A_5	C_5	Figure 8(a)
A_6	C_6	Figure 9(a)
A_7	C_7	Figure 8(b)
A_8	C_8	Section VI-B2

II. Artifact Identification

A. Computational Artifact A_1

Relation To Contributions

Tested GPU GEMM computation performance by running GEMM calculation code through Torch.

The GEMM of the PCIe card can achieve about 80% of the performance of DGX A100.

Expected Results

TF32 GEMM performance:
1) A100 PCIe: 107TFLOPS;
2) DGX A100: 131TFLOPS.
FP16 GEMM performance:
1) A100 PCIe: 220TFLOPS;
2) DGX A100: 263TFLOPS.

Expected Reproduction Time (in Minutes)

Artifact Setup: 5 minutes.
Artifact Execution: 5 minutes.
Artifact Analysis: 1 minute.

Artifact Setup (incl. Inputs)

Hardware: 1) DGX A100: epyc 7742 * 2, DDR4-3200*16, A100 SXM4 40GB * 8; 2) PCIe A100: epyc Rome 7502 *2, DDR4-3200*16, A100 PCIe 40GB * 8, IB HDR 200G * 1.

Software: Ubuntu20.04 / Python3.8 / PyTorch 1.12 / CUDA 11.3.

Datasets / Inputs: N/A.

Installation and Deployment: Used HaiPlatform ubuntu2004-cu113 image, source haienv 202111.

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A1`.

Obtained results by executing "python bench_gemm.py" on A100 and DGX A100 separately.

Artifact Analysis (incl. Outputs)

Type: torch.float32 N=16384;
time_per_iter: 70399.85 usecs;
average performance: 124.94 TFLOPS.

B. Computational Artifact A_2

Relation To Contributions

As shown in table 1:
1) PCIe A100: 2500 Watts;
2) DGX A100: 4200 Watts.

Power consumption is measured by ResNet50 mdoel training workload.

A ResNet (Residual Neural Network) is a seminal deep learning model in which the weight layers learn residual functions with reference to the layer inputs. ResNet is widely used and very representative.

Expected Results

System power:
1) PCIe A100: about 2500 Watts;
2) DGX A100: about 4200 Watts.

Expected Reproduction Time (in Minutes)

Artifact Setup: 5 minutes.
Artifact Execution: 5 minutes.
Artifact Analysis: 1 minute.

Artifact Setup (incl. Inputs)

Hardware: 1) DGX A100: epyc 7742 * 2, DDR4-3200*16, A100 SXM4 40GB * 8; 2) PCIe A100: epyc Rome 7502 *2, DDR4-3200*16, A100 PCIe 40GB * 8, IB HDR 200G * 1.

Software: Ubuntu 20.04 / Python 3.8 / PyTorch 1.12 / CUDA 11.3.

Datasets / Inputs: ImageNet.

Installation and Deployment: Used HaiPlatform ubuntu2004-cu113 image, source haienv 202111.

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A2`.
1) Allocate one node for testing.
2) Run "python resnet.py".
3) When the training speed is stable, use ipmitool to read the overall machine power consumption.
3.a) PCIe A100: Run "ipmitool sensor get Total_Power" and view the result.
3.b) DGX A100: Run "ipmitool sensor get PWR_SYSTEM" and view the result.

Artifact Analysis (incl. Outputs)

1) PCIe A100:
1.a) Sensor ID: Total_Power;
1.b) Sensor Reading: 2580 (+/- 0) Watts;
2) DGX A100:
2.a) Sensor ID: PWR_SYSTEM;
2.b) Sensor Reading: 4398 (+/- 0) Watts.

C. Computational Artifact A_3

Relation To Contributions

Strong Scalability: HFReduce can achieve an inter-node bandwidth of 7-8GB/s when performing an allreduce test with 186MiB data, scaling from 16 to 1440 GPUs. In the same scenario, NCCL's inter-node bandwidth is only 2-4GB/s.

Expected Results

GPU Count	HFReduce	NCCL
16	8.10	4.01
32	8.03	4.41
64	7.95	4.29
128	7.78	3.73
256	7.12	4.83
512	7.33	4.62
1024	6.31	1.63
1440	6.99	1.65

Expected Reproduction Time (in Minutes)

Artifact Setup: 5 minutes.
Artifact Execution: 20 minutes.
Artifact Analysis: 5 minutes.

Artifact Setup (incl. Inputs)

Hardware: PCIe A100: epyc Rome 7502 *2, DDR4-3200*16, A100 PCIe 40GB * 8, IB HDR 200G * 1.

Software: Ubuntu 20.04 / Python 3.8 / PyTorch 1.12 / CUDA 11.3.

Datasets / Inputs: N/A.

Installation and Deployment: Used HaiPlatform ubuntu2004-cu113 image, source haienv 202111.

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A3`.
See bench_allreduce.py for communication bandwidth test code.

You could login with a platform account and run `submit.sh` script for submitting cluster tasks.

Execution: Run the task submission script, automatically submit tasks from 16 to 1440 GPUs; wait for the tasks to complete, and check the individual execution results.

Artifact Analysis (incl. Outputs)

View the code test results.

NCCL uses ringallreduce for allreduce communication, and the amount of data sent over the network is 2*(N-1)/N of the data that needs to be reduced.

To unify the calculation of network bandwidth, we use 2*(N-1)/N of the algorithm bandwidth as the network bandwidth.

D. Computational Artifact A_4

Relation To Contributions

Strong Scalability: Inter-node bandwidth of HFReduce with NVLink can achieve more than 10GB/s. In Cross Fat-Tree Zone operations, HFReduce runs very effectively with minimal performance decay.

Expected Results

GPU Count	HFReduce with NVLink	HFReduce cross Fat-Tree Zone
16	19.18	N/A
32	13.00	N/A
64	12.07	N/A
128	10.30	9.27
256	9.66	8.63
512	8.56	8.06
1024	7.99	7.75

Expected Reproduction Time (in Minutes)

Artifact Setup: 5 minutes.
Artifact Execution: 20 minutes.
Artifact Analysis: 5 minutes.

Artifact Setup (incl. Inputs)

Hardware: PCIe A100: epyc Rome 7502 *2, DDR4-3200*16, A100 PCIe 40GB * 8, IB HDR 200G * 1.
Software: Ubuntu 20.04 / Python 3.8 / PyTorch 1.12 / CUDA 11.3.
Datasets / Inputs: N/A.
Installation and Deployment: Used HaiPlatform ubuntu2004-cu113 image, source haienv 202111.

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A4`.
See submit.sh for running communication bandwidth test in Fire-Flyer 2 Platform.
You could login with a platform account and run `submit.sh` script for submitting cluster tasks.
Execution: Run the task submission script, automatically submit tasks from 16 to 1024 GPUs; wait for the tasks to complete, and check individual execution results.

Artifact Analysis (incl. Outputs)

View the code test results.
Since the allreduce algorithm first performs a reduce, and then broadcasts the reduced result to all nodes, the amount of data sent over the network is twice the amount of data that needs to be reduced.
To unify the calculation of network bandwidth, we use the same formula as in the previous step: 2*(N-1)/N of the algorithm bandwidth is taken as the network bandwidth.

E. Computational Artifact A_5

Relation To Contributions

Weak Scalability: Training VGG16 with HFReduce takes only half the time compared to using the Torch Distributed Data Parallel (DDP) NCCL backend. It achieves nearly 88% parallel scalability when scaling from 32 GPUs to 512.
The VGG model is based on the paper "Very Deep Convolutional Networks for Large-Scale Image Recognition" and VGG16 is a classical model for image classification tasks.

Expected Results

GPU Count	HFReduce	NCCL
32	0.13	0.27
64	0.133	0.271
128	0.139	0.279
256	0.149	0.287
512	0.15	0.288

Expected Reproduction Time (in Minutes)

Artifact Setup: 5 minutes.
Artifact Execution: 20 minutes.
Artifact Analysis: 5 minutes.

Artifact Setup (incl. Inputs)

Hardware: PCIe A100: epyc Rome 7502 *2, DDR4-3200 *16, A100 PCIe 40GB * 8, IB HDR 200G * 1.
Software: Ubuntu 20.04 / Python 3.8 / PyTorch 1.12 / CUDA 11.3
Datasets / Inputs: ImageNet.
Installation and Deployment: Used HaiPlatform ubuntu2004-cu113 image, source haienv 202207.

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A5`.
See train_vgg16.py for the test code.
You could login with a platform account and run `submit.sh` script for submitting cluster tasks.
Execution: Run the task submission script, automatically submit tasks from 32 to 512 GPUs; wait for the tasks to complete, and check individual execution results.

Artifact Analysis (incl. Outputs)

View the execution results, it will output second/step.

F. Computational Artifact A_6

Relation To Contributions

Strong Scalability: When scaling up from 64 GPUs to 512 GPUs, the step time of training LLaMA 13B decreases from 64.118s to 9.717s, achieving a parallel efficiency of 91% at 256 GPUs. LLaMA (Large Language Model Meta AI) is a family of autoregressive large language models (LLMs), released and open source by Meta AI.

Expected Results

GPU Count	ZBPP + PPO
64	64.12
128	32.51
256	17.45
512	9.72

Expected Reproduction Time (in Minutes)

Artifact Setup: 5 minutes.
Artifact Execution: 20 minutes.
Artifact Analysis: 5 minutes.

Artifact Setup (incl. Inputs)

Hardware: PCIe A100: epyc Milan 7513 *2, DDR4-3200*16, A100 PCIe 40GB * 8, IB HDR 200G * 1.
Software: Ubuntu 20.04 / Python 3.8 / PyTorch 2.01 / CUDA 11.7.
Datasets / Inputs: Wikitext-103.
Installation and Deployment: Used Hai-Platform ubuntu2004-cu113 image and our hai-llm framework.

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A6`.
The hai-llm framework is not yet open source.
You may need login with a platform account and run `submit.sh` script for submitting cluster tasks.
Execution: Run the task submission script, automatically submit tasks from 64 to 512 GPUs; wait for the tasks to complete, and check individual execution results.

Artifact Analysis (incl. Outputs)

View the execution results, it will output second/step.

G. Computational Artifact A_7

Relation To Contributions

Weak Scalability: When training GPT2-medium and scaling from 16 to 128 GPUs, we achieve a parallel scalability of 95%.
GPT-2, developed by OpenAI, is a large-scale unsupervised language model that uses transformer-based deep learning techniques to generate human-like text. It's a classic transformer-based model in NLP.

Expected Results

GPU Count	HaiScale	Torch FSDP
16	0.57	0.86
32	0.58	0.985
64	0.598	0.875
128	0.595	0.99

Expected Reproduction Time (in Minutes)

Artifact Setup: 5 minutes.
Artifact Execution: 20 minutes.
Artifact Analysis: 5 minutes.

Artifact Setup (incl. Inputs)

Hardware: PCIe A100: epyc Rome 7502 *2, DDR4-3200*16, A100 PCIe 40GB * 8, IB HDR 200G * 1.
Software: Ubuntu 20.04 / Python 3.8 / PyTorch 1.12 / CUDA 11.3.
Datasets / Inputs: Wikitext-103.
Installation and Deployment: Used HaiPlatform ubuntu2004-cu113 image, source haienv 202207.

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A7`.
See train_haiscale.py and train_torch_fsdp.py for the test code. You could login with a platform account and run `submit.sh` script for submitting cluster tasks.
Execution: Run the task submission script, automatically submit tasks from 16 to 128 GPUs; wait for the tasks to complete, and check individual execution results.

Artifact Analysis (incl. Outputs)

View the execution results, it will output second/step.

H. Computational Artifact A_8

Relation To Contributions

Our distributed file storage systemhas achieved a total read throughput of 8TB/s with 180 storage node, 2880 PCIe4.0x4 NVMe SSDs and 360 InfiniBand CX6 200G HCAs.

Expected Results

Run fio, the total throughput consistently surpasses 8TB/s.

Expected Reproduction Time (in Minutes)

Artifact Setup: 5 minutes.
Artifact Execution: 10 minutes.
Artifact Analysis: 5 minutes.

Artifact Setup (incl. Inputs)

Hardware: 1) Compute Node: PCIe A100: epyc Rome 7502 *2, DDR4-3200*16, A100 PCIe 40GB * 8, IB HDR 200G * 1; 2) Storage Node: EPYC 7742,DDR4-3200*8, IB HDR 200G * 2, 15.36 NVMe SSD * 16.
Software: Ubuntu 20.04 / Customized version of fio with 3fs custom API / 3FS version 231023-rel-0-70409-8ea13fe7.
Datasets / Inputs: N/A.
Installation and Deployment: The cluster has 180 3FS storage nodes.

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A8`.
You may need login with a platform account and run submit.sh script for submitting cluster tasks.
Execution: Run customized version of `fio` with 3FS custom API on 400 3FS client nodes; wait for 10 minutes.

Artifact Analysis (incl. Outputs)

View the 3FS monitoring dashboard.

Artifact Evaluation (AE)

Evaluation scripts and codes are availble at https://doi.org/10.5281/zenodo.13327567.

We provide the necessary compute resources and nodes for your evaluations. If you would like to evaluate on our Fire-Flyer 2 AIHPC Platform, please contact us via email at ly.zhang@high-flyer.cn to request a platform account and further support.

Please see files with DOI link:

https://doi.org/10.5281/zenodo.13327567

Download `sc_firefly2_ad_ae.tgz` and extract it. You will get eight folders named `A1` to `A8`, each corresponding to one artifact as follows:

A_1	sc_firefly2_ad_ae/A1
A_2	sc_firefly2_ad_ae/A2
A_3	sc_firefly2_ad_ae/A3
A_4	sc_firefly2_ad_ae/A4
A_5	sc_firefly2_ad_ae/A5
A_6	sc_firefly2_ad_ae/A6
A_7	sc_firefly2_ad_ae/A7
A_8	sc_firefly2_ad_ae/A8

A. Computational Artifact A_1

Artifact Setup (incl. Inputs)

Hardware:

- DGX A100: 2x EPYC 7742 CPUs, 16x DDR4-3200, 8x NVIDIA A100 SXM4 40GB GPUs, 9x IB HDR 200G
- PCIe A100: 2x EPYC 7502 CPUs, 16x DDR4-3200, 8x NVIDIA A100 PCIe 40GB GPUs, 1x IB HDR 200G

Software: Ubuntu 20.04 / Python 3.8 / PyTorch 1.12 / CUDA 11.3

Datasets / Inputs: N/A.

Installation and Deployment: Utilized the Fire-Flyer 2 HaiPlatform ubuntu2004-cu113 image, and source haienv 202111

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A1`.

Results were obtained by executing `python bench_gemm.py` on both the A100 and DGX A100 systems separately.

Artifact Analysis (incl. Outputs)

The `bench_gemm.py` script produced the following outputs:

- DGX A100:
  - Type: `torch.float32`, N=8192, Average Performance: 130.17 TFLOPS
  - Type: `torch.bfloat16`, N=8192, Average Performance: 262.87 TFLOPS
- PCIe A100:
  - Type: `torch.float32`, N=8192, Average Performance: 106.37 TFLOPS
  - Type: `torch.bfloat16`, N=8192, Average Performance: 226.52 TFLOPS

The PCIe A100 system achieved over 80% of the performance of the DGX A100 system.

B. Computational Artifact A_2

Artifact Setup (incl. Inputs)

Hardware:

- DGX A100: 2x EPYC Rome 7742 CPUs, 16x DDR4-3200 RAM, 8x NVIDIA A100 SXM4 40GB GPUs, 9x IB HDR 200G HCAs;
- PCIe A100: 2x EPYC Rome 7502 CPUs, 16x DDR4-3200 RAM, 8x NVIDIA A100 PCIe 40GB GPUs, 1x IB HDR 200G HCA.

Software: Ubuntu 20.04 / Python 3.8 / PyTorch 1.12 / CUDA 11.3

Datasets / Inputs: ImageNet https://www.image-net.org/download.php

Installation and Deployment: Utilized the Fire-Flyer 2 HaiPlatform ubuntu2004-cu113 image, and source haienv 202111

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A2`.

1) Allocate one node for running the test script `python train.py`, or simply run `hfai_run.sh`.
2) When the training speed stabilizes, use `ipmitool` to measure the overall machine power consumption.
   a) PCIe A100: Run `ipmitool sensor get Total_Power` and view the result.
   b) DGX A100: Run `ipmitool sensor get PWR_SYSTEM` and view the result.

Artifact Analysis (incl. Outputs)

1) Allocate one node for running the test script `python train.py`, or simply run `hfai_run.sh`.
2) When the training speed stabilizes, use `ipmitool` to measure the overall machine power consumption.
   a) PCIe A100:
      - Sensor ID: `Total_Power`
      - Sensor Reading: 2580 ($\pm$ 0) Watts
   b) DGX A100:
      - Sensor ID: `PWR_SYSTEM`
      - Sensor Reading: 4398 ($\pm$ 0) Watts

C. Computational Artifact A_3

Artifact Setup (incl. Inputs)

Hardware: PCIe A100: 2x EPYC Rome 7502 CPUs, 16x DDR4-3200 RAM, 8x NVIDIA A100 PCIe 40GB GPUs, 1x IB HDR 200G HCA.

Software: Ubuntu 20.04 / Python 3.8 / PyTorch 1.12 / CUDA 11.3

Datasets / Inputs: N/A.

Installation and Deployment: Utilized the Fire-Flyer 2 HaiPlatform ubuntu2004-cu113 image, and source haienv 202111

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A3`.

See bench_allreduce.py for communication bandwidth test code.

You could login with a platform account and run submit.sh script for submitting cluster tasks.

Execution: Run the task submission script, automatically submit tasks from 16 to 1440 GPUs; wait for the tasks to complete, and check the individual execution results.

Artifact Analysis (incl. Outputs)

Each task submitted by `submit.sh` would output results similar to the following:

```
[RANK]: 0 , [hfreduce] size: 1.84e+02 MiB, algoBW 4.634GB/s, Network Bandwidth 8.688367340653281GB/s
```

This **Network Bandwidth** is the expected result. All test cases should get network bandwidth results as follows:

GPU Count	HFReduce	NCCL
16	8.10	4.01
32	8.03	4.41
64	7.95	4.29
128	7.78	3.73
256	7.12	4.83
512	7.33	4.62
1024	6.31	1.63
1440	6.99	1.65

Algorithm Bandwidth and Network Bandwidth:

NCCL (NVIDIA Collective Communications Library) uses the ring-allreduce algorithm for allreduce communication. The amount of data sent over the network is $\frac{2(N-1)}{N}$ times the data that needs to be reduced.

To unify the calculation of network bandwidth, we use $\frac{2(N-1)}{N}$ of the algorithm bandwidth as the network bandwidth.

D. Computational Artifact A_4

Artifact Setup (incl. Inputs)

Hardware: PCIe A100: 2x EPYC Rome 7502 CPUs, 16x DDR4-3200 RAM, 8x NVIDIA A100 PCIe 40GB GPUs, 1x IB HDR 200G HCA.

Software: Ubuntu 20.04 / Python 3.8 / PyTorch 1.12 / CUDA 11.3

Datasets / Inputs: N/A.

Installation and Deployment: Utilized the Fire-Flyer 2 Hai-Platform ubuntu2004-cu113 image, and source haienv 202111

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A4` .

See `submit.sh` for running communication bandwidth test in Fire-Flyer 2 Platform.

You could login with a platform account and run `submit.sh` script for submitting cluster tasks.

Execution: Run the task submission script, automatically submit tasks from 16 to 1024 GPUs; wait for the tasks to complete, and check individual execution results.

Artifact Analysis (incl. Outputs)

Each task submitted by `submit.sh` would output results similar to the following:

```
Algorithm bandwidth: 8.956921GiB/s, Network Bandwidth 16.794226875GB/s
```

This **Network Bandwidth** is the expected result. All test cases should get network bandwidth results as follows:

GPU Count	HFReduce with NVLink	HFReduce cross Fat-Tree Zone
16	19.18	N/A
32	13.00	N/A
64	12.07	N/A
128	10.30	9.27
256	9.66	8.63
512	8.56	8.06
1024	7.99	7.75

E. Computational Artifact A_5

Artifact Setup (incl. Inputs)

Hardware: PCIe A100: 2x EPYC Rome 7502 CPUs, 16x DDR4-3200 RAM, 8x NVIDIA A100 PCIe 40GB GPUs, 1x IB HDR 200G HCA.

Software: Ubuntu 20.04 / Python 3.8 / PyTorch 1.12 / CUDA 11.3

Datasets / Inputs: ImageNet https://www.image-net.org/download.php

Installation and Deployment: Utilized the Fire-Flyer 2 Hai-Platform ubuntu2004-cu113 image, and source haienv 202207

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A5`.

See `train_vgg16.py` for the test code.

You could login with a platform account and run `submit.sh` script for submitting cluster tasks.

Execution: Run the task submission script, automatically submit tasks from 32 to 512 GPUs; wait for the tasks to complete, and check individual execution results.

Artifact Analysis (incl. Outputs)

Each task submitted by `submit.sh` would output results similar to the following:

```
Step 20: 0.1321681 second/step.
```

This **second/step** is the expected result. All test cases should get **second/step** results as follows:

GPU Count	HFReduce	NCCL
32	0.13	0.27
64	0.133	0.271
128	0.139	0.279
256	0.149	0.287
512	0.15	0.288

F. Computational Artifact A_6

Artifact Setup (incl. Inputs)

Hardware: PCIe A100: 2x EPYC Milan 7513 CPUs, 16x DDR4-3200 RAM, 8x NVIDIA A100 PCIe 40GB GPUs, 1x IB HDR 200G HCA.

Software: Ubuntu 20.04 / Python 3.8 / PyTorch 2.01 / CUDA 11.7

Datasets / Inputs: Wikitext-103 https://paperswithcode.com/dataset/wikitext-103

Installation and Deployment: Utilized the Fire-Flyer 2 HAI-Platform ubuntu2004-cu113 image, and source haienv 202207. It is necessary to use our hai-llm framework.

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A6`.

The hai-llm framework is not yet open source. You may need login with a platform account and run `submit.sh` script for submitting cluster tasks.

Execution: Run the task submission script, automatically submit tasks from 64 to 512 GPUs; wait for the tasks to complete, and check individual execution results.

Artifact Analysis (incl. Outputs)

Each task submitted by `submit.sh` would output results similar to the following:

```
RANK 0, step 2, consumed_tokens 0.025
B, loss 0.00000, time 64.089, global_bs
4096, bs 256, 159.695 TFLOPS, util 51.18%
, 63.911123 samples/s
```

This **time 64.089** is the expected result means 64.089 second/s. All test cases should get **second/step** results as follows:

GPU Count	ZBPP + PPO
64	64.12
128	32.51
256	17.45
512	9.72

G. Computational Artifact A_7

Artifact Setup (incl. Inputs)

Hardware: PCIe A100: 2x EPYC Rome 7502 CPUs, 16x DDR4-3200 RAM, 8x NVIDIA A100 PCIe 40GB GPUs, 1x IB HDR 200G.

Software: Ubuntu 20.04 / Python 3.8 / PyTorch 1.12 / CUDA 11.3

Datasets / Inputs: Wikitext-103 https://paperswithcode.com/dataset/wikitext-103

Installation and Deployment: Utilized the Fire-Flyer 2 HAI-Platform ubuntu2004-cu113 image, and source haienv 202207.

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A7`.

See code files `train_haiscale.py` and `train_torch_fsdp.py` for the running test.

You could login with a platform account and run `submit.sh` script for submitting cluster tasks.

Execution: Run the task submission script, automatically submit tasks for from 16 to 128 GPUs; wait for the tasks to complete, and check individual execution results.

Artifact Analysis (incl. Outputs)

Each task submitted by `submit.sh` would output results similar to the following:

```
RANK 0, epoch 1, step 60/929, lr
0.000032 loss 8.383, Speed: 0.87123
seconds/step
```

This **second/step** is the expected result. All test cases should get **second/step** results as follows:

GPU Count	HaiScale	Torch FSDP
16	0.57	0.86
32	0.58	0.985
64	0.598	0.875
128	0.595	0.99

H. Computational Artifact A_8

Artifact Setup (incl. Inputs)

Hardware:

- Compute Node: PCIe A100: 2x EPYC Rome 7502 CPUs, 16x DDR4-3200 RAM, 8x A100 PCIe 40GB GPUs, 1x IB HDR 200G HCA;
- Storage Node: EPYC 7742 CPU, 8x DDR4-3200 RAM, 2x IB HDR 200G HCAs, 16x 15.36TB NVMe SSDs.

Software: Ubuntu 20.04 / Customized version of fio with 3FS custom API / 3FS version 231023-rel-0-70409-8ea13fe7

Datasets / Inputs: N/A.

Installation and Deployment: The cluster has 180 3FS storage nodes. Submit 400 node tasks as clients to perform the fio read benchmark.

Artifact Execution

Refer to the files at `sc_firefly2_ad_ae/A8`.

You may need to log in with a platform account and run the `submit.sh` script to submit cluster tasks. Execute the customized version of fio with the 3FS custom API on 400 3FS client nodes and wait for 10 minutes.

Artifact Analysis (incl. Outputs)

View the 3FS monitoring dashboard to evaluate the total read bandwidth.