ECE 375 PRELAB 6

Lab Time: Wednesday 12-2

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QUESTIONS

1. In computing, there are traditionally two ways for a microprocessor to listen to other devices and communicate: polling and interrupts. Give a concise overview/description of each method, and give a few examples of situations where you would want to choose one method over the other.

   In polling the CPU will cycle through each device or pin that is hooked up for I/O using a protocol that checks to see if it needs any attention. In interrupts it is made in hardware and handled by an interrupt request line that tells the CPU to stop what it is doing and see what needs attention. Polling is good if you have a lot of I/O that need to be checked but the is not critical for the CPU to immediately look at it. Interrupts are good for shorter commands but commands that will need direct attention. Everything on the CPU will stop when one interrupt is being handled.

2. Describe the function of each bit in the following ATmega128 I/O registers: EICRA, EICRB, and EIMSK. Do not just give a brief summary of these registers; give specific details for each bit of each register, such as its possible values and what function or setting results from each of those values. Also, do not just directly paste your answer from the datasheet, but instead try to describe these details in your own words.

   The EICR, or External Interrupt Control Registers, is made up of two 8 bit registers known as EICRA and EICRB. They can have one of four different inputs; 00, 01, 10, 11. 00 will trigger an interrupt request upon low level input, 10 will generate an interrupt request upon the falling edge, 11 will generate an interrupt request upon the rising edge, and 01 will differ between the two registers. For EICRA a value of 01 will be reserved for that value while on the EICRB, any logical change will generate an interrupt request.

   EIMSK or External Interrupt Mask Register controls whether an interrupt should be detected or ignored. Each value that it has as a 1 will be interpreted as enabled/detected. So, if it has a value of 0b00000111, then the only the first three interrupts will be detected.

3. The ATmega128 microcontroller uses interrupt vectors to execute particular instructions when an interrupt occurs. What is an interrupt vector? List the interrupt vector (address) for each of the following ATmega128 interrupts: Timer/Counter0 Overflow, External Interrupt 5, and Analog Comparator.

   Interrupt vectors are used to store the memory location of the interrupt handlers.

   Timer/Counter0 Overflow: $0020

   External Interrupt 5: $000C

   Analog Comparator: $002E

4. Microcontrollers often provide several different ways of configuring interrupt triggering, such as level detection and edge detection. Suppose the signal shown in Figure 1 was connected to a microcontroller pin that was configured as an input and had the ability to trigger an interrupt based on certain signal conditions. List the cycles (or range of cycles) for which an external interrupt would be triggered if that pin's sense control was configured for: (a) rising edge detection, (b) falling edge detection, (c) low level detection, and (d) high level detection. Note: There should be no overlap in your answers, i.e., only one type of interrupt condition can be detected during a given cycle.

(a) Rising Edge: 5-6, 17-18

(b) Falling Edge: 2-3, 8-9

(c) Low Level: 3-5, 9-17

(d) High Level: 0-2, 6-8, 18-21

REFERENCE

https://www.geeksforgeeks.org/difference-between-interrupt-and-polling/#:~:text=In%20interrupt%2C%20the%20device%20notices,whether%20the%20device%20needs%20attention.&text=In%20interrupt%2C%20the%20device%20is,device%20is%20serviced%20by%20CPU.