CMPE 260 Laboratory Exercise 4

Vending Machine

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Performed: March 22nd, 2018
Submitted: March 26th, 2018

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1 Abstract

In this exercise, a vending machine controller with 2 states was designed in VHDL. The goal of the exercise was to learn how to implement state machines in VHDL. The controller took three coin inputs, a drink select, and a drink request. The outputs consisted of error, success, and 7-segment display signals for the machine's balance. The controller was tested successfully with behavioral and post route simulations, and then on a physical Field Programmable Gate Array (FPGA).

2 Design Methodology

For this laboratory exercise, the goal is to implement a vending machine controller. This controller has three coin inputs (for quarters, nickels, and dimes), a drink select input that is four bits wide, and a drink request input. For outputs, it has a soda drop signal, an insufficient funds signal, and a 7-segment display encoding of the monetary balance of the controller. A block diagram of the controller is shown in Figure 1.

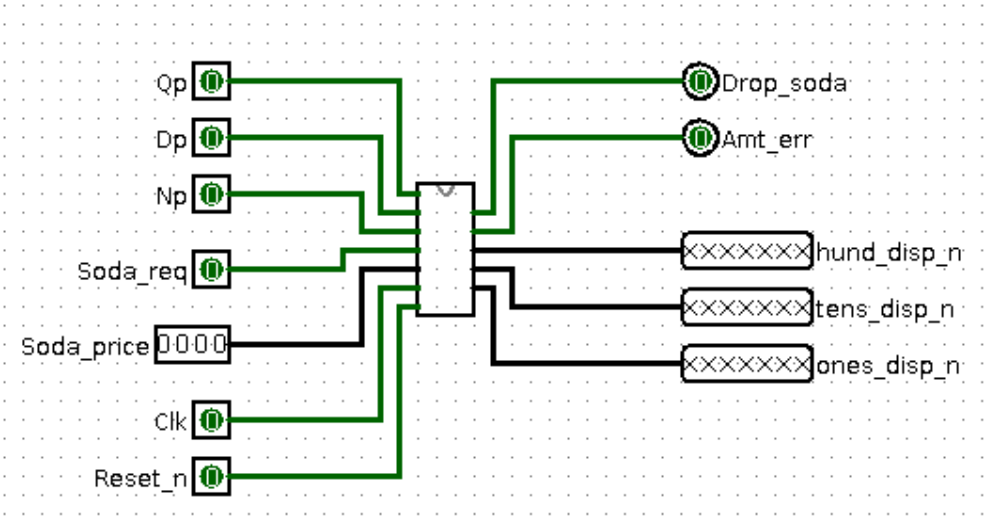

Figure 1: Vending machine controller block diagram

The Controller is implemented with a two-state state machine. The initial state is IDLE. This is also the state that the controller resets to. When a button is pressed, the controller transitions to the PRESSED state and does the logic specified for each button. When the button is no longer pressed, the state transitions back to IDLE. A state transition diagram is shown in Figure 2.

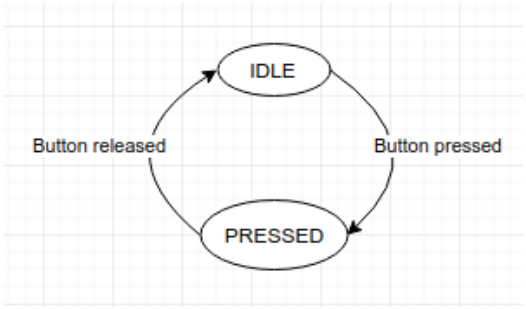

Figure 2: Controller state transition diagram

After the controller was designed, it was implemented in VHDL. A VHDL testbench gave the controller a series

of inputs and compared the outputs to expected ones. This testbench was then used to do a behavioral simulation in GHDL. This simulation was successful.

After the code was successfully simulated, the code was synthesized in Xilinx ISE Project Navigator 14.7. This allowed for a post-route simulation in ModelSim. This simulation was successful.

After synthesis and post-route testing, inputs and outputs were mapped to the switches, buttons, seven-segment display, and LEDS on the Nexys 3 FPGA Development Board for manual testing. This was done using Plan Ahead. Switches were mapped to the selection and reset inputs. Buttons were mapped to the coin inputs. LEDs were mapped to the output. The seven-segment display was mapped to the controller balance.

3 Results

The results of the behavioral simulation are shown in Figure 3.

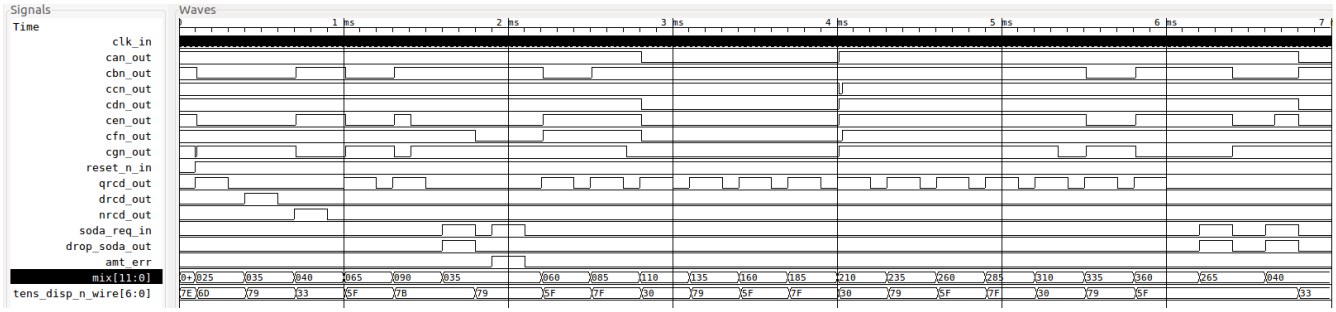

Figure 3: Behavioral simulation

The results of the post-route simulation are shown in Figure 4.

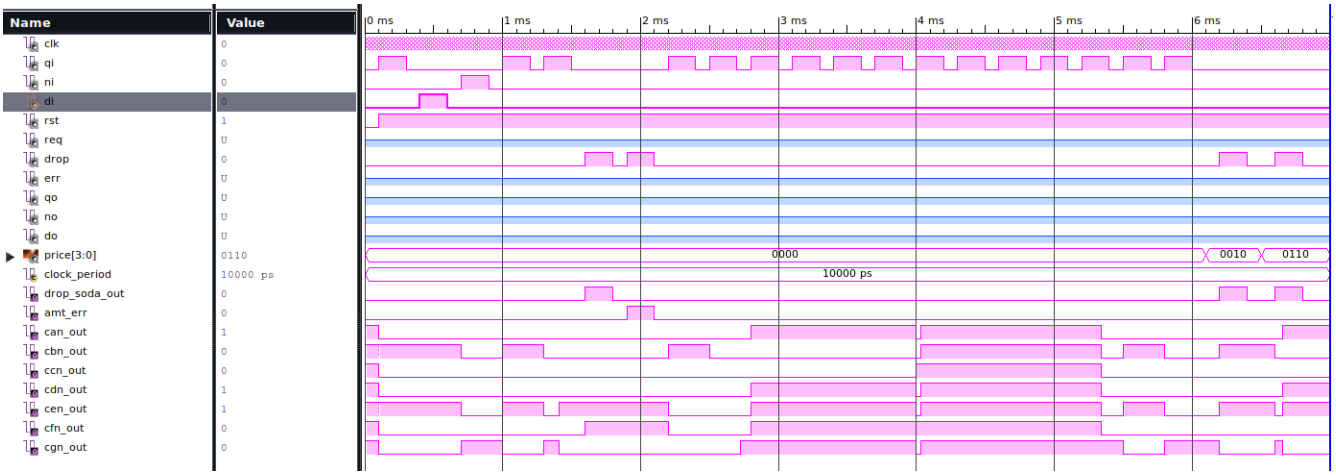

Figure 4: Post-Route simulation

After the FPGA was programmed, it worked successfully.
After synthesis, 113 slices were used, with 360 LUTs used.

4 Conclusion

This exercise was successful. A vending machine controller with 2 states was designed in VHDL. The goal of the exercise was to learn how to implement state machines in VHDL. The controller took three coin inputs, a drink select, and a drink request. The outputs consisted of error, success, and 7-segment display signals for the machine's balance. The controller was tested successfully with behavioral and post route simulations, and then on a physical Field Programmable Gate Array (FPGA).