VHDL Model: M45PExx memory

WARNING:
These VHDL models are provided “as is” without warranty of any kind, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose.

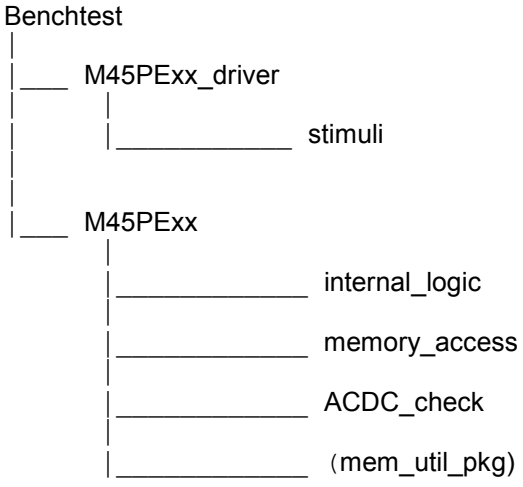
PROJECT ARCHITECTURE

This project offers a VHDL behavioral model of the M45PExx Serial EEPROM and has been built and compiled in VHDL’93 mode optimized for IEEE_std_logic_1164 standard.

a) The VHDL simulation of the M45PExx FLASH is the *M45PExx.vhd* file.
b) In order to offer an example of a complete VHDL project, some other VHDL files are offered and this project is based on two blocks:

- the *M45PExx_driver* block which defines the instructions to transmit to the M45PExx memory
- the *M45PExx* block which simulates the behaviour of the M45PExx memory.

These two blocks are called by the *Benchtest.vhd*.



When compiling all blocks, the project must compile them with the following order:

- mem_util_pkg.vhd
- stimuli.vhd
- internal_logic.vhd
- memory_access.vhd
- ACDC_check.vhd
- M45PExx.vhd
- M45PExx_driver.vhd
- Benchtest.vhd

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VHDL BLOCKS DESCRIPTION

mem_util_pkg.vhd
Tool box containing several functions used by *internal_logic.vhd* , *memory_access.vhd* , and *acdc_check.vhd.*

Stimuli.vhd
Read and Write instructions and Vcc control procedures used to drive the M45PExx _driver.vhd.

internal_logic.vhd
Decodes the SPI protocol and prepares actions for further operations to be performed in the memory array.

memory_access.vhd
Simulates the memory array contents. This contents can be initialized (with the initialization file, see the last paragraph of this document).

ACDC_check.vhd
Performs all checks to be done on received AC timings and VCC value.

M45PExx.vhd
Defines the M45PExx memory device: memory size, page size and AC/DC parameters Min/Max values.

M45PExx_driver.vhd
Simulates an SPI bus Master transmitting instructions to the M45PExx. *M45Pexx_driver.vhd* uses the SPI instructions defined in *Stimuli_SPI.vhd*

benchtest.vhd
Links the *M45PExx_driver.vhd* to the *M45PExx.vhd*.

MESSAGES WHEN RUNNING A SIMULATION

When running a simulation, the M45PExx VHDL model might send warning messages with several severity levels, as commonly used in most VHDL simulators:

Lowest severity

- Note
  - A note message is only informative.
- Warning
  - A warning message informs the user that the M45PExx VHDL model is not properly driven (through the SPI bus) and that the SPI sequence is not compliant with the M45PExx specification
- Error
  - An error message also informs the user that the M45PExx VHDL model is not properly driven (through the SPI bus) and that the SPI sequence is not compliant with the M45PExx specification
- Failure
  - A failure message stops the simulation

Highest severity

Note: although most VHDL development packs offer the possibility to change the severity level in the options menu, it is recommended to keep the initial severity levels (above) as this will insure the safest application check under VHDL.

HOW TO USE THE INITIALIZATION FILE

Default state

An initialization file (*init.txt*) is offered to define the content of the memory array before the simulation starts.

Initialize the memory with your own content

The *init.txt* file is a parameter of the *M45PEXX.vhd* memory model and can be customized in the *benchtest.vhd* module.

The example hereafter shows how to define two M45PExx memories (connected to the same SPI bus) with a different initialization content (named in this example: *init1.txt* and *init2.txt*).

```
-------------------------------------------------------
-----------  body of structural architecture ------------
-------------------------------------------------------
BEGIN
Tester: M45PE80_driver
 PORT MAP(VCC=>Vcc,clk=>clock,din=>data,cs_valid=>S,hard_protect=>W, RESET=>RESET);

Memory1: M45PE80
GENERIC MAP (init_file => string'("init1.txt"))
-- memory initialization with user memory content (all FFh as an example)
 PORT MAP(VCC=>Vcc,C=>clock,D=>data,S=>s,W=>W,RESET =>RESET,Q=>Q);

Memory2: M45PE80
GENERIC MAP (init_file => string'("init2.txt"))
-- memory initialization with user memory content all AAh as an example)
 PORT MAP(VCC=>Vcc,C=>clock,D=>data,S=>s,W=>W,RESET =>RESET,Q=>Q);
```

The format used to define this *Init.txt* initialization file is:

- Each byte is defined in Hexadecimal, using two ASCII characters.
- Bytes are packed into lines of N bytes, N being the M45PExx page size, with no separator between each byte.
- Each line (page) ends with a <CR> (carriage return)

The M45Pexx VHDL model package provides a software tool to convert .BIN files into .txt initialization files. The use of the converter1.1 utility is illustrated below:

- Launch converter1.1 (double click on converter1.1.exe as an example),
- Enter .BIN file name (init.bin as an example)
- Enter .TXT destination file for memory model initialization (initmemory.txt as an example)
- When conversion is finished, the tool window is automatically closed and the .TXT file is available in the converter1.1 directory.