

mMips Optimization Report

Made by :
Martyn van Dijke

March 13, 2016

Contents

1	Problem context	2
2	Possible architecture optimizations	2
2.1	Theoretical speed-up	2
3	Description of improvements	2
4	Testing	2
5	Results	2
6	Conclusion	3
7	References	3

1 Problem context

2 Possible architecture optimizations

Although the mips processor is relatively fast because of the RISC idea, improvements can be made to the architecture of the mips processor next to the architecture improvements, improvements in the compiler itself and the complication of the C code.

All the possible improvements that can be made to the processor are listed below

1. Adding clipping instruction
2. Changing the critical path
3. Forwarding
4. Optimization of the C code
5. Branch prediction
6. Compiler optimizations
7. Multi issue
8. Multi core
9. 64-bit architecture
10. Scalar processing

2.1 Theoretical speed-up

In order to measure the speed up of the processor an equation is need that relates the the number of cycles C to the total execution time T and the frequency f of the processor. This equation is given by

$$T = \frac{C}{f} \quad (1)$$

In order measure the the performance gain of each change in the architecture a equation is needed that relates the relative gain in execution time T this gain G is given by

$$G = \frac{T_{original} - T}{T_{original}} \cdot 100\% \quad (2)$$

With the equations (2) and (1) it is possible to measure the improvement of the processor.

3 Description of improvements

4 Testing

5 Results

Table 1: Speed improvements mMips

Change to the architecture	Number of cycles	Frequency [Hz]	Execution Time [s]	Performance Gain [%]
Reference	2350122	56625000	0.041503258278146	-
Adding own instruction	2315926	56625000	0.040899355408389	1.455073396189640
Changing the critical path	2108766	56626000	0.037240242997916	8.94662611167187

6 Conclusion

7 References