

## 74LVX4245

### 8-Bit Dual Supply Translating Transceiver with 3-STATE Outputs

#### General Description

The LVX4245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 5V bus and a 3V bus in a mixed 3V/5V supply environment. The Transmit/Receive (T/R) input determines the direction of data flow. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B Ports by placing them in a high impedance condition. The A Port interfaces with the 5V bus; the B Port interfaces with the 3V bus.

The LVX4245 is suitable for mixed voltage applications such as laptop computers using 3.3V CPU's and 5V LCD displays.

#### Features

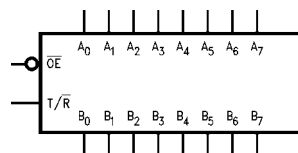
- Bidirectional interface between 5V and 3V buses
- Control inputs compatible with TTL level
- 5V data flow at A Port and 3V data flow at B Port
- Outputs source/sink 24 mA at 5V bus; 12 mA at 3V bus
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Implements patented EMI reduction circuitry
- Functionally compatible with the 74 series 245

#### Ordering Code:

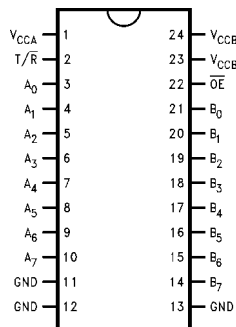
Order Number	Package Number	Package Description
74LVX4245WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVX4245QSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
74LVX4245MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Symbol



#### Connection Diagram



#### Pin Descriptions

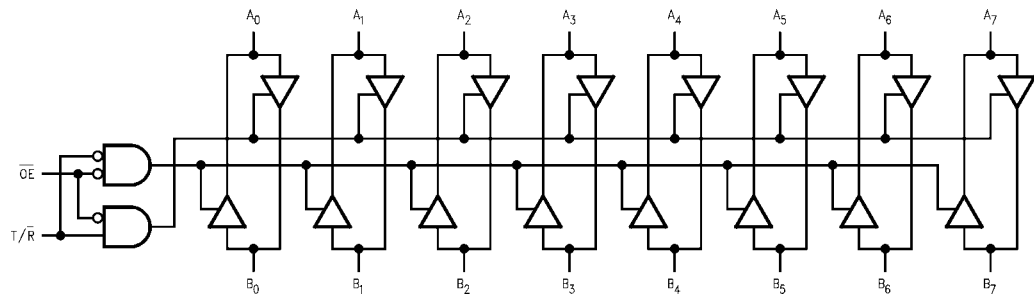
Pin Names	Description
$\overline{OE}$	Output Enable Input
T/R	Transmit/Receive Input
A <sub>0</sub> –A <sub>7</sub>	Side A Inputs or 3-STATE Outputs
B <sub>0</sub> –B <sub>7</sub>	Side B Inputs or 3-STATE Outputs

#### Truth Table

Inputs		Outputs
$\overline{OE}$	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CCA}, V_{CCB}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ ) @ $\overline{OE}$ , $T/\overline{R}$	-0.5V to $V_{CCA} + 0.5V$
DC Input/Output Voltage ( $V_{IO}$ )	
@ $A_n$	-0.5V to $V_{CCA} + 0.5V$
@ $B_n$	-0.5V to $V_{CCB} + 0.5V$
DC Input Diode Current ( $I_{IN}$ )	
@ $\overline{OE}$ , $T/\overline{R}$	$\pm 20$ mA
DC Output Diode Current ( $I_{OK}$ )	$\pm 50$ mA
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ ) and Max Current @ $I_{CCA}$	$\pm 50$ mA
@ $I_{CCB}$	$\pm 200$ mA
Storage Temperature Range ( $T_{STG}$ )	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
DC Latch-Up Source or Sink Current	$\pm 300$ mA

**Recommended Operating Conditions** (Note 2)

Supply Voltage	4.5V to 5.5V
$V_{CCA}$	2.7V to 3.6V
$V_{CCB}$	0V to $V_{CCA}$
Input Voltage ( $V_I$ ) @ $\overline{OE}$ , $T/\overline{R}$	0V to $V_{CCA}$
Input/Output Voltage ( $V_{IO}$ )	
@ $A_n$	0V to $V_{CCA}$
@ $B_n$	0V to $V_{CCB}$
Free Air Operating Temperature ( $T_A$ )	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	8 ns/V
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.0V, 4.5V, 5.5V	

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter		V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	T <sub>A</sub> +25°C		T <sub>A</sub> = -40°C to +85°C	Units	Conditions	
					Typ	Guaranteed Limits				
V <sub>IHA</sub>	Minimum HIGH Level	A <sub>n</sub> , T/ $\overline{R}$ , $\overline{OE}$	5.5	3.3		2.0	2.0	V	V <sub>OUT</sub> ≤ 0.1V or ≥ V <sub>CC</sub> - 0.1V	
V <sub>IHB</sub>		Input Voltage	B <sub>n</sub>	5.0	3.6		2.0			2.0
			5.0	2.7		2.0	2.0			
V <sub>ILA</sub>	Maximum LOW Level	A <sub>n</sub> , T/ $\overline{R}$ , $\overline{OE}$	5.5	3.3		0.8	0.8	V	V <sub>OUT</sub> ≤ 0.1V or ≥ V <sub>CC</sub> -0.1V	
V <sub>ILB</sub>		Input Voltage	B <sub>n</sub>	5.0	2.7		0.8			0.8
			5.0	3.6		0.8	0.8			
V <sub>OHA</sub>	Minimum HIGH Level Output Voltage		4.5	3.0	4.5	4.4	4.4	V	I <sub>OUT</sub> = -100 μA	
				4.5	3.0	4.25	3.86	3.76		I <sub>OH</sub> = -24 mA
V <sub>OHB</sub>			4.5	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = -100 μA	
				4.5	3.0	2.8	2.4		2.4	I <sub>OH</sub> = -12 mA
				4.5	2.7	2.5	2.4		2.4	I <sub>OL</sub> = -8 mA
V <sub>OLA</sub>	Maximum LOW Level Output Voltage		4.5	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> =100 μA	
				4.5	3.0	0.18	0.36	0.44		I <sub>OL</sub> = 24 mA
V <sub>OLB</sub>			4.5	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 100 μA	
				4.5	3.0	0.1	0.31		0.4	I <sub>OL</sub> = 12 mA
				4.5	2.7	0.1	0.31		0.4	I <sub>OL</sub> = 8 mA
I <sub>IN</sub>	Maximum Input Leakage Current @ $\overline{OE}$ , T/ $\overline{R}$		5.5	3.6		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CCA</sub> , GND	
I <sub>OZA</sub>	Maximum 3-STATE Output Leakage @ A <sub>n</sub>		5.5	3.6		±0.5	±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> $\overline{OE}$ = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCA</sub> , GND	
I <sub>OZB</sub>	Maximum 3-STATE Output Leakage @ B <sub>n</sub>		5.5	3.6		±0.5	±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> $\overline{OE}$ = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCB</sub> , GND	
ΔI <sub>CC</sub>	Maximum I <sub>CCT</sub> /Input @ A <sub>n</sub> , T/ $\overline{R}$ , $\overline{OE}$		5.5	3.6	1.0	1.35	1.5	mA	V <sub>I</sub> = V <sub>CCA</sub> - 2.1V	
	Input @ B <sub>n</sub>		5.5	3.6		0.35	0.5	mA	V <sub>I</sub> = V <sub>CCB</sub> - 0.6V	

## DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		Units	Conditions
				Typ	Guaranteed Limits				
I <sub>CCA</sub>	Quiescent V <sub>CCA</sub> Supply Current	5.5	3.6		8	80		μA	A <sub>n</sub> = V <sub>CCA</sub> or GND B <sub>n</sub> = V <sub>CCB</sub> or GND, OE = GND T/R = GND
I <sub>CCB</sub>	Quiescent V <sub>CCB</sub> Supply Current	5.5	3.6		5	50		μA	A <sub>n</sub> = V <sub>CCA</sub> or GND B <sub>n</sub> = V <sub>CCB</sub> or GND, OE = GND T/R = V <sub>CCA</sub>
V <sub>OLPA</sub> V <sub>OLPB</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0 5.0	3.3 3.3		1.5 0.8			V	(Note 4)(Note 5)
V <sub>OLVA</sub> V <sub>OLVB</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0 5.0	3.3 3.3		−1.2 −0.8			V	(Note 4)(Note 5)
V <sub>IHDA</sub> V <sub>IHDB</sub>	Minimum HIGH Level Dynamic Input Voltage	5.0 5.0	3.3 3.3		2.0 2.0			V	(Note 4)(Note 6)
V <sub>ILDA</sub> V <sub>ILDB</sub>	Maximum LOW Level Dynamic Input Voltage	5.0 5.0	3.3 3.3		0.8 0.8			V	(Note 4)(Note 6)

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** Worst case package.

**Note 5:** Max number of outputs defined as (n). Data inputs are driven 0V to V<sub>CC</sub> level; one output at GND.

**Note 6:** Max number of Data Inputs (n) switching. (n-1) inputs switching 0V to V<sub>CC</sub> level. Input-under-test switching:  
V<sub>CC</sub> level to threshold (V<sub>IHD</sub>), 0V to threshold (V<sub>ILD</sub>), f = 1 MHz.

## AC Electrical Characteristics

Symbol	Parameters	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF V <sub>CCA</sub> = 5V (Note 7) V <sub>CCB</sub> = 3.3V (Note 8)			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF V <sub>CCA</sub> = 5V (Note 7) V <sub>CCB</sub> = 3.3V (Note 8)		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF V <sub>CCA</sub> = 5V (Note 7) V <sub>CCB</sub> = 2.7V		Units
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay A to B	1.0 1.0	5.1 5.3	8.5 8.5	1.0 1.0	9.0 9.0	1.0 1.0	10.0 10.0	ns
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay B to A	1.0 1.0	5.4 5.5	8.5 8.5	1.0 1.0	9.0 9.0	1.0 1.0	10.0 10.0	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time OE to B	1.0 1.0	6.5 6.7	10.0 10.0	1.0 1.0	10.5 10.5	1.0 1.0	11.5 11.5	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time OE to A	1.0 1.0	5.2 5.8	9.0 9.0	1.0 1.0	9.5 9.5	1.0 1.0	10.0 10.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OE to B	1.0 1.0	6.0 3.3	9.5 6.5	1.0 1.0	10.0 7.0	1.0 1.0	10.0 7.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OE to A	1.0 1.0	3.9 2.9	7.0 6.5	1.0 1.0	7.5 7.0	1.0 1.0	7.5 7.5	ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output to Output Skew (Note 9) Data to Output		1.0	1.5		1.5		1.5	ns

**Note 7:** Voltage Range 5.0V is 5.0V ± 0.5V.

**Note 8:** Voltage Range 3.3V is 3.3V ± 0.3V.

**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

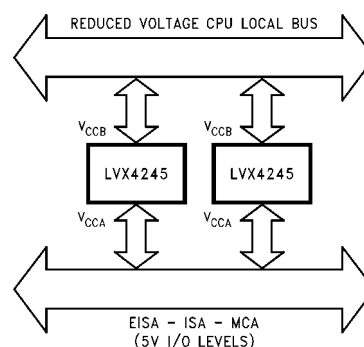
Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
$C_{I/O}$	Input/Output Capacitance	15	pF	$V_{CCA} = 5.0V$ $V_{CCB} = 3.3V$
$C_{PD}$	Power Dissipation Capacitance (Note 10)	B→A	55	pF
		A→B	40	pF

**Note 10:**  $C_{PD}$  is measured at 10 MHz

## 8-Bit Dual Supply Translating Transceiver

The LVX4245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX4245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



## Power Up Considerations

To insure the system does not experience unnecessary  $I_{CC}$  current draw, bus contention, or oscillations during power up, the following guidelines should be adhered to (refer to Table 1):

- Power up the control side of the device first. This is the  $V_{CCA}$ .
- $\overline{OE}$  should ramp with or ahead of  $V_{CCA}$ . This will help guard against bus contention.
- The Transmit/Receive control pin ( $T/\overline{R}$ ) should ramp with or ahead of  $V_{CCA}$ , this will ensure that the A Port data

pins are configured as inputs. With  $V_{CCA}$  receiving power first, the A I/O Port should be configured as inputs to help guard against bus contention and oscillations.

- A side data inputs should be driven to a valid logic level. This will prevent excessive current draw.

The above steps will ensure that no bus contention or oscillations, and therefore no excessive current draw occurs during the power up cycling of these devices. These steps will help prevent possible damage to the translator devices and potential damage to other system components.

**TABLE 1. Low Voltage Translator Power Up Sequencing Table**

Device Type	$V_{CCA}$	$V_{CCB}$	$T/\overline{R}$	$\overline{OE}$	A Side I/O	B Side I/O	Floatable Pin Allowed
74LVX4245	5V (power up 1st)	3V (power up 2nd)	ramp with $V_{CCA}$	ramp with $V_{CCA}$	logic 0V or $V_{CCA}$	outputs	No

Please reference Application Note AN-5001 for more detailed information on using Fairchild's LVX Low Voltage Dual Supply CMOS Translating Transceivers.

## Applications: Mixed Mode Dual Supply Interface Solution

LVX4245 is designed to solve 3V/5V interfacing issues when CMOS devices cannot tolerate I/O levels above their applied  $V_{CC}$ . If an I/O pin of 3V ICs is driven by 5V ICs, the P-Channel transistor in 3V ICs will conduct causing current flow from I/O bus to the 3V power supply. The resulting high current flow can cause destruction of 3V ICs through latchup effects. To prevent this problem, a current limiting resistor is used typically under direct connection of 3V ICs and 5V ICs, but it causes speed degradation.

In a better solution, the LVX4245 configures two different output levels to handle the dual supply interface issues. The "A" port is a dedicated 5V port to interface 5V ICs. The "B" port is a dedicated port to interface 3V ICs. *Figure 2* shows how LVX4245 fits into a system with 3V subsystem and 5V subsystem.

This device is also configured as an 8-bit 245 transceiver, giving the designer 3-STATE capabilities and the ability to select either bidirectional or unidirectional modes. Since the center 20 pins are also pin compatible to 74 series 245, as shown in *Figure 1*, the designer could use this device in

either a 3V system or a 5V system without any further work to re-layout the board.

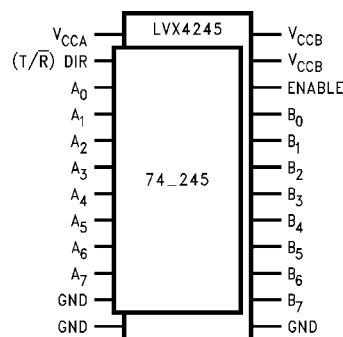


FIGURE 1. LVX4245 Pin Arrangement is Compatible to 20-Pin 74 Series 245

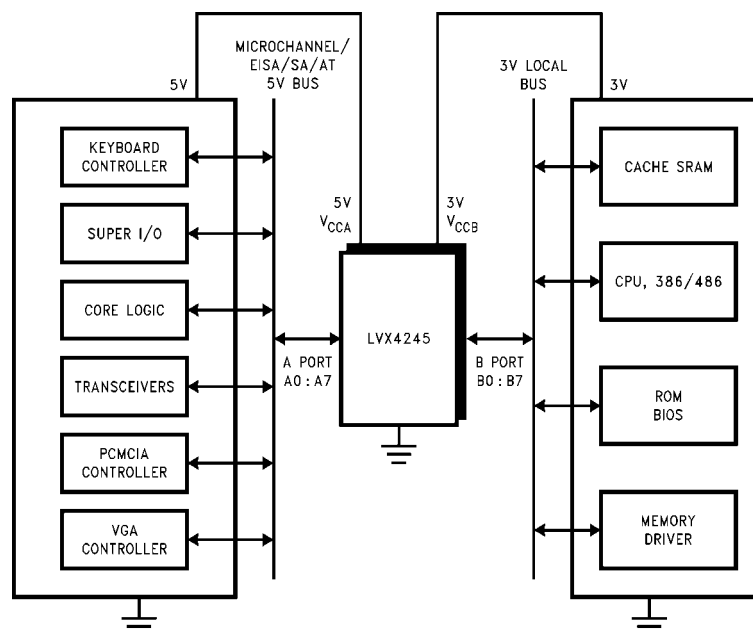
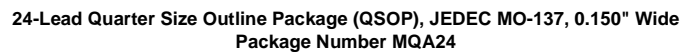
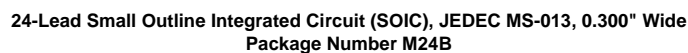
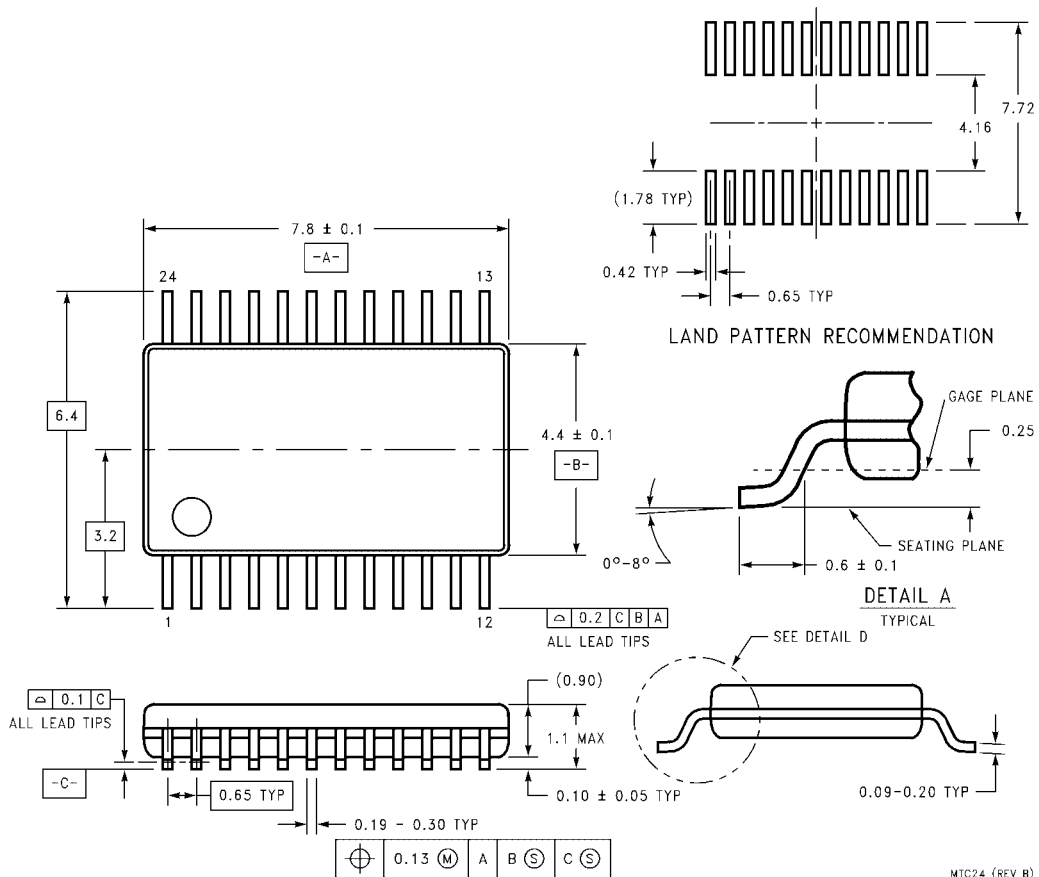


FIGURE 2. LVX4245 Fits into a System with 3V Subsystem and 5V Subsystem



## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC24

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