

DATA SHEET

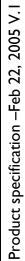
ARRAY CHIP RESISTORS

YC324 (8Pin/4R; Pb Free)

5%, 1% sizes 1220



YAGEO







Chip Resistor Surface Mount

SERIES

324 (Pb Free)

SCOPE

This specification describes YC324 series chip resistor arrays with lead-free terminations made by thick film process.

ORDERING INFORMATION

Part number is identified by the series, size, tolerance, packing type, temperature coefficient, taping reel and resistance value.

YAGEO ORDERING CODE

CTC CODE

YC324 - X X X XX XXXX L (1) (2) (3) (4) (5) (6)

(I) TOLERANCE

 $F = \pm 1\%$ $| = \pm 5\%$

(2) PACKAGING TYPE

K = Embossed taping reel

(3) TEMPERATURE COEFFICIENT OF RESISTANCE

- = Base on spec

(4) TAPING REEL

07 = 7 inch dia. Reel

(5) RESISTANCE VALUE

56R, 560R, 5K6, 56K, 1M

(6) RESISTOR TERMINATIONS

L = Lead free terminations (pure Tin)

ORDERING EXAMPLE

The ordering code of a YC324 convex chip resistor array, value 1,000 Ω with ±5% tolerance, supplied in 7-inch tape reel is: YC324-JK-071KL.

NOTE

- The "L" at the end of the code is only for ordering. On the reel label, the standard CTC will be mentioned an additional stamp "LFP"= lead free production.
- 2. Products with lead in terminations fulfil the same requirements as mentioned in this datasheet.
- 3. Products with lead in terminations will be phased out in the coming months (before July 1st, 2006)





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MARKING

YC324



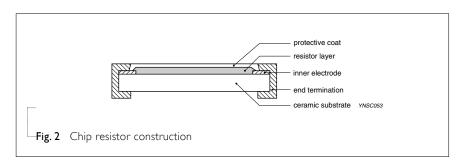
E-24 series: 3 digits

First two digits for significant figure and 3rd digit for number of zeros

For marking codes, please see EIA-marking code rules in data sheet "Chip resistors marking".

CONSTRUCTION

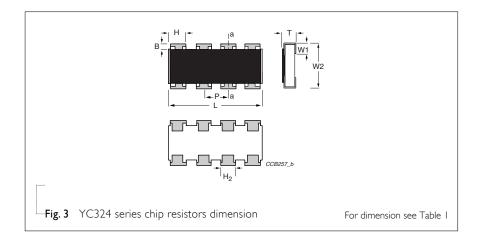
The resistors are constructed out of a high-grade ceramic body. Internal metal electrodes are added at each end and connected by a resistive paste. The composition of the paste is adjusted to give the approximate required resistance and laser cutting of this resistive layer that achieves tolerance trims the value. The resistive layer is covered with a



protective coat. Finally, the eight external terminations (pure Tin) are added. See fig. 2.

DIMENSIONS

Table I	
TYPE	YC324
B (mm)	0.50 ±0.20
H (mm)	1.10 ±0.15
P (mm)	1.27 ±0.05
L (mm)	5.08 ±0.20
H ₂ (mm)	0.90 ±0.15
T (mm)	0.60 ±0.10
W _I (mm)	0.50 ±0.15
W ₂ (mm)	3.20 ±0.20



SCHEMATIC





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ELECTRICAL CHARACTERISTICS

Table 2			
CHARACTERISTICS	YC324 1/8 W		
Operating Temperature Range	–55 °C to +155 °C		
Maximum Working Voltage	200 V		
Maximum Overload Voltage	500 V		
Dielectric Withstanding Voltage	500 V		
Number of Resistors	4		
Resistance Range	5% (E24) 10 Ω to MΩ		
Resistance Range	I% (E24/E96) $$ I0 Ω to I M Ω		
Temperature Coefficient	±200 ppm/°C		

<u>FOOTPRINT AND SOLDERING</u> PROFILES

For recommended footprint and soldering profiles, please see the special data sheet "Chip resistors mounting".

ENVIRONMENTAL DATA

For material declaration information (IMDS-data) of the products, please see the separated info "Environmental data" conformed to EU RoHS.

PACKING STYLE AND PACKAGING QUANTITY

Table 3 Packing style and packaging quantity

PRODUCT TYPE	PACKING STYLE	REEL DIMENSION	QUANTITY PER REEL
YC324	Embossed taping reel (K)	7" (178 mm)	4,000 units

NOTE

1. For embossed tape and reel specification/dimensions, please see the special data sheet "Packing" document.

FUNCTIONAL DESCRIPTION

POWER RATING

YC324 rated power at 70°C is I/8 W

RATED VOLTAGE

The DC or AC (rms) continuous working voltage corresponding to the rated power is determined by the following formula:

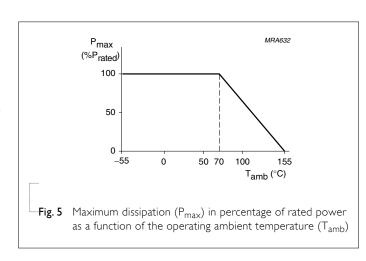
$$V = \sqrt{(P \times R)}$$

Where

V = Continuous rated DC or AC (rms) working voltage (V)

P = Rated power (W)

 $R = Resistance value (\Omega)$





TESTS AND REQUIREMENTS

Table 4 Test condition, procedure and requirements

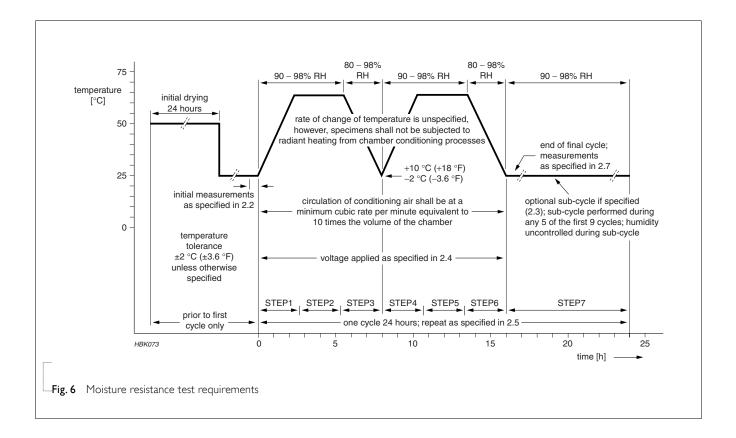
TEST	TEST METHOD	PROCEDURE	REQUIREMENTS
Temperature Coefficient of	MIL-STD-202F-method 304; JIS C 5202-4.8	At +25/−55 °C and +25/+125 °C	Refer to table 2
Resistance	JIS C 3202-4.0	Formula:	
(T.C.R.)		T.C.R = $\frac{R_2 - R_1}{R_1(t_2 - t_1)} \times 10^6 \text{ (ppm/°C)}$	
		Where $t_1 = +25$ °C or specified room temperature	
		$t_2 = -55$ °C or +125 °C test temperature	
		R_1 = resistance at reference temperature in ohms	
		R_2 = resistance at test temperature in ohms	
Thermal Shock	MIL-STD-202F-method 107G;	At -65 (+0/-10) °C for 2 minutes and at +155	$\pm (0.5\% + 0.05 \ \Omega)$ for 1% tol.
	IEC 60115-1 4.19	(+10/-0) °C for 2 minutes; 25 cycles	$\pm ($ 1.0% +0.05 $\Omega)$ for 5% tol.
Low	MIL-R-55342D-Para 4.7.4	At -65 (+0/-5) °C for I hour; RCWV applied for	$\pm (0.5\% + 0.05 \ \Omega)$ for 1% tol .
Temperature		45 (+5/–0) minutes	$\pm (1.0\%$ +0.05 $\Omega)$ for 5% tol.
Operation			No visible damage
Short Time	MIL-R-55342D-Para 4.7.5;	2.5 × RCWV applied for 5 seconds at room	\pm (1.0% +0.05 Ω) for 1% tol.
Overload	IEC 60115-1 4.13	temperature	$\pm (2.0\% + 0.05 \ \Omega)$ for 5% tol.
			No visible damage
Insulation	MIL-STD-202F-method 302;	RCOV for I minute	≥10 GΩ
Resistance	IEC 60115-1 4.6.1.1	Type YC324	
		Voltage (DC) 500 V	
Dielectric	MIL-STD-202F-method 301;	Maximum voltage (V _{ms}) applied for 1 minute	No breakdown or flashover
Withstand Voltage	IEC 60115-1 4.6.1.1	Type YC324	
		Voltage (AC) 500 V _{rms}	
		11113	
Resistance to Soldering Heat	MIL-STD-202F-method 210C;	Unmounted chips; 260 ± 5 °C for 10 ± 1 seconds	$\pm (0.5\%$ +0.05 $\Omega)$ for 1% tol.
	IEC 60115-1 4.18		$\pm (1.0\%$ +0.05 $\Omega)$ for 5% tol.
			No visible damage
Life	MIL-STD-202F-method 108A;	At 70 ±2 °C for 1,000 hours; RCWV applied for	$\pm (1\% +0.05 \Omega)$ for 1% tol.
	IEC 60115-1 4.25.1	1.5 hours on and 0.5 hour off	$\pm(3\% + 0.05 \Omega)$ for 5% tol.



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TEST	TEST METHOD	PROCEDURE	REQUIREMENTS	
Solderability	MIL-STD-202F-method 208A;	Solder bath at 245 ±3 °C	Well tinned (≥95% cov	ered)
	IEC 60115-1 4.17	Dipping time: 2 ±0.5 seconds	No visible damage	
Bending	JIS C 5202.6.14;	Resistors mounted on a 90 mm glass epoxy	\pm (1.0% +0.05 Ω) for 19	% tol.
Strength	IEC 60115-1 4.15	resin PCB (FR4)	\pm (1.0% +0.05 Ω) for 5% tol.	
		Bending: I mm	No visible damage	
Resistance to	MIL-STD-202F-method 215;	Isopropylalcohol (C ₃ H ₇ OH) or dichloromethane	No smeared	
Solvent	IEC 60115-1 4.29	(CH ₂ Cl ₂) followed by brushing		
Noise	JIS C 5202 5.9;	Maximum voltage (V _{rms}) applied.	Resistors range	Value
	IEC 60115-1 4.12		R < 100 Ω	10 dB
			$100 \Omega \le R < 1 K\Omega$	20 dB
			$1 \text{ K}\Omega \leq R < 10 \text{ K}\Omega$	30 dB
			$10 \text{ K}\Omega \leq R < 100 \text{ K}\Omega$	40 dB
			$100 \text{ K}\Omega \leq \text{R} < 1 \text{ M}\Omega$	46 dB
			$-$ I M $\Omega \le R \le 22 M\Omega$	48 dB
Humidity	JIS C 5202 7.5;	I,000 hours; 40 ±2 °C; 93(+2/-3)% RH	\pm (0.5% +0.05 Ω) for 15	% tol.
(steady state)	IEC 60115-8 4.24.8	RCWV applied for 1.5 hours on and 0.5 hour off	$\pm (2.0\% + 0.05 \Omega)$ for 5% tol.	
Leaching	EIA/IS 4.13B;	Solder bath at 260 ±5 °C	No visible damage	
	IEC 60115-8 4.18	Dipping time: 30 ± 1 seconds		
Intermittent Overload	JIS C 5202 5.8	At room temperature; 2.5 × RCWV applied for	\pm (1.0% +0.05 Ω) for 19	% tol.
		I second on and 25 seconds off; total 10,000 cycles	$\pm (2.0\% + 0.05 \Omega)$ for 5% tol.	
Resistance to Vibration	On request	On request		
Moisture	MIL-STD-202F-method 106F;	42 cycles; total 1,000 hours	±(0.5% +0.05Ω) for 1%	6 tol.
Resistance Heat	IEC 60115-1 4.24.2	Shown as Fig. 6	$\pm (2.0\% + 0.05\Omega)$ for 5% tol.	
			No visible damage	

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REVISION HISTORY

REVISION	DATE	CHANGE NOTIFICATION	DESCRIPTION
Version I	Feb 22, 2005	-	- Test method and procedure updated
Version 0	Nov. 10, 2003	-	- First issue of PbFree specification