

GATE input voltage is LOW then P-channel MOSFET connected in the circuit will be turned ON letting VBAT flow to LDO

The diagram illustrates a P-channel MOSFET circuit used for pre-regulating the input voltage of an LDO. The MOSFET (Q2, Si2301) has its source connected to +VBAT and its drain connected to the LDO's input (D5). The gate of the MOSFET is driven by +VBUS through a 10K resistor (R10). A diode (D4) is connected from the MOSFET's drain to ground. The LDO (U2, MCP1700-3302E) has its input (VI) connected to the MOSFET's drain, its output (VO) connected to +3V3, and its ground (GND) connected to ground. Input and output capacitors C1 and C2 (10uF) are shown.

[illegible]

REVISION HISTORY:  
v1.0 Left / Right pins swapped because Martin never  
.. used an SWD programmer  
v1.1 Corrected after looking up the pinout

The diagram shows a 10-pin connector labeled CN1. The pins are numbered 1 through 10. The connections are as follows:

- Pin 1: SWDIO (green line)
- Pin 3: SWCLK (orange line)
- Pin 4: +3V3 (red line with an upward arrow)
- Pin 5: MCU\_RST (red line)
- Pin 6: GND (green line with a downward arrow)
- Pin 7: GND (green line with a downward arrow)
- Pin 8: GND (green line with a downward arrow)
- Pin 9: GND (green line with a downward arrow)
- Pin 10: GND (green line with a downward arrow)

There are also two crossed-out connections:

- Pin 2: SWDIO (green line with an 'X')
- Pin 7: SWCLK (orange line with an 'X')

Below the diagram, the text "HX JN1.27-2X5 TP H4.9" is displayed.

The diagram shows the USB\_C\_Receptacle\_USB2.0 module with the following connections:

- VBUS:** Connected to pin A4.
- CC1:** Connected to pin A5.
- CC2:** Connected to pin B5.
- D-:** Connected to pins A7 and B7.
- D+:** Connected to pins A6 and B6.
- SBU1:** Connected to pin A8.
- SBU2:** Connected to pin B8.
- Shield:** Connected to pin S1.
- Resistors:** R1 (5.1k) and R20 (5.1k) are connected between the D- and D+ lines and GND.
- Grounding:** Pins A1 and S1 of the J1 connector are connected to GND.

The schematic diagram illustrates the internal circuitry of the AF24-S24FIC-00 module. The module's 24 pins are connected to various components:

- Pin 1 (VCOM):** Connected to TP2 and a 10k pull-up resistor (R3) to +3V3.
- Pin 2 (PREVGL):** Connected to a 4.7uF capacitor (C8) to GND.
- Pin 3 (VSH):** Connected to a 4.7uF capacitor (C11) to GND.
- Pin 4 (VSS):** Connected to GND.
- Pin 5 (VDD):** Connected to a 4.7uF capacitor (C10) to GND.
- Pin 6 (VDD):** Connected to a 4.7uF capacitor (C9) to GND.
- Pin 7 (VDD):** Connected to GND.
- Pin 8 (VDD):** Connected to GND.
- Pin 9 (VDD):** Connected to GND.
- Pin 10 (VDD):** Connected to GND.
- Pin 11 (EPD\_MOSI):** Connected to GND.
- Pin 12 (EPD\_CLK):** Connected to GND.
- Pin 13 (EPD\_CS):** Connected to GND.
- Pin 14 (EPD\_DC):** Connected to GND.
- Pin 15 (EPD\_RST):** Connected to GND.
- Pin 16 (EPD\_BUSY):** Connected to GND.
- Pin 17 (GND):** Connected to GND.
- Pin 18 (GND):** Connected to GND.
- Pin 19 (VGH):** Connected to a 4.7uF capacitor (C6) to GND.
- Pin 20 (VGL):** Connected to a 4.7uF capacitor (C7) to GND.
- Pin 21 (VGL):** Connected to a 4.7uF capacitor (C7) to GND.
- Pin 22 (RESE):** Connected to a 10k resistor (R7) to GND.
- Pin 23 (GDR):** Connected to a 10k resistor (R7) to GND.
- Pin 24 (GDR):** Connected to a 10k resistor (R7) to GND.

The module is powered by +3V3 and GND. The output is labeled EPD\_RST.

SM04B-SR55-TB\_LF\_SN\_

Diagram of a 7-pin connector J3 (Conn\_01x07) with the following pin assignments:

- Pin 1: P1.00
- Pin 2: P0.22
- Pin 3: P0.20
- Pin 4: P0.26
- Pin 5: P0.13
- Pin 6: +3V3
- Pin 7: GND