

Diagram illustrating the components of the open source hardware:

- open source hardware
- H1 MountingHole
- H2 MountingHole
- H3 MountingHole
- H4 MountingHole

SM04B-SRSS-TB_LF__SN_

The diagram shows the SGM6029 CYG/TR voltage converter circuit. The input is VDD, which is connected to the GND pin (A1) and the EN pin (C2). The VDD33 input is connected to the VOS pin (A2) and the VIN pin (B1). The EN pin (C1) is connected to the SW pin (B2). The SW pin (B2) is connected to the output of the converter, which is connected to GND. The output is also connected to a 249k 1% resistor (R3) and a 0.47 uH inductor (L2). The inductor (L2) is connected to a 10 uF capacitor (C3), which is connected to GND. A 10 uF capacitor (C2) is connected to the input VDD and GND.

[illegible]

• superCAP needs to be hand-soldered

GATE input voltage is LOW then P-channel MOSFET connected in the circuit will be turned ON letting VBAT flow to LDO

The diagram illustrates a P-channel MOSFET-based LDO pre-regulator circuit. The MOSFET (Q2, Si2301CDS) is controlled by a gate voltage divider (R10, R11) connected to VBUS and GND. The MOSFET's source is connected to VBAT, and its drain is connected to the LDO's VCC pin. The LDO (U3, TP4057-42-SOT26-R) has its GND and *CHRG pins connected to the MOSFET drain. Its PROG pin is connected to a divider (R12, R13) between VBUS and GND. Its STDBY pin is connected to the MOSFET gate. A diode D6 is connected between VBUS and the LDO's output.

J3
SM02B-SRSS-TB(LF)(SN)

MP1 1 1
MP2 2 2

VBAT
GND

Wiring diagram for J5 connector:

- Pin 4: OLEDA → SDA
- Pin 3: SCL
- Pin 2: +3.3V
- Pin 1: GND

IC1
W25Q80DV55IG

Pin 1: SPICS0
Pin 2: DO_ (I/O1)
Pin 3: SPI_D2
Pin 4: WP_ (I/O2)
Pin 5: GND
Pin 6: HOLD_ (I/O3)
Pin 7: CLK
Pin 8: DL_ (I/O0)

External Connections:
SPI_D1 (to Pin 2)
SPI_D2 (to Pin 3)
SPI_D0 (to Pin 5)
SPI_D3 (to Pin 7)
SPIVDD (to Pin 8)
GND (to Pin 4)

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