

Diagram illustrating the concept of open source hardware. A red gear icon is labeled "open source hardware". To its right, four red circular nodes are shown, each labeled with a number and the text "MountingHole":

- #H1 MountingHole
- #H2 MountingHole
- #H3 MountingHole
- #H4 MountingHole

The diagram shows the SGM6029 CYG/TR voltage converter circuit. The input is VDD, which is connected to the EN pin (C2) and the SW pin (B2). The output is connected to GND. The circuit includes a 10 uF capacitor (C2) at the input, a 249k 1% resistor (R3) and a 0.47 uH inductor (L2) in the feedback path, and a 10 uF capacitor (C3) at the output. The SGM6029 is configured with A1 to GND, A2 to VDD33, B1 to VDD33, C1 to EN, C2 to EN, C3 to EN, and B2 to SW.

• superCAP needs to be hand-soldered

Y1
RV-3032-C7

VDD_RTC

1 VBACKUP

2 SDA

3 INT

4 EVI

5 VSS

6 VDD

7 CLKOUT

8 SCL

RTC_SQW

VDD33

GND

PWR_FLAG

SDA

I010

I011

RTC_INT

RTC_EVI

VDD_RTC

RTC_SQW

RTC_EVI

R4 10 K

R5 10 K

C24 superCAP

GATE input voltage is LOW then P-channel MOSFET MOSFET connected in the circuit will be turned ON letting VBAT flow to LDO

TP4
COIN BAT + ○
TP5
COIN BAT - ○
GND

VDD

VDD

U3
TP4057-42-SOT26-R

VCC
*STDBY
PROG

VBAT

BAT
GND
*CHRG

5.1k
R11

5.1k
R13

2K2

2K2

GND

D4 RED

D6

VBUS

GND

C12044

J3
SM02B-SR55-TB(LF)(SN)

MP1	1	1
MP2	2	2

VBAT

GND

A circuit diagram showing the connections for a 5-pin header labeled J5. The pins are numbered 1 through 5. Pin 1 is connected to a ground symbol labeled GND. Pin 2 is connected to a rectangular box labeled VDD33. Pin 3 is connected to the text SCL. Pin 4 is connected to the text SDA. Pin 5 is labeled J5.